Light must be coupled to the pixel through a microlens or by back illumination in order to obtain a high effective fill factor; this is necessary to ensure high quantum efficiency, a loss of which would minimize the efficacy of the dynamic-range-enhancement scheme. Once the level of illumination of the pixel exceeds the threshold, TSR is turned on, causing the transfer gate to conduct, thereby adding C_L to the pixel capacitance. The added capacitance reduces the conversion gain, and increases the pixel electron-handling capacity, thereby providing an extension of the dynamic range.

By use of an array of comparators also at the bottom of the column, photocharge voltages on sampling capacitors in each column are compared with a reference voltage to determine whether it is necessary to switch from the high-gain to the low-gain mode. Depending upon the built-in offset in each pixel and in each comparator, the point at which the gain change occurs will be different, adding gain-dependent fixed pattern noise in each pixel. The offset, and hence the fixed pattern noise, is eliminated by sampling the pixel readout charge four times by use of four capacitors (instead of two such capacitors as in conventional design) connected to the bottom of the column via electronic switches SHS1, SHR1, SHS2, and SHR2, respectively, corresponding to high and low values of the signals TSR and RST. The samples are combined in an appropriate fashion to cancel offset-induced errors, and provide spurious-free imaging with extended dynamic range.

This work was done by Bedabrata Pain of Caltech for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1).

In accordance with Public Law 96-517, the contractor has elected to retain title to this invention. Inquiries concerning rights for its commercial use should be addressed to:

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Refer to NPO-41897, volume and number of this NASA Tech Briefs *issue, and the page number.*

Flight Qualified Micro Sun Sensor

Attributes include compactness, low mass, and low power consumption.

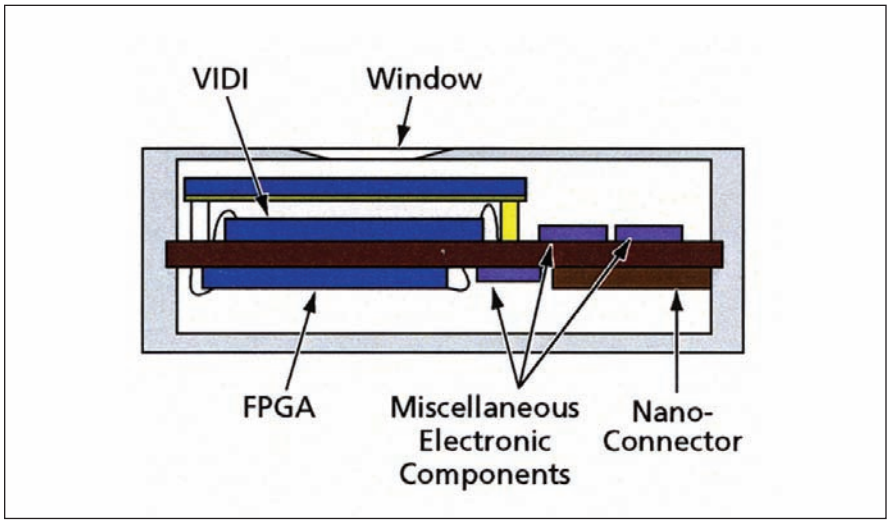
NASA's Jet Propulsion Laboratory, Pasadena, California

A prototype small, lightweight micro Sun sensor (MSS) has been flight qualified as part of the attitude-determination system of a spacecraft or for Mars surface operations. The MSS has previously been reported at a very early stage of development in *NASA Tech Briefs*, Vol. 28, No. 1 (January 2004).

An MSS is essentially a miniature multiple-pinhole electronic camera combined with digital processing electronics that functions analogously to a sundial. A micromachined mask containing a number of microscopic pinholes is mounted in front of an active-pixel sensor (APS). Electronic circuits for controlling the operation of the APS, readout from the pixel photodetectors, and analog-to-digital conversion are all integrated onto the same chip along with the APS. The digital processing includes computation of the centroids of the pinhole Sun images on the APS. The spacecraft computer has the task of converting the Sun centroids into Sun angles utilizing a calibration polynomial.

The micromachined mask comprises a 500-μm-thick silicon wafer, onto which is deposited a 57-nm-thick chromium adhesion-promotion layer followed by a 200-nm-thick gold light-absorption layer. The pinholes, 50 μm in diameter, are formed in the gold layer by photolithography. The chromium layer is thin enough to be penetrable by an amount of Sunlight adequate to form measurable pinhole images. A spacer frame between the mask and the APS maintains a gap of ≈1 mm between the pinhole plane and the photodetector plane of the APS.

To minimize data volume, mass, and power consumption, the digital processing of the APS readouts takes place in a single field-programmable gate array (FPGA). The particular FPGA is a radiation-tolerant unit that contains ≈32,000 gates. No external memory is used so the FPGA calculates the centroids in real time as pixels are read off the APS with minimal internal memory. To enable the MSS to fit into a small package, the APS, the FPGA, and other components are mounted on a single two-sided board following chip-on-board design practices (see figure).



The **Entire MSS** fits into a compact package.

This work was done by Carl Christian Liebe, Sohrab Mobasser, Chris Wrigley, Jeffrey Schroeder, Youngsam Bae, James Naegle, Sunant Katanyoutanant, Sergei Jerebets, Donald Schatzel, and Choonsup Lee of Caltech for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1).
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