does not require a battery backup, yet is has unlimited read and write cycles, and a much smaller access time (60 nanoseconds) than traditional flash memory. The FRAM may be used to store data from the C8051.

The new design of the module creates a robust serial-to-Ethernet conversion that is powered using the existing Ethernet cable. Not only can the module perform these conversions, it also has the processing capability and memory to implement other protocols (like IEEE 1451, IEEE 1588, etc.) and to offload these tasks from other embedded processors.

This innovation has a small form factor that allows it to power processors and transducers with minimal space requirements. The power for the module is provided over the spare pins of the Ethernet CAT-5 cable from Power Source Equipment (PSE) according to IEEE 802.11a. The power and communication module then converts the power into three different voltage levels: 5 volts DC, +12 volts DC and –12 volts DC, which are provided to the embedded processor or transducer through a power header on the PCB.

The power and communication module is also equipped with an Ethernet Controller and microprocessor that can send and receive Internet Protocol (IP)-based packets over the CAT-5 cable on a 10/100 Megabit Ethernet network. The Ethernet controller takes care of overhead communication with the network, and the microprocessor is able to access packets stored in the Ethernet controller's buffer. The microprocessor translates the packets to and from serial data to packets using a standard serial peripheral interface (SPI). The SPI data can be sent and received to another embedded processor over the digital header on the PCB.

The power and communication module is equipped with a hardware watchdog timer that monitors the SPI communication and resets the processors if communications cease. The power and communication module has the additional feature of a real time clock (RTC) that is used to synchronize the time of the power and communication module and its associated embedded processor(s) with the time of another entity on the Ethernet network. Time synchronization is achieved through a combination of hardware and software using the RTC and IEEE 15888 1588 Precision Time Protocol.

This work was done by Jose Perotti of Kennedy Space Center, and Carlos Mata and Rebecca Oostdyk of ASRC Aerospace Corp. Further information is contained in a TSP (see page 1). ***KSC-13112***

Electrically Variable Resistive Memory Devices

Data are written or read using larger or smaller current pulses, respectively.

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Nonvolatile electronic memory devices that store data in the form of electrical-resistance values, and memory circuits based on such devices, have been invented. These devices and circuits exploit an electrically-variable-resistance phenomenon that occurs in thin films of certain oxides that exhibit the colossal magnetoresistive (CMR) effect. It is worth emphasizing that, as stated in the immediately preceding article, these devices function at room temperature and do not depend on externally applied magnetic fields.

A device of this type is basically a thin-film resistor: it consists of a thin film of a CMR material located between, and in contact with, two electrical conductors. The application of a short-duration, low-voltage current pulse via the terminals changes the electrical resistance of the film. The amount of the change in resistance depends on the size of the pulse. The direction of change (increase or decrease of resistance) depends on the polarity of the pulse. Hence, a datum can be written (or a prior datum overwritten) in the memory device by applying a pulse of size and polarity tailored to set the resistance at a value that represents a specific numerical value. To read the datum, one applies a smaller pulse — one that is large enough to enable accurate measurement of resistance, but small enough so as not to change the resistance.

In writing, the resistance can be set to any value within the dynamic range of the CMR film. Typically, the value would be one of several discrete resistance values that represent logic levels or digits. Because the number of levels can exceed 2, a memory device of this type is not limited to binary data. Like other memory devices, devices of this type can be incorporated into a memory integrated circuit by laying them out on a substrate in rows and columns, along with row and column conductors for electrically addressing them individually or collectively.

This work was done by Shangqing Liu, Nai-Juan Wu, Alex Ignatiev, and E. J. Charlson of the University of Houston for Marshall Space Flight Center. For more information, contact Sammy Nabors, MSFC Commercialization Assistance Lead, at sammy.a.nabors@nasa.gov. ***MFS-32511-1***