# G⁴FET Implementations of Some Logic Circuits

## One circuit can be made to perform multiple logic functions.

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Some logic circuits have been built and demonstrated to work substantially as intended, all as part of a continuing effort to exploit the high degrees of design flexibility and functionality of the electronic devices known as G⁴FETs and described below. These logic circuits are intended to serve as prototypes of more-complex advanced programmable-logic-device-type integrated circuits, including field-programmable gate arrays (FPGAs). In comparison with prior FPGAs, these advanced FPGAs could be much more efficient because the functionality of G⁴FETs is such that fewer discrete components are needed to perform a given logic function in G⁴FET circuitry than are needed perform the same logic function in conventional transistor-based circuitry. The underlying concept of using G⁴FETs as building blocks of programmable logic circuitry was also described, from a different perspective, in "G⁴FETs as Universal and Programmable Logic Gates" (NPO-41698), *NASA Tech Briefs*, Vol. 31, No. 7 (July 2007), page 44.

A G⁴FET can be characterized as an accumulation-mode silicon-on-insulator (SOI) metal oxide/semiconductor field-effect transistor (MOSFET) featuring two junction field-effect transistor (JFET) gates. The structure of a G⁴FET (see Figure 1) is the same as that of a p-channel inversion-mode SOI MOSFET with two body contacts on each side of the channel. The top gate (G1), the substrate emulating a back gate (G2), and the junction gates (JG1 and JG2) can be biased independently of each other and, hence, each can be used to independently control some aspects of the conduction characteristics of the transistor. The independence of the actions of the four gates is what affords the enhanced functionality and design flexibility of G⁴FETs.

The present G⁴FET logic circuits include an adjustable-threshold inverter, a real-time-reconfigurable logic gate, and a dynamic random-access memory (DRAM) cell (see Figure 2). The configuration of the adjustable-threshold inverter is similar to that of an ordinary complementary metal oxide semiconductor (CMOS) inverter except that an NMOSFET (a MOSFET having an n-doped channel and a p-doped Si substrate) is replaced by an n-channel G⁴FET. The side gates (JG1 and JG2) are used to linearly modulate the threshold voltage of the G⁴FET, thereby modulating the switching threshold voltage of the inverter. By judiciously selecting the design and operational parameters that affect the switching threshold voltage, the inverter can be made to function as a quaternary down literal converter. (The term "down literal converter" denotes a circuit that performs a function, known as the down

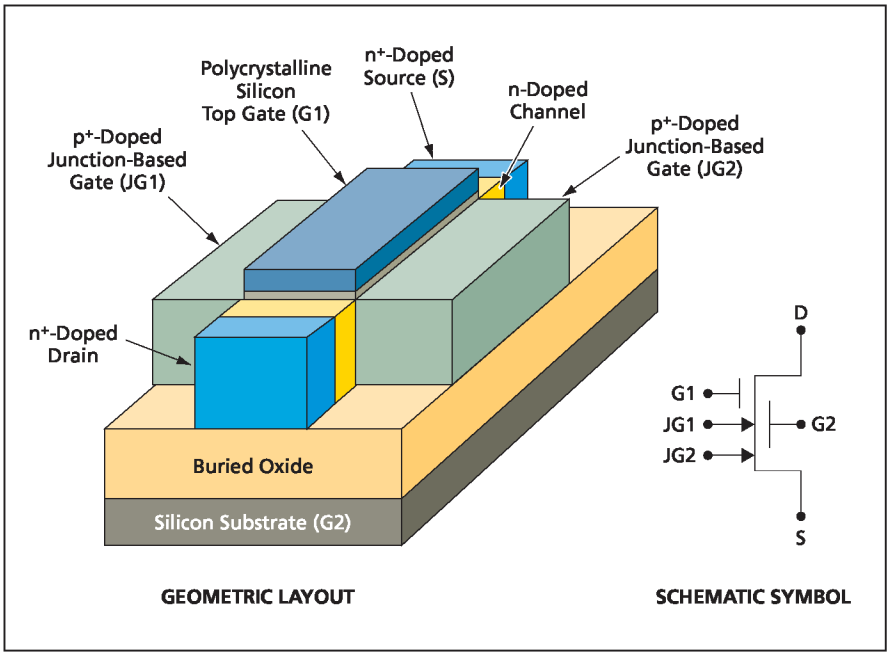


Figure 1. In a **G⁴FET**, the four gates (G1, G2, JG1, and JG2) can be biased independently. JG1 and JG2 can be considered as extra gates that provide additional degrees of freedom for design and operation, beyond those of a conventional MOSFET.

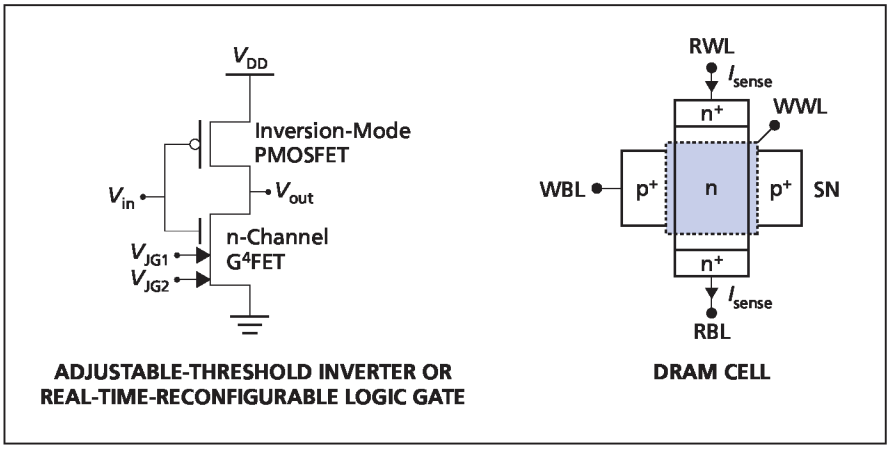


Figure 2. **These G⁴FET Logic Circuits** can be building blocks of complex programmable logic devices.

literal function, that is the fundamental element in multi-valued logic.) Hence, the adjustable-threshold inverter can be made a basic building block of quaternary logic circuits.

The real-time-reconfigurable logic gate can be realized, in a circuit partly resembling the adjustable-threshold inverter, by applying the logic input signals to JG1 and JG2 and connecting the input terminal of what would otherwise be the inverter to a constant reference voltage (that is, making $V_{in}$ a constant voltage). The number of transistors in this circuit is smaller than in a classical CMOS circuit that performs an equivalent logic function. The same hardware can be made to form any of three different functions: Depending on the value of $V_{in}$, the function is disabled output ($V_{out} = V_{DD}$ or 0), the NOR of the logic levels represented by $V_{JG1}$ and $V_{JG2}$, or the NAND of the logic levels represented by $V_{JG1}$ and $V_{JG2}$.

In the DRAM cell, the lateral inversion-mode PMOSFET (a MOSFET having a p-doped channel and an n-doped Si substrate) inherent in the n-channel $G^4$FET is used for writing data in the horizontal direction, while the p-channel JFET serves to read the data in the vertical direction. When the WWL signal turns on the PMOS switch, the potential of the storage node (SN) is modulated by WBL. When writing is disabled, SN is isolated, and during the retention time, its depletion region is more or less extended toward the body, depending on value of the datum stored in it. As a result, the resistance of the JFET channel in the vertical direction is affected, causing the sensing current ($I_{sense}$) to be a function of the stored data. The sensing-current characteristics can be optimized via the layout of the $G^4$FET structure.

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# Electrically Variable or Programmable Nonvolatile Capacitors

## Capacitances are measured using small AC signals or changed using larger pulses.

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Electrically variable or programmable capacitors based on the unique properties of thin perovskite films are undergoing development. These capacitors show promise of overcoming two important deficiencies of prior electrically programmable capacitors:

- Unlike in the case of varactors, it is not necessary to supply power continuously to make these capacitors retain their capacitance values. Hence, these capacitors may prove useful as components of nonvolatile analog and digital electronic memories.
- Unlike in the case of ferroelectric capacitors, it is possible to measure the capacitance values of these capacitors without changing the values. In other words, whereas readout of ferroelectric capacitors is destructive, readout of these capacitors can be nondestructive.

A capacitor of this type is a simple two-terminal device. It includes a thin film of a suitable perovskite as the dielectric layer, sandwiched between two metal or metal oxide electrodes (for example, see Figure 1). The utility of this device as a variable capacitor is based on a phenomenon, known as electrical-pulse-induced capacitance (EPIC), that is observed in thin perovskite films and especially in those thin perovskite films that exhibit the colossal magnetoresistive (CMR) effect. In EPIC, the application of one or more electrical pulses that exceed a threshold magnitude (typically somewhat less than 1 V) gives rise to a nonvolatile change in capacitance. The change in capacitance depends on the magnitude duration, polarity, and number of pulses. It is not necessary to apply a magnetic field or to cool the device below (or heat it above) room temperature to obtain EPIC. Examples of suitable CMR perovskites include $Pr_{1-x}Ca_xMnO_3$, $La_{1-x}Ca_xMnO_3$, $La_{1-x}Sr_xMnO_3$, and $Nb_{1-x}Ca_xMnO_3$.

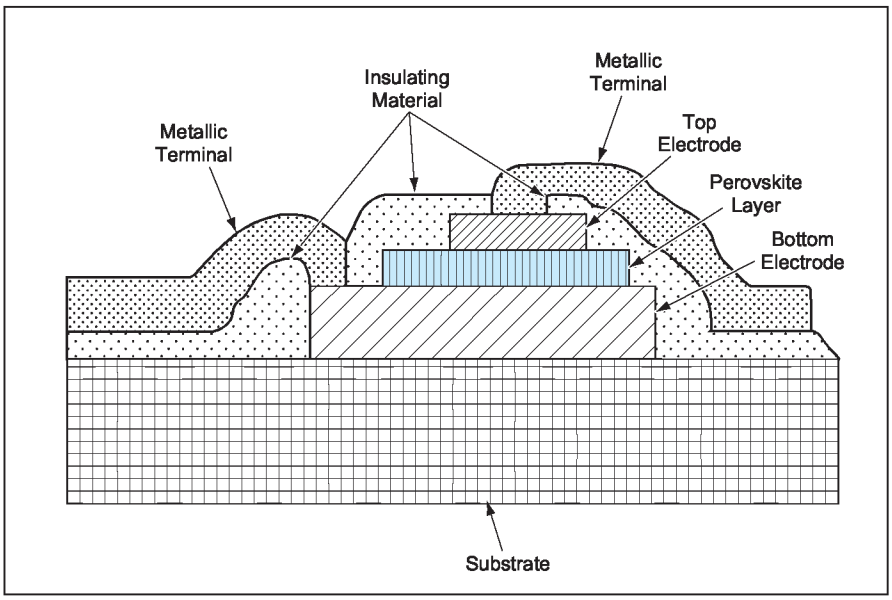


Figure 1. An **Electrically Variable Capacitor** of the type described in the text can be fabricated on a silicon or other substrate as part of an integrated circuit.

Figure 2 is a block diagram showing an EPIC capacitor connected to a circuit that can vary the capacitance, measure the capacitance, and/or measure the re-