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Lightning Pin Injection Testing on MOSFETS

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1 Introduction

The NASA Aviation Safety Integrated Vehicle Health Management (IVHM) Project is conducting research to determine early warning indicators of avionic semiconductor component degradation which can be used to predict the onset of system failures. To understand the interplay between lightning-induced surges and aging (i.e. humidity, vibration thermal stress, etc.) on component degradation, a collaborative research effort has been established between NASA Langley Research Center (LaRC) HIRF Lab personnel and researchers at the NASA Ames Prognosis Center of Excellence to determine the effects of lighting induced electrical transients on MOSFET components. The purpose of this research is to develop validated tools, technologies, and techniques for automated detection, diagnosis and prognosis that enable mitigation of adverse events during flight, such as from lightning transients.[1] Commercial transport airplanes are typically struck by lightning about once every 1000 to 20,000 flight hours.[2] A single lightning strike may result in dozens of voltage or current surges that may exceed the normal operating parameters of semiconductor components installed.[3] This report describes lightning environmental testing which was performed in January and February 2009. The effort fits within "Aircraft Systems Health Management" Discipline-Level research, Diagnosis milestone 2.1.2.2 and Prognosis milestone 2.1.3.1; and "Advanced Sensors and Materials" Foundational-Level Research milestone 1.1.2.1.

2 Objective

The test objective was to evaluate MOSFETs for induced fault modes caused by pin-injecting standard lightning waveforms into the semiconductor components. Lightning Pin-Injection testing was performed at NASA LaRC. Fault mode and aging studies are currently being performed by NASA Ames researchers using their Aging and Characterization Platform for semiconductor components, for the purpose of developing predictive algorithms as part of IVHM prognostic health management program goals. This report documents the test process and results, to provide a basis for subsequent lightning tests. It is expected that NASA Ames researchers will use this report and test data files as part of their continued fault-mode and aging research and publications.

3 Approach

NASA Ames Research Center IVHM researchers supplied 400 identical IRF520NPBF Power MOSFETS. IRF520NPBF MOSFETS are manufactured in a TO-220 package as shown in Figure 1. The IRF520NPBF was selected to be representative of devices that are present in DC-DC power supplies and electromechanical actuator circuits that will be used on board aircraft. Most of the MOSFETS were characterized prior to arriving at LaRC using the NASA Ames Aging and Characterization Platform for power transistors.[4] Elements of the system were transported to NASA LaRC to use for characterizing damage caused by lightning pin-injected transients. For all tests described herein, the MOSFETS were unpowered during lightning pin-injection tests (i.e., not connected to any circuitry other than lightning generator).

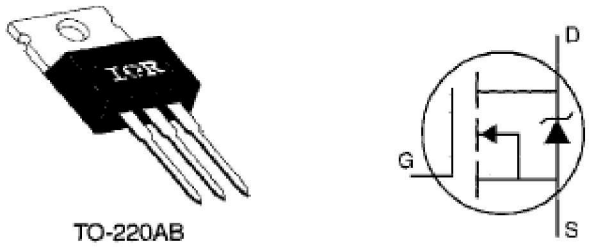


Figure 1: IRF520NPBF MOSFET package (left) and schematic (right).

3.1 RTCA/DO-160E Lightning Waveforms

RTCA/DO-160E "Environmental Conditions and Test Procedures for Airborne Equipment", Section 22 "Lightning Induced Transient Susceptibility", was used.[5] DO-160E Section 22 includes procedures for pin-injection and cable bundle tests, and is intended for establishing flight worthiness of airborne equipment. DO-160E test processes are intended for assembled electronic systems, rather than individual components, so these tests were modified to accommodate the special situation of testing individual components. The DO-160E lightning- induced voltage Waveform 3 "Damped Sinusoid" and voltage Waveform 4 "6.4 μs-Rise Double Exponential" were originally selected for these tests, and Waveform 5 was added to augment the severity of the applied lightning environment for the MOSFET Drain-Source pin injection test. See Figure 2 for description of the lightning waveforms.

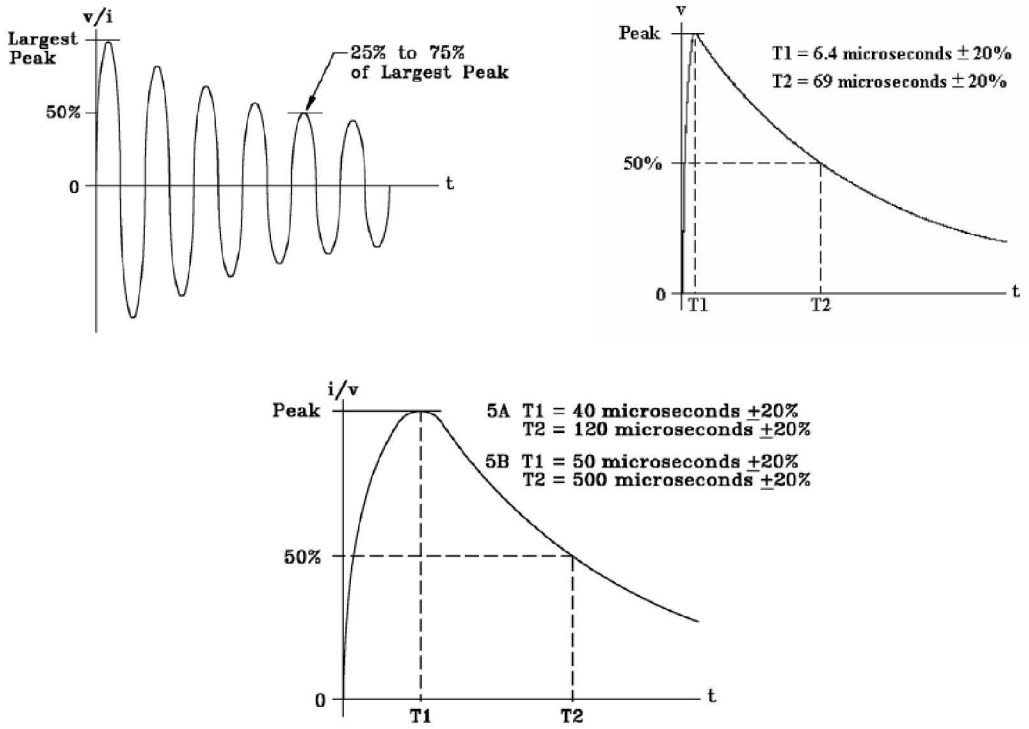


Figure 2: RTCA Voltage/Current Waveform 3 (top left, frequency= 1MHz for pin-injection testing), Voltage Waveform 4 (top right) Current/Voltage Waveform 5 (bottom).

DO-160E recommends Waveforms 3 (1MHz) and 4 for airborne equipment that may be subjected to lightning-induced magnetic fields coupled onto their wiring. Waveform 5 is recommended for pin-injection testing when avionics wiring may be subjected to direct conduction currents created as lightning current flows through the airframe. Peak DO-160E Test Levels for Waveforms 3, 4 & 5A are shown in Table 1. DO-160E allows devices to be un-powered during pin-injection testing. For all tests described herein, the devices were unpowered.

Table 1: DO-160E Generator Peak Test Levels for Pin Injection

Level	Representative Environment	Waveform 3 (WF3) Voc/Isc	Waveform 4 (WF4) Voc/Isc	Waveform 5A (WF5A) Voc/Isc
1	Well Shielded	100/4	50/10	50/50
2	Partial Shielded	250/10	125/25	125/125
3	Partial Exposed	600/24	300/60	300/300
4	Severe	1500/60	750/150	750/750
5	More Severe	3200/128	1600/320	1600/1600
	Source Impedance:	WF3: 25 Ohms	WF4: 5 Ohms	WF5: 1 Ohm

3.2 Facility and Equipment

All testing was conducted in NASA's High Intensity Radiated Field (HIRF) Laboratory, located in Building 1220, Room 144, on 1 South Wright Street at NASA LaRC. The HIRF Laboratory is typically used for reverberation chamber radiated emissions and immunity testing. However, the reverberation chambers are easily adapted to lightning testing. An overview of HIRF Laboratory capability is provided in the Reference section[6,7,8]. The HIRF Laboratory is equipped with EMC Partner MIG-System generators for lightning indirect effects testing, and is capable of performing DO-160E Section 22, up to Test Level 5 for pin, cable and ground injection for Waveforms 1, 4 and 5. Waveform 2 & 3 tests can be performed up to Test Level 3. Multiple stroke and multiple burst tests, as specified in DO-160E Section 22 can also be performed. The HIRF laboratory is also able to perform additional test types beyond DO-160E. Figure 3 shows the EMC Partner equipment that was used for pin-injection tests, and Table 2 summarizes the test equipment used.

Table 2: Test Equipment

Equipment Item	Manufacturer/Model	SN/ECN	Cal. Due
Impulse Gen. (WF 4 & 5, Lev. 1 to 4)	EMC Partner MIG0600MS	260/2104741	N/A
Impulse Gen. (WF 4 & 5, Lev. 2 to 5)	EMC Partner MIG0618SS	751/2205667	N/A
Impulse Gen. (WF 3)	EMC Partner MIG-OS-MB	216/2104742	N/A
Step Down 1:8 Transformer	EMC Partner NW-MS-Level1	SN002	N/A
Oscilloscope	Tektronix DPO4054	ECN1641291	1/9/2010
Current Sensor 100X	Pearson 5046	120468/A037686	7/9/2008*
High Voltage Probes (2)	Tektronix P5100	N/A	N/A
MOSFET Test Board	Provided By NASA Ames	N/A	N/A

*The Pearson 5046 Current Sensor calibration was expired during this test. Subsequently, on August 28, 2009, the probe calibration was verified to be within specification.
(NASA Ames personnel used a Component Evaluation System, consisting of a Keithley 2410 SourceMeter, a Dell PP05XA Notebook computer and a National Instruments GPIB-USB-HS adapter for their MOSFET characterizations. The NASA Ames equipment was not part of the pin injection test setup but is later described in Section 5 of this report.)

Figure 3: EMC Partner lightning-generating equipment was used for pin-injection tests.

3.3 Test Setup

NASA LaRC personnel pin-injected lightning Waveforms 3, 4 and 5a into the IRF520NPBF MOSFETS using each combination of input terminals (i.e. Gate-Drain, Gate-Source, and Drain-Source). The unused MOSFET terminal was left unconnected. NASA Ames personnel performed functional testing of components after lightning pin-injection tests, to assess damage. Figure 4 shows the Pin Injection Test Setup. Oscilloscope Settings are shown in Table 3, and Lightning Generator connections and settings are shown in Table 4.

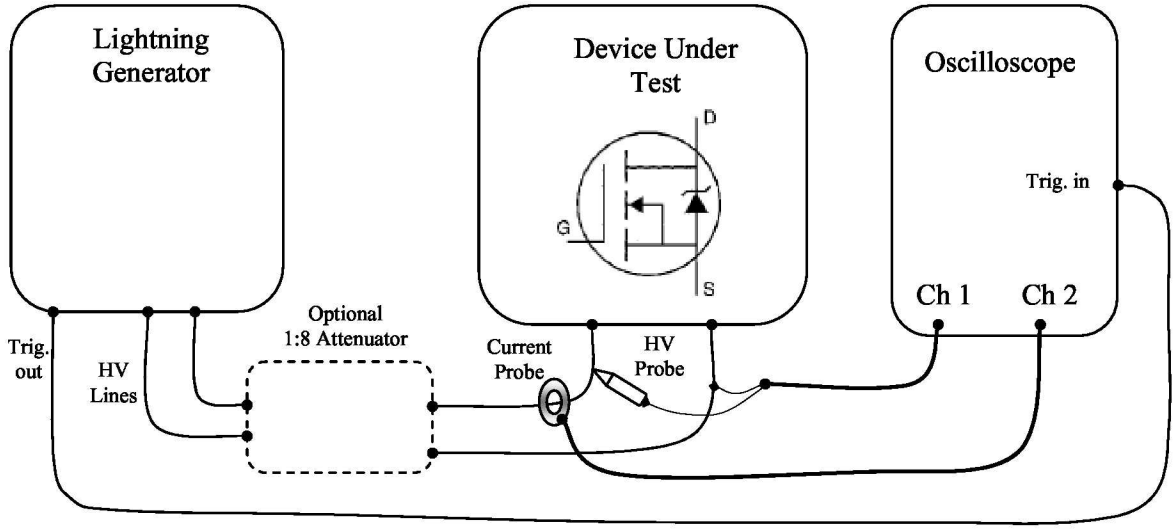


Figure 4: Pin injection test setup diagram. (High voltage 'HV' lines were each 81.5"+43.0"= 124.5 inches long. Two sections allowed connection-to/bypass-of Attenuator Box.)

In Figure 4, the Device Under Test is simply an IRF520NPBF MOSFET mounted in a socket soldered to a circuit board. On the test board, MOSFET terminals are routed to banana jacks for simple interconnect with laboratory equipment.

Table 3: Oscilloscope Settings

Parameter	**Setting**	
Timebase	20 uS (WF4) 2 uS (WF3)	
Trigger	Edge, Source=Ext. Coupling=DC, Slope=Pos, Level= 8000mV	
	Channel 1	**Channel 2**
Level	Varied	Varied
Coupling	DC	DC
Position	0 Div	0 Div
Offset	0 V	0 A
Probe	100X Voltage	100X Current
Input Impedance	1M Ohm	1 M Ohm

Table 4: Lightning Generator Connections & Settings

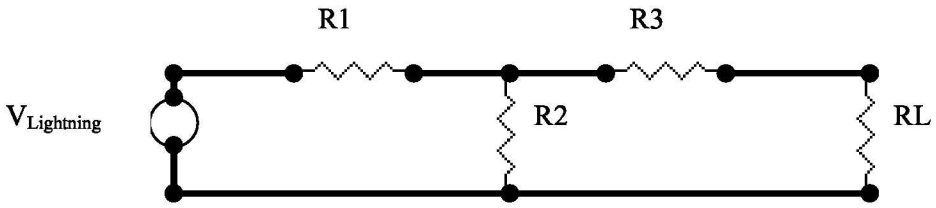
Transient Generator	**MIG-OS-MB (80V minimum)**	**MIG0600MS (70V minimum)**	**MIG0618SS (125V minimum)**
Connections	-High Voltage -Trigger	- High Voltage -Trigger -Use NW-MS-LEVEL1 Step Down 1:8 Transformer if VPeak below 80V	- High Voltage -Trigger
Settings	1. On/Stby Press 2. Safety Ckt- Closed 3. Waveform 3 (1MHz) 4. VPeak: Test Matrix 5. Polarity: Pos 6. Trig. Mode: SS=Manual, MS=Auto, Test Time, Repetition	1. On/Stby Press 2. Safety Ckt- Closed 3. Waveform 4 4. VPeak: Test Matrix 5. Polarity: Pos 6. Trig. Mode: SS=Manual, MS=Auto, Test Time, Repetition	1. On/Stby Press 2. Safety Ckt- Closed 3. Waveform 4 4. VPeak: Test Matrix 5. Polarity: Pos 6. Trig. Mode: SS=Manual, MS=Auto, Test Time, Repetition

The Figure 4 test setup allows the oscilloscope to capture the actual voltage and current waveforms applied to the device-under-test. Several methods were compared for saving oscilloscope data.

- Tektronix Open Choice Desktop .XLS (Microsoft Excel format)
- Tektronix Open Choice Desktop .CSV (Comma Separated Variable)
- Agilent VEE Custom Program
- ★ Direct .CSV output from Tektronix DPO4054 USB port.

After some experimentation, it was decided to use the Direct .CSV output from the Tektronix DPO4054 USB port, using a memory stick. This option had the benefit of being fast and simple, with standard data formatting. The default filenames were formatted as "tekXXXXALL", to save all traces, where XXXX is a counter that resets to zero in any new folder. (If there are existing "tek" files in the folder, it will append XXXX.)

Some testing required pin-injection levels below DO-160E Level 1. The EMC Partner MIG-OS-MB Lightning Waveform generator does not allow testing below 80V peak. To accommodate test voltages below 80V, a resistor network was used to reduce Open-Circuit voltage of Waveform 3 by half, while still maintaining the correct source impedance. A schematic of the resistor network is shown in Figure 5, and a photograph of its implementation is shown in Figure 6.



R1= Lightning Generator Source Impedance
RL= Load Impedance of Test Device
R2= R1
R3= ½ R1

Figure 5: Circuit Schematic to enable Waveform 3 testing down to 40V Peak with MIG-OS-MG Transient Generator. Actual values were R1=25 Ohm, R2=25 Ohm, R3=12.5 Ohm.

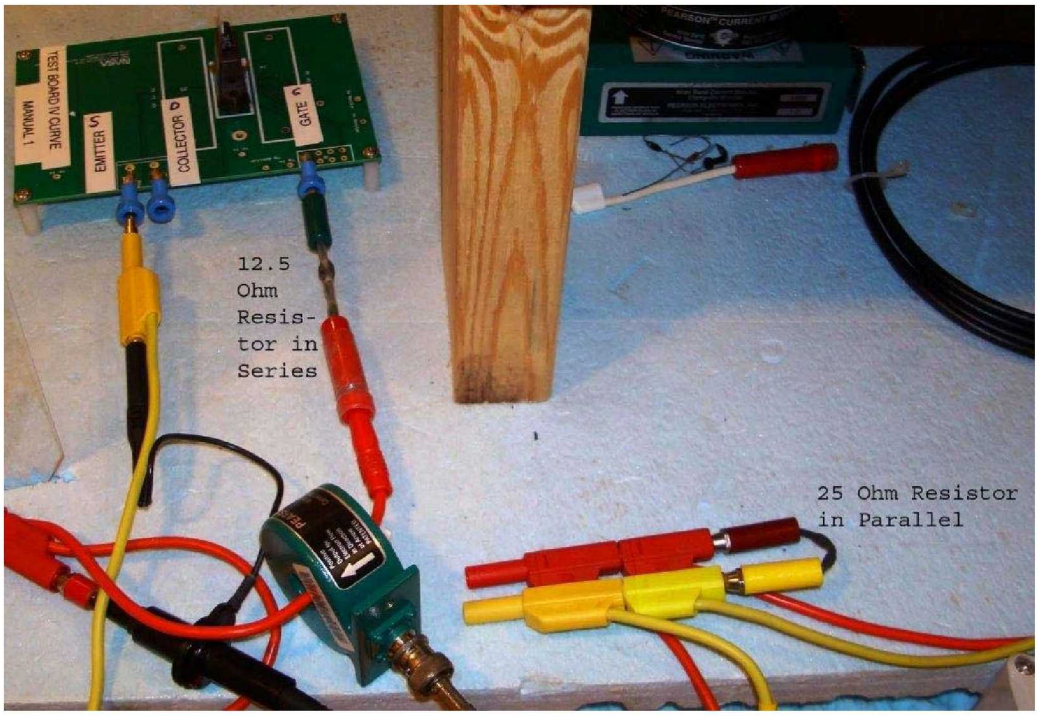


Figure 6: Photograph of R2=25 Ohms (in parallel), R3=12.5 Ohms (in series), implementation.

3.4 Safety Hazards & Precautions

Test Personnel were briefed on the standard HIRF Laboratory Safety procedures, including:

- Location of Exits
- Marshalling Areas
- Location of Fire Extinguishers and AEDs, qualified AED Responders
- Out-Of-The-Ordinary operations: (i.e. construction, blocked exits, auditory alarms, other testing, etc.)

Test operations complied with all NASA LaRC electrical safety standards and requirements. The following warning was prominently displayed in the test Plan:

> **WARNING**
> The transient generators used in these tests produce lethal voltage and current levels.
> Exercise all operational safety precautions to prevent injury or death of test and support personnel.

A Hazards Identification Meeting was held to discuss additional safety hazards and to identify precautions and controls to mitigate them. Table 5 shows the hazards identified and their precautions and controls.

Table 5: Lightning Generator Connections & Settings

Hazard	**Precaution**
1. High Voltages: Source Measurement Unit	All Personnel: 1ft clearance from device and all high voltage connections when source measurement unit (SMU) blue light is ON.
2. High Voltages: Lightning Transient Generator	All Personnel: 1ft clearance from device and all high voltage connections when generator is in RUN mode.
3. Un-Authorized Personnel in Test Area	-Post "DANGER: TEST IN PROGRESS" sign during all high voltage test operations. -Test personnel instructed to stop test when unauthorized personnel in Chamber B.
4. Device Destruction during HV Test	Place clear safety shield over device during lightning transient testing.
5. Inadvertent Operation Lightning Transient Generator	-Push SAFETY CIRCUIT button to OFF on Lightning Transient Generators when test operations are not being conducted.

4 Results Summary

4.1 Pre-Test

To check the accuracy of the MIG0600MS and MIG-OS-MB Lightning Generator displays prior to MOSFET testing, the Open Circuit Voltage (OCV) was measured at several setting points. Table 6 shows the data. Essentially, both units' displays were found to understate the OCV by 3% to 35%. Table 6 shows the maximum OCV obtained after several repetitions. Minimum OCV values were found to be no more than 6% lower than the maximum values shown in Table 6.

Table 6: VOC Data for MIG0600MS and MIG-OS-MB

V_{out} Setting (nominal)	**Measured OCV from MIG0600MS (Waveform 4)**	**Measured OCV from MIG-OS-MG (Waveform 3)**
10	11.0 * (110%)	-
20	22.6 * (113%)	-
40	45.6 * (114%)	-
80	82.0 (103%)	95.5 (119%)
160	164 (103%)	193 (121%)
320	332 (104%)	378 (118%)
640	682 (107%)	730 (114%)
1280	1359 (106%)	1730 (135%)
1700	1798 (106%)	2270 (134%)

*(NW-MS-LEVEL1 step down 1:8 transformer required)

A Pre-Test procedure was used to determine single-stroke test level required to cause permanent damage, for each input pin configuration (i.e. Source-Drain, Source-Gate, and Gate-Drain). The Lightning Transient Generator was connected to two pins of a single MOSFET at a time. The third pin was left unconnected (open-circuit). Single stroke waveforms 3 and 4 were used for most tests. For a particular waveform and pin configuration, the test level was increased until a change was observed on the current & voltage waveforms displayed on the oscilloscope. The MOSFET was then evaluated using the NASA Ames Component Evaluation System. The pin nomenclature is shown in Table 7.

Table 7: Pin Connection Nomenclature

Pin Configuration	**+ Voltage Connected To:**	**- Voltage Connected To:**
① G-D	Gate	Drain
❶ D-G	Drain	Gate
② G-S	Gate	Source
❷ S-G	Source	Gate
③ D-S	Drain	Source
❸ S-D	Source	Drain

The Pre-Test procedure facilitated an understanding of setups, including Current Probe orientation ("Positive Output for Electron Flow in Direction of Arrow"), and correct oscilloscope input impedance setting (i.e. 1 M Ohm). Table 8 shows lightning generator settings required to cause MOSFET failure ("failure" is defined as device malfunction) for each Waveform. Waveform 5 was used only for the S-D configuration, and was used because the MOSFET-under-test could not be made to fail given the maximum setting of the MIG0600MS generator. Only three pin configurations were tested with Waveform 3 (rather than 6 pin configurations), because connection polarity was assumed to be irrelevant (I.e., waveform 3 is a damped sinusoid. See Fig. 2.)

Table 8: MOSFET Fail Levels

Device SN	Wave-form	Pin Config.	V_{Peak} Set (Voc)	V_{Fail} Meas (Volts)	I_{Fail} Meas (Amps)	Filename
F0	4	① G-D	90	86.8	56mA to >1A	0024
F3	4	② G-S	100 (80)*	91.7	107mA to >1A	0034 (0138)
F4	4	③ D-S	240 (280)*	95.0	31A	0043 (0239)
F5	4	❶ D-G	200	107.7	63mA to >2.5A	0051
F6	4	❷ S-G	70	68.2	50mA to >1A	0059
F7	4	❸ S-D	1700 Max	62.2 NoFail	365A NoFail	0102
F8	5a	❸ S-D	1650 Max	>100 **	>1008A **	0104
V6	5b	❸ S-D	1650	237	1469A	0509
F9	3	G-D| D-G	90 (80)*	98.0 (88.0)	>1.9A (789mA)	0106 (0105)
G0	3	G-S | S-G	80 (55)*	95.9	1A	0107 (0848)
G1	3	D-S | S-D	2200 Max	250.9 **	82A **	0131

* Subsequent Testing Updated Fail Levels shown in ( ).
** No discontinuities in oscilloscope data, but NASA Ames Aging and Characterization Platform showed device failure.

Voltage and Current versus Time plots are shown in Figures 7 through 10, for the Waveform 3 & 4 failures noted in Table 8. Waveform 5 S-D failure plots are provided separately in Section 4.3. In every case, the current *increased* after failure, which is an interesting result.

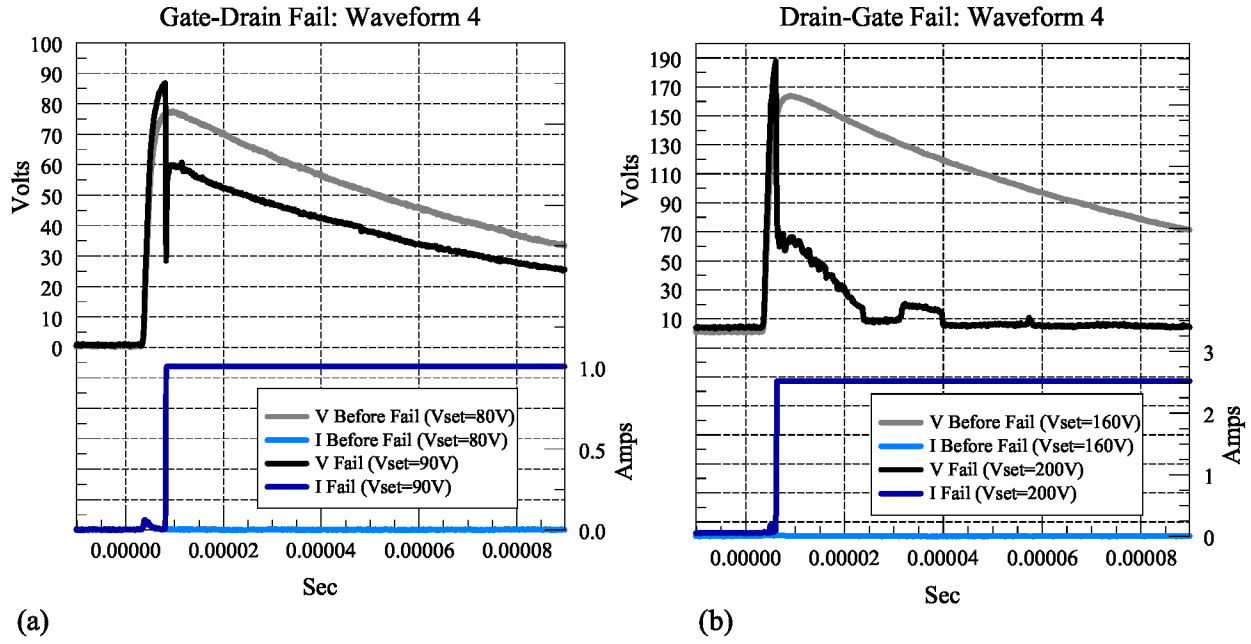


Figure 7: (a) ① G-D fail plot for Waveform 4 shows V and I before failure (file 0023, Vset=80V) and after failure (file 0024, Vset=90V). (b) ❶ D-G fail plot for Waveform 4 shows V and I before failure (file 0050, Vset=160V) and after failure (file 0051, Vset=200V).

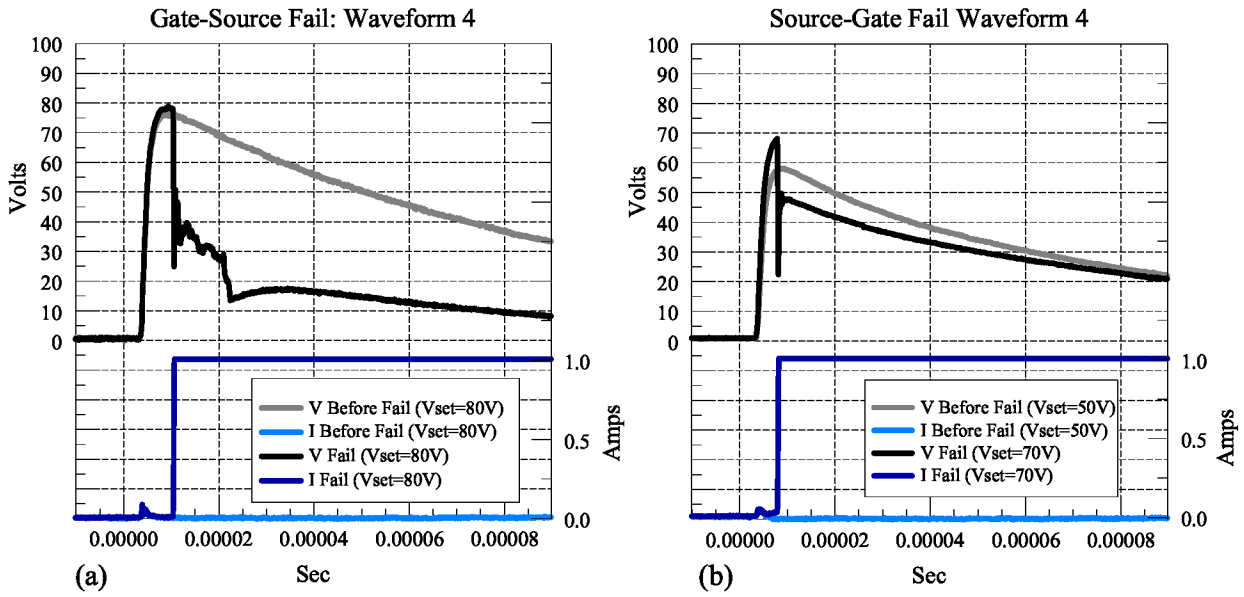


Figure 8: (a) ② G-S fail plot for Waveform 4 shows V and I before failure (file 0137, Vset=80V) and after failure (file 0138, Vset=80V). This device initially showed no change in the I and V data with Vset=80V, however, it failed on Stroke #7 of the multiple stroke test. (b) ❷ S-G fail plot for Waveform 4 shows V and I before failure (file 0058, Vset=50V) and after failure (file 0059, Vset=70V).

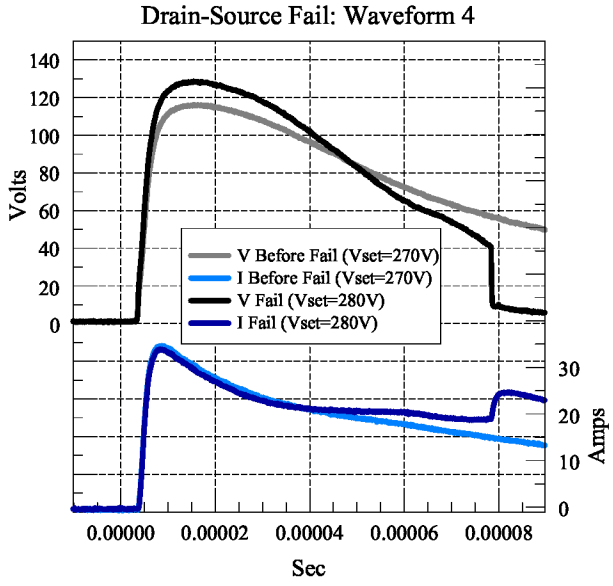


Figure 9: ③ D-S fail plot for Waveform 4 shows V and I before failure (file 0238, Vset=270V) and after failure (file 0239, Vset=280V). The ❸ S-D fail plot is of special interest, and is discussed separately in Section 4.3.

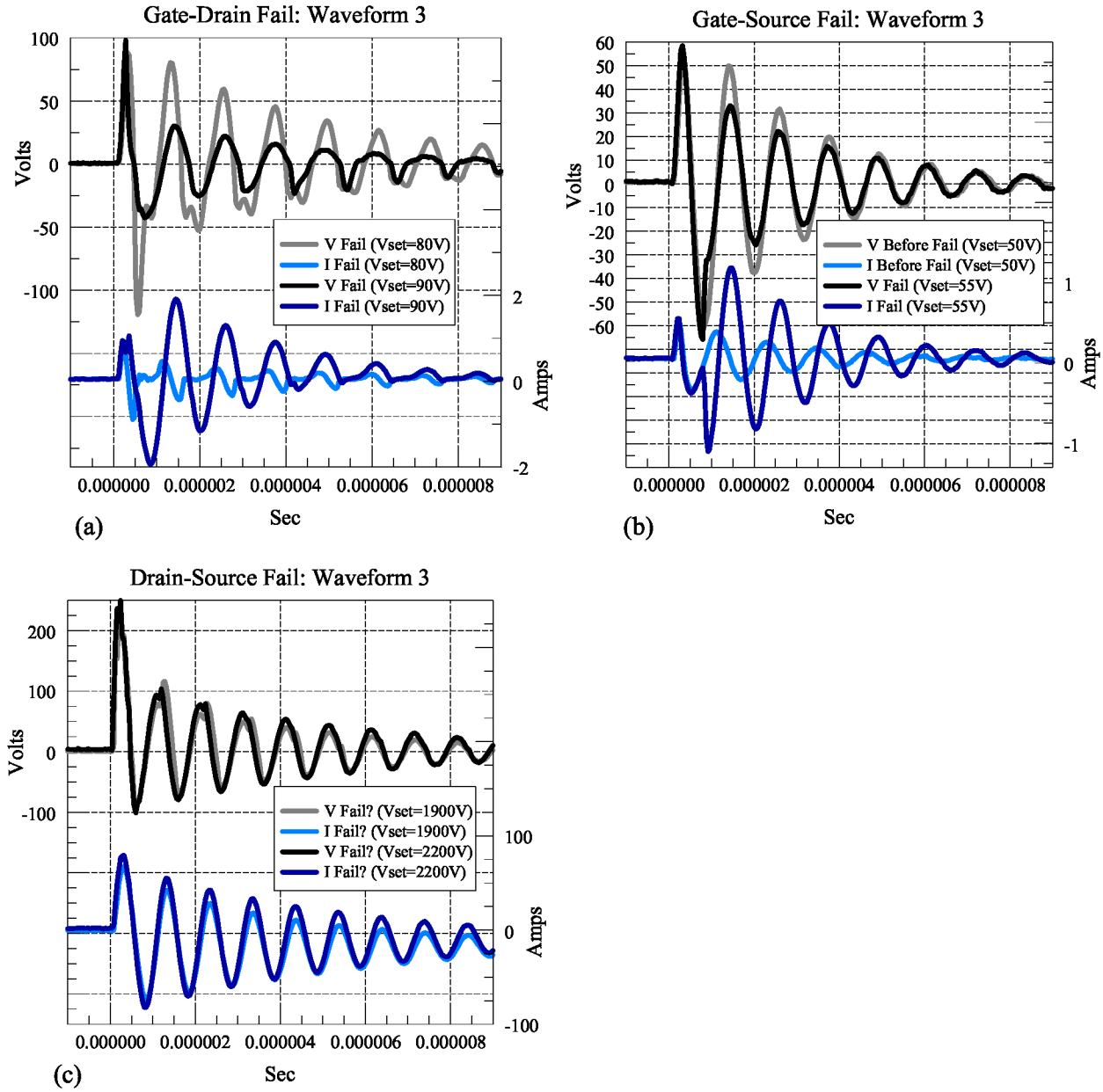


Figure 10: (a) G-D|D-G fail plot for Waveform 3. Although unrecognized during testing, it is apparent from the plot (note V and I discontinuity at 0.0000005 sec) that the device actually failed during the first test (file 0105 Vset=80V). In the subsequent test (file 0106, Vset=90V) note that the current (I) is much higher than before.
(b) G-S|S-G fail plot for Waveform 3 shows V and I before failure (file 0847, Vset=50V) and after failure (file 0848, Vset=55V).
(c) D-S|S-D plot for Waveform 3. During testing it was recorded that the device responded in a typical manner with Vset=1900V (file 0130), with failure occurring with Vset=2200V (file 0131). However, it is not apparent from the plot that device failure occurred with either setting.

NASA Ames researchers needed to determine the highest V_{Fail} setting where a MOSFET can tolerate up to 20 lightning strokes without apparent failure. Such a test would model a scenario where a MOSFET is subjected to about two lightning strikes. (A typical lightning strike contains about 10 strokes.[9]) Using the data from Table 8 as a guide, more MOSFETs were tested to determine the highest V_{Fail} setting where the device could tolerate 20 strokes without failure. The final data is shown in Table 9. As expected, the 20-stroke Pass Level was lower than the Single Stroke Fail Level for most pin configurations. The only exception was for the D-S configuration. Several additional MOSFETS passed multiple stroke tests above 240V in the D-S configuration, with a failure occurring at 280V. So, it was deduced that the 240V failure shown in Table 8 was an anomalous finding.

Table 9: MOSFET Pass Levels after 20 Strokes

Device SN	Waveform	Pin Config.	V_{Peak} Set (Voc)	V_{Peak} Meas	I_{Peak} Meas	Filename
I6	4	① G-D	75	71.7	63mA	0277
H5	4	② G-S	76	73.4	85mA	0253
H6	4	③ D-S	266	14.7	52A	0257
H9	4	❶ D-G	170	172.7	172mA	0263
I3	4	❷ S-G	55	63.4	62mA	0270
I7	4	❸ S-D	1700 Max	62.2 NoFail	365A NoFail	0281

The 20-Stroke Pass Levels were taken to be the "High" setting for subsequent testing. "Medium" and "Low" settings were taken to be 90%, and 80% of "High", respectively. The values 80% and 90% were selected, somewhat arbitrarily, expecting that some statistical difference may be obtained from device failures after subsequent aging processes (thermal, vibration, etc.) to be conducted at NASA Ames. A summary of the High, Medium, and Low Test Levels, along with Fail Levels is shown in Table 10. It is important to note that polarity was found to affect the Fail Levels when using Waveform 3.

Table 10: Final Test Voltage Levels determined from Pre-Test

Pin Config	W4 Fail (V)	W4 HI: Pass 20 Strokes	W4 Med=90% of HI	W4 Lo=80% of HI	W3 Fail (V)	W3 HI Pass 20 Strokes	W3 Med=90% of HI	W3 Lo=80% of HI	W5a Fail (V)	W5b Fail (V)
① G-D	90	75	68	60	90	86	77	68		
② G-S	80	76	68	61	55	47	42	40		
③ D-S	280	266	239	213	2200	2090	1881	1672		
❶ D-G	200	170	153	136	*90*	*86*	*77*	*68*		
❷ S-G	70	*55*	50	44	*55*	*47*	*42*	*40*		
❸ S-D	>1700				*>2200*				>1650	1650

(Waveform 3 S-D, S-G and D-G values are italicized to denote that the values were not measured directly, but assumed from corresponding data of opposite polarity: i.e. D-S, G-S and G-D *data.)*

4.2 Test Matrix

Table 10 summarizes all the pre-test results. The next step was to produce multiple samples of MOSFETS having been subjected to different test levels, varying numbers of strokes, and varying pin-injection configurations. The devices may then be subjected to various aging processes and statistical data obtained for latent failures. Using lightning Waveform 4, five MOSFETS were tested at High, Medium and Low Test Levels, with 5, 10 and 20 strokes, resulting in 45 devices tested for each pin configuration. Waveform 4 was the primary focus for this testing, however, there were additional devices

available to test Waveform 3 also. For Waveform 3, only the G-S pin configuration was tested, with 4 samples of each device. All test data are summarized in Table 11. The 302 MOSFETS are subsequently being evaluated by NASA Ames researchers using their Aging and Characterization Platform for semiconductor components, for the purpose of developing predictive algorithms as part of IVHM prognostic health management program goals.

Table 11: Final MOSFET Test Data Summary

Waveform	Pin Config.	Levels	Strokes	Samples Each	Devices Tested
4	① G-D*	H, M, L	5, 10, 20	5	3 x 3 x 5= 45
4	② G-S	H, M, L	5, 10, 20	5	3 x 3 x 5= 45
4	③ D-S	H, M, L	5, 10, 20	5	3 x 3 x 5= 45
4	❶ D-G	H, M, L	5, 10, 20	5	3 x 3 x 5= 45
4	❷ S-G	H, M, L	5, 10, 20	5	3 x 3 x 5= 45
4	❸ S-D	H, M, L	5, 10, 20	5	3 x 3 x 5= 45
3	G-S|S-G	H, M, L	5**, 10, 20	4	8+12+12=32
Total MOSFETS Tested					302

*Extra data was obtained for the G-D configuration because the test setup was left in that configuration during the first attempted S-G test. (i.e., S-G levels used for G-D configuration)

** G-S High Test Level was performed with 10 and 20 strokes (not 5) to conserve MOSFETS

4.3 Physical Damage MOSFET Test

From Tables 8, 9 and 10, it can be seen that the S-D pin configuration was highly resistant to damage by injecting lightning waveforms. Using Waveform 4, the V_{Peak} setting of 1700V resulted in an MOSFET terminal voltage of 62.2V and a current of 365 Amps, with no apparent functional damage. Comparing Waveforms 4 and 5 in Figure 2 shows that Waveform 5A contains more energy than Waveform 4 (i.e. level decreases to 50% in 120 µsec versus 69 µsec), and Waveform 5B contains more energy than Waveform 5a (i.e. level decreases to 50% in 500 µsec versus 120 µsec) . As part of the Pre-Test, Waveform 4, 1700V (maximum setting) was applied to MOSFET F8, without apparent damage. Then, Waveform 5A was applied with 1650V (maximum setting). The resulting plot is shown in Figure11a. At the time, it was thought that the MOSFET was damaged; however, subsequent data review indicated a likelihood that the discontinuous oscilloscope display was caused by the measurement being out-of-range instead. To evaluate the damage scenario further, the team decided to try again with Waveform 5B. The V_{Peak} set level was increased in steps, and repeatedly applied to the same MOSFET (V6). Surprisingly the MOSFET withstood a V_{Peak} Set (Voc) of 1400V, with voltage and current values of 105V and 1326A developed over the MOSFET S-D terminals, respectively. When V_{Peak} Set (Voc)= 1650 V was reached, the MOSFET exploded with a sound comparable to a firecracker. The final MOSFET terminal voltage and current values were V_{Peak}= 237V and I_{Peak}= 1469A. The resulting plot is shown in Figure11b. A photograph of the exploded MOSFET is shown in Figure 12. This test demonstrated that lightning-induced transients from an IRF 520 MOSFET Source-to-Drain are significantly less likely to be damaged than other pin configurations. As shown in Figure 1, the IRF520NPBF includes an integral reverse p-n junction source-to-drain diode, which is likely responsible for the high source-to-drain current characteristic.

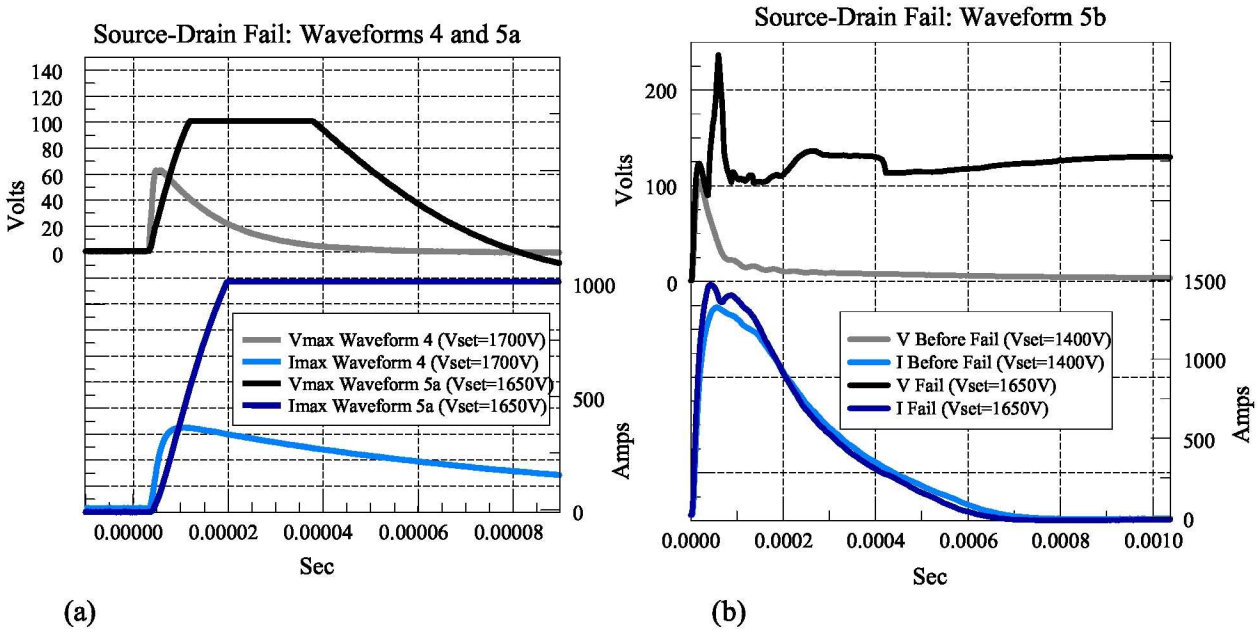


Figure 11: (a) ❸ S-D plot for Waveforms 4 (file 0103, Vset=1700V) and 5a (file 0104, Vset=1650V). It is unlikely that the MOSFET was damaged by either stroke, rather it is likely that the discontinuous oscilloscope display was because of the measurement being out-of-range instead. The plot shows V and I before failure (file 0847, Vset=50V) and after failure (file 0848, Vset=55V). (b) ❸ S-D fail plot for Waveform 5b shows V and I before failure (file 0508, Vset=1400V) and after failure (file 0509, Vset=1650V). After failure, the current remained similar to before, however, the voltage remained over 100V, indicating significant additional deposit of energy into the device.

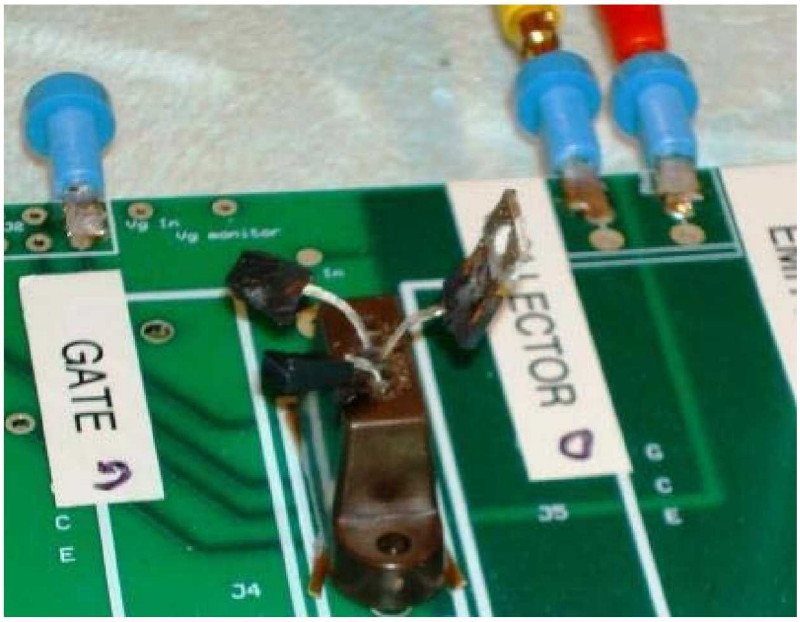


Figure 12: Photograph of exploded MOSFET.

5 Preliminary Damage Assessment Based on Electrical Parameters

Lightning pin-injection into power MOSFETs can result in total damage after which the device does not operate as intended (which is defined as "Fail Level" in this report). On the other hand, there could be damage that manifests itself in changes on key operational parameters of the device. In such cases, the device may still perform its switching operation but under diminished performance. Three key MOSFET parameters are Breakdown Voltage, Leakage Current and Threshold Voltage. In this section, these parameters are evaluated to provide a preliminary assessment of the damage level of a MOSFET after pin-injection of a lightning waveform.

5.1 Breakdown Voltage

The Breakdown Voltage ($V_{(BR)DSS}$) indicates the voltage at which the drain-to-source path of the device starts conducting drain current (I_D) given that the gate is not biased (V_{GS}=0V). When the gate is not biased, the drain-source path should behave like an open circuit and very little current (in the μA range) should flow through the device. As the voltage applied to the drain and source terminal (V_{DS}) increases it reaches a point when the device starts conducting current, this is known as the Breakdown Voltage. A source measurement unit (SMU, also identified as the Keithley 2410 SourceMeter in Section 3.2) is required to assess the value of this parameter. The SMU is able to source large voltages while measuring the supplied current with high precision (usually at the pA level). Figure 13 shows the configuration of the Breakdown Voltage test. The SMU equipment is controlled via a LabView virtual instrument in order to automate the drain-source voltage sweep to identify the Breakdown Voltage.

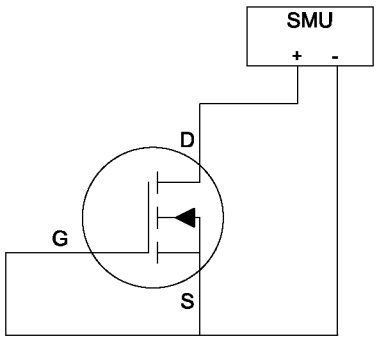


Figure 13: Configuration of Leakage Current and Breakdown Voltage tests for an n-type power MOSFET.

The Breakdown Voltage rating for the MOSFET IRF520NPbF is available in the manufacturer datasheet[10]. The datasheet shows that at room temperature the minimum rated Breakdown Voltage is $V_{(BR)DSS}$= 100V, at I_D= 250uA and V_{DS}= 0V.

Figure 14 shows the I-V curve sweep results on V_{DS} and I_D which is used to identify $V_{(BR)DSS}$ for device J9. Device J9 was injected with the G-S configuration using a high-voltage setting (76V) and 20 consecutive strokes. As a result of the repeated injection, the Breakdown Voltage shifts to the left by ~1 V. It should be noted that even after the injection, the Breakdown voltage still complies with the rating given in the datasheet. It is also evident that there is damage due to the injections and it should be investigated further whether such damage affects the future operation and remaining useful life of the device.

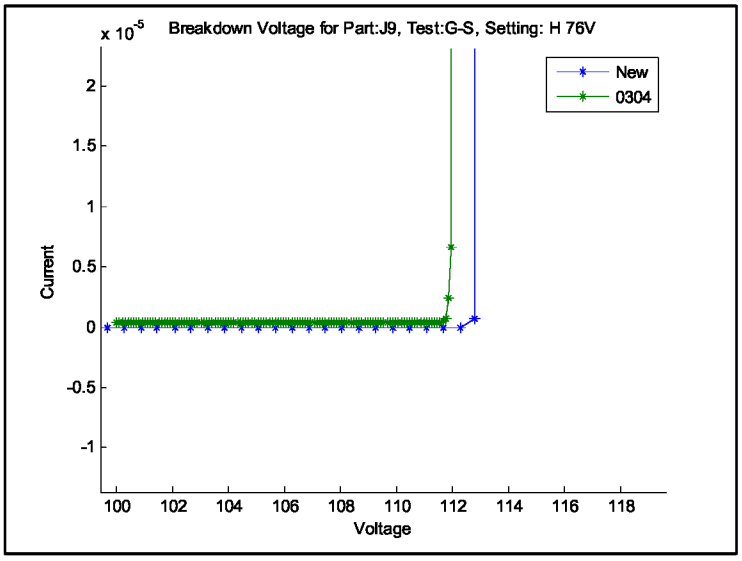


Figure 14: Breakdown Voltage plot for Device J9, G-S injection at high voltage setting (76V). New device is compared to same device after pin-injecting 20 consecutive strokes (Test File Number 0304).

5.2 Leakage Current

The drain-to-source Leakage Current (I_{DSS}) is the current flowing from drain-to-source as the gate is shorted with the source (no gate bias V_{GS}= 0V). Gate and source are connected to the negative connector of the SMU which is the ground and the drain is connected to the positive connector (see Figure 13). The Leakage Current is a parameter indicated in the specifications of the device. For the IRF520Npbf MOSFET the drain-to-source Leakage Current (I_{DSS}) specifications are: a) max I_{DSS}= 25uA for V_{DS}= 100V and V_{GS}= 0V at room temperature; and b) max I_{DSS}= 250uA for V_{DS}= 88V, V_{GS}= 0V, and T_J= 150°C[11].

The measurements are controlled via LabView in order to obtain a sweep of voltages from 0 to the vicinity of the Breakdown Voltage and to limit the test if the current sourced becomes much greater than the maximum specifications. This will avoid incurring any damage on the device during the test. The test performed on these devices consists on a voltage sweep from 0V to 120V which is stopped if the current is larger than 25uA.

Figure 15 shows the results of the test performed on Device J9. It can be observed that there is an increase in the Leakage Current due the lightning injection. Even though the device still conforms to the datasheet rating, it is evident that there is damage resulting from the repeated lightning strokes.

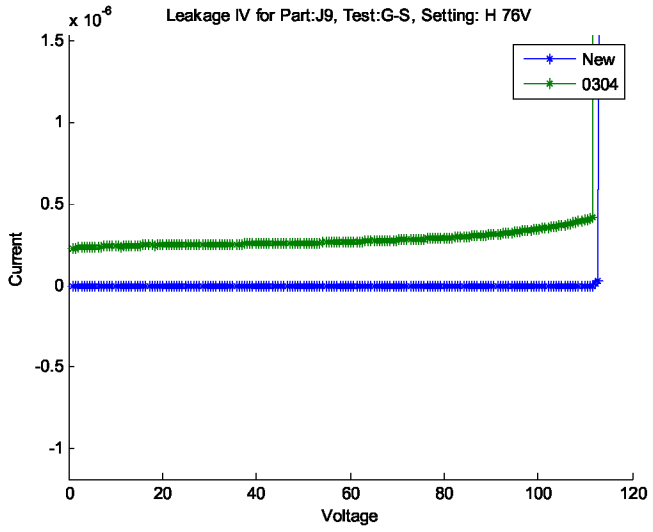


Figure 15: Drain-to-source Leakage Current plot for Device J9, G-S injection at high voltage setting (76V). New device is compared to same device after pin-injecting 20 consecutive strokes (Test File Number 0304).

5.3 Threshold Voltage

Gate Threshold Voltage ($V_{GS(th)}$) refers to the minimum voltage required to bias the gate in order for the device to switch ON and allow I_D current to flow. This parameter is likely to change due to damage in the gate of the device. The SMU equipment can be used to measure these parameters by providing a voltage sweep at V_{GS} until reaching the point where I_D starts growing exponentially. Figure 16 shows the test configuration for Threshold Voltage measurement using the SMU.

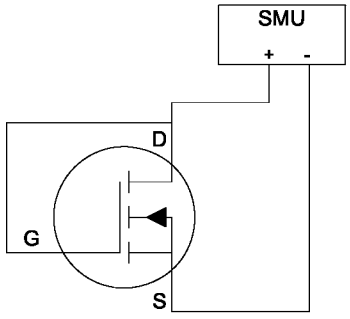


Figure 16: Configuration of Threshold Voltage tests for an n-type power MOSFET.

The threshold voltage rating for IRF520NPbF indicates a minimum Threshold Voltage $V_{GS(th)}$= 2V and a maximum of $V_{GS(th)}$= 4V with V_{GS}= V_{DS} and I_D= 250uA. Figure 17 shows Threshold Voltage results for Device J9. It can be observed that the lightning pin-injection resulted in a shift on the Threshold Voltage by a few hundred mV, which means that the device requires a lower bias voltage to switch ON. This change is an indication of damage on the gate, though the device still complies with the rating specified in the datasheet.

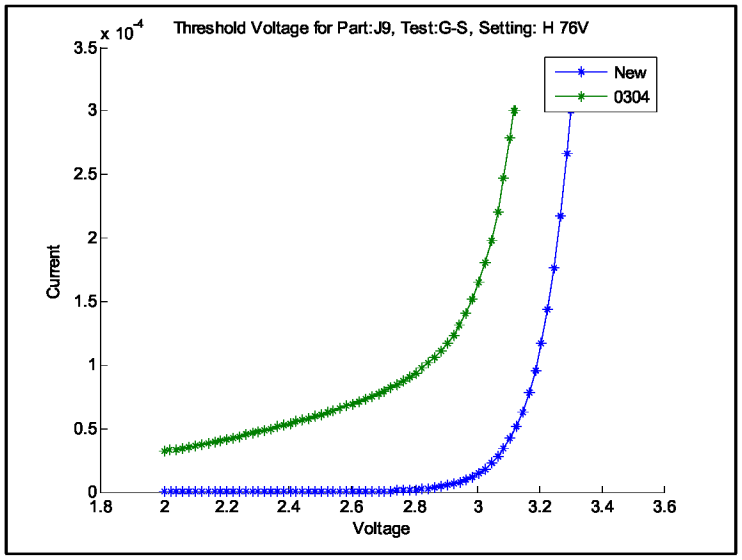


Figure 17: Threshold Voltage plot for Device J9, G-S injection at high voltage setting (76V). New device is compared to same device after pin-injecting 20 consecutive strokes (Test File Number 0304).

6 Conclusions

NASA Ames Prognosis Center of Excellence and NASA LaRC IVHM HIRF Laboratory researchers tested a set of 400 identical MOSFETs by pin-injecting standard lightning waveforms to induce fault modes and to degrade performance. Pre-Tests identified Fail Levels for each pin configuration (i.e. Gate-Source, Gate-Drain, and Drain-Source). The Test Level was then reduced to levels below the Fail Level, and the MOSFET subjected to multiple strokes. "High" Test Level defined as highest possible 20-strokes test-level without damage. "Medium"= 0.9 x "High". "Low"= 0.8 x "High". Lightning waveform voltages up to 1700V, and currents up to 1460A, were applied to various MOSFET pin configurations. Safety Hazards and Precautions were identified by the research team before testing, and all test personnel participated in a safety briefing. MOSFETS were evaluated using the NASA Ames Aging and Characterization Platform for semiconductor components.

Table 10 shows test levels required to cause IRF520NPBF MOSFET failure, when using different lightning waveforms. The IRF520NPBF was selected to be representative of devices that may be present in DC-DC power supplies and electromechanical actuator circuits that may be used on board aircraft. Comparing these levels with the DO-160E representative environments shown in Table 1, it may be seen

that MOSFET Gates are susceptible to failure, even when installed in systems in well-shielded and partial-shielded locations. MOSFET Drains and Sources are significantly less susceptible, but are likely to be prone to failure when installed in partial-exposed to fully-exposed locations. These fail levels assume that transient suppression circuitry has not been added to the IRF520NPBF terminals.

Most tests focused on Lightning Waveform #4. Some testing was also performed using Waveforms #3, 5A and 5B. Results show that device impedance decreased (current *increased*) after every failure. (See Figures 7 through 11.) Such a failure mode may lead to cascading failures, as the damaged MOSFET may allow excessive current to flow through other circuitry.

Preliminary assessments on a MOSFET subjected to 20-stroke pin-injection testing demonstrate that Breakdown Voltage, Leakage Current and Threshold Voltage characteristics show damage, while the device continues to meet manufacturer performance specifications. Ames researchers are continuing to evaluate the MOSFETS to determine the effects of lightning on device-aging characteristics.

Testing of additional MOSFET devices in the ON state was later conducted in the Langley HIRF Facility May 4 to 15, 2009. Results from the May tests will be provided in a subsequent report. Possible follow-on investigations may include tests where the MOSFET is driving a motor, or testing of IGBTs.

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14. ABSTRACT

Lightning transients were pin-injected into metal-oxide-semiconductor field-effect transistors (MOSFETs) to induce fault modes. This report documents the test process and results, and provides a basis for subsequent lightning tests. MOSFETs may be present in DC-DC power supplies and electromechanical actuator circuits that may be used on board aircraft. Results show that unprotected MOSFET Gates are susceptible to failure, even when installed in systems in well-shielded and partial-shielded locations. MOSFET Drains and Sources are significantly less susceptible. Device impedance decreased (current increased) after every failure. Such a failure mode may lead to cascading failures, as the damaged MOSFET may allow excessive current to flow through other circuitry. Preliminary assessments on a MOSFET subjected to 20-stroke pin-injection testing demonstrate that Breakdown Voltage, Leakage Current and Threshold Voltage characteristics show damage, while the device continues to meet manufacturer performance specifications. The purpose of this research is to develop validated tools, technologies, and techniques for automated detection, diagnosis and prognosis that enable mitigation of adverse events during flight, such as from lightning transients; and to understand the interplay between lightning-induced surges and aging (i.e. humidity, vibration thermal stress, etc.) on component degradation.

15. SUBJECT TERMS
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