Abstract

Emerging and next-generation test instrumentation needs increasingly demand network communication to manage complex and dynamic test scenarios. Adapting wireless communication infrastructure to accommodate challenging testing needs can benefit from reconfigurable radio technology. A fundamental requirement for a software-definable radio system is independence from carrier frequencies, one of the radio components that to date has seen only limited progress toward programmability. This paper overviews a project to validate the viability of a promising chipset that digitizes RF and performs direct down-conversion of the wireless signal to its baseband equivalent. As programmable components mature, field of software defined radio pursues the promises of completely programmable radios that are independent from the hardware on which they are implemented. The Software Configurable Multichannel Transceiver enables four transmitters and four receivers in a single unit, programmable for any frequency band between 500 MHz and 6 GHz.

Software Configurable Multichannel Transceiver

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Abstract

Emerging test instrumentation and test scenarios increasingly require network communication to manage complexity. Adapting wireless communication infrastructure to accommodate challenging testing needs can benefit from reconfigurable radio technology. A fundamental requirement for a software-definable radio system is independence from carrier frequencies, one of the radio components that to date has seen only limited progress toward programmability. This paper overviews an ongoing project to validate the viability of a promising chipset that performs conversion of radio frequency (RF) signals directly into digital data for the wireless receiver and, for the transmitter, converts digital data into RF signals. The Software Configurable Multichannel Transceiver (SCMT) enables four transmitters and four receivers in a single unit the size of a commodity disk drive, programmable for any frequency band between 1 MHz and 6 GHz.

Keywords: *Software-defined radio, reconfigurable computing, cognitive radio, unmanned systems*

Introduction

Vehicle systems studied by the test and evaluation communities are quickly growing in complexity, and these systems are in turn expected to perform within increasingly complex scenarios. Different types of unmanned and autonomous systems must cooperate and converse with each other and with humans in dispersed geographical settings. Information flows in many directions simultaneously, for different reasons, with different sets of requirements. Communications involving command and control, information upload and download, and monitoring for safety or health necessarily includes multiple data communication technologies and approaches. Effectively studying the behavior of a few or just one of the systems within a dynamically changing complex system of systems is challenging.

Effective and affordable test infrastructure solutions to these challenges demand a capability for communication systems to adapt on demand to the frequencies and protocols needed for a particular task. In this paper we therefore describe a project to develop a dynamically reconfigurable transceiver system – i.e., a software-defined radio

(SDR) - that is agile across most, if not all, frequencies and modulation protocols of interest to the test and evaluation communities.

Background

The Software Defined Radio (SDR) Forum defines an ideal software radio as one in which programmability extends to the entire system, with analog conversion occurring only at the antenna and (if present) speaker and microphone. Heterodyne mixing and analog signal amplification are eliminated in an ideal software radio.[1]

In 2007 a new programmable chipset referred to as True Software Radio® (TSR) became available. Implemented with 0.18 micron SiGE technology, this patented integrated circuit contains an advanced delta-sigma architecture that converts RF signals directly into digital data for the wireless receiver and directly from digital data into radio signals for the transmitter. TSR chips replace the analog front end, intermediate frequency (IF) processing, analog-to-digital conversion (ADC), and digital filtering sections of today's conventional wireless transmitters and receivers. Elimination of analog circuitry implies that frequency-agile radios can be created. Figure 1 compares a traditional approach to radios to the TSR approach

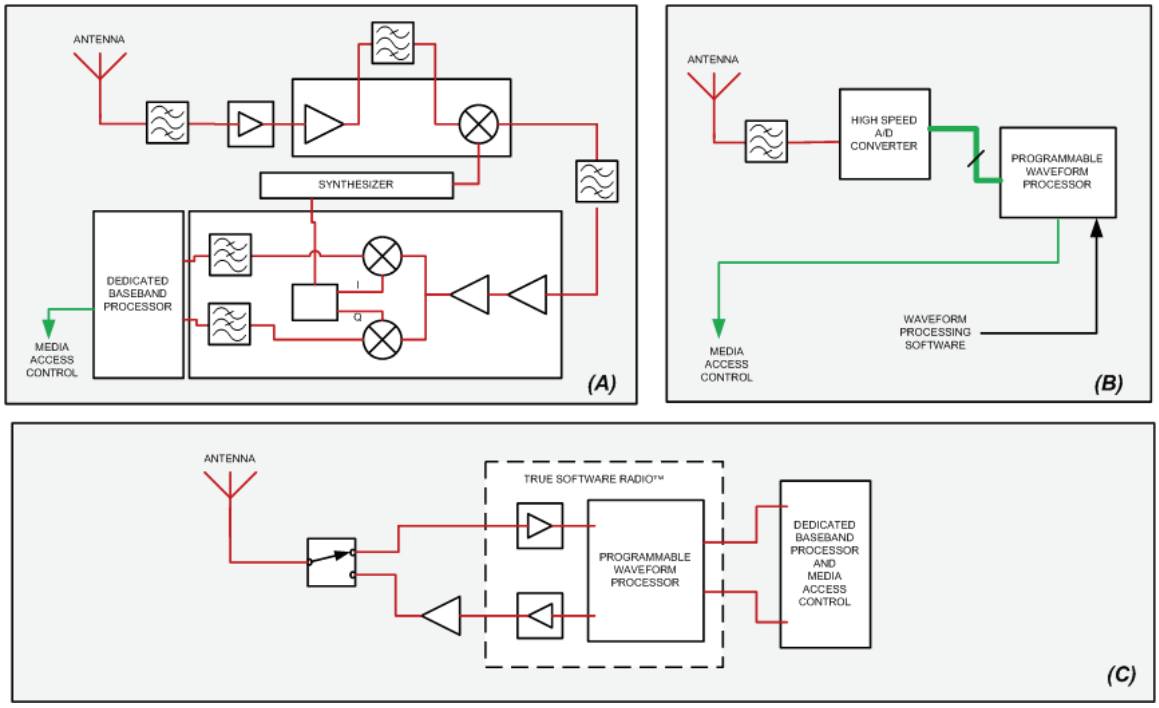

Figure 1. Comparison of conventional radio receiver *(A)* with True Software Radio receiver *(B)*. The transceiver approach *(C)* is the notional building block of the current multichannel transceiver.

[1] http://www.sdrforum.org/pages/aboutTheForum/faqs.asp.

An informal study of the performance of the TSR receiver using existing evaluation boards revealed that the frequency agility and programmable nature of the chipset functioned as advertised. Two examples from that study are shown in Figure 2.

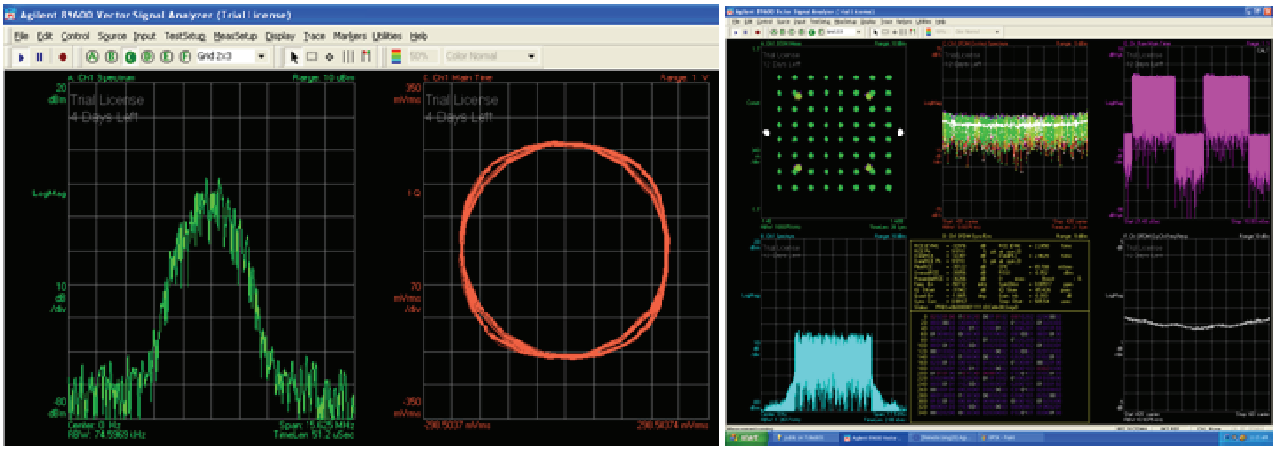

Figure 2. Excerpts from preliminary study of TSR chipset performance. The left figure shows a received SOQPSK spectrum and constellation for a 5 Mbps PRN-15 BERT. The figure on the right shows a WiMAX signal as received from a TSR transmitter. Data analyzed with Agilent VSA software. *(Credit: Hal Cornelius)*

Recognizing the potential value of this technology to support development of new communications solutions of interest to the test and evaluation (T&E) communities, a small group of individuals representing NASA and DoD interests advocated for support to design and build a prototype system containing four transceivers. Four transceivers in one system was deemed a reasonable balance between capabilities and engineering simplicity as would be required to support technical evaluation and assessments for various production applications. A four-channel transceiver was complicated enough to enable engineers to consider sophisticated applications yet conservative enough to be achievable without violating notional size, power, weight, and cost constraints.

Project Goals and Objectives

The following objectives were established for the project:

- Develop and build a four-channel transceiver based on existing TSR™ chipsets. The initial vision of the project was to deliver this transceiver, if possible, in a reasonably small form factor such as PC/104 or CompactPCI (CPCI)
- Develop or acquire, and integrate software and firmware as necessary to program the transceiver to operate with several different protocols and waveforms in several different frequency bands
- Develop a "tabletop" concept demonstration underscoring the frequency agility and waveform flexibility of TSR™ technology
- Demonstrate interoperation of two or three transceivers in parallel
- Leverage the experience gained to develop a road map for technology enhancements in support of the needs of test and evaluation communities.

Table one offers a traceability of key specifications to overall T&E needs.

Table 1. Traceability of Specifications to Test and Evaluation Needs.

Test and Evaluation Needs	Relevant Specifications
Flexible multi-band command and control communications system to support data capture during complex multi-agent test scenarios that include unique test aspects of UAS communications	Wide bandwidth coverage – 1 MHz to 6 GHz Multiple receivers and transmitters Rapid reprogrammability of frequency and protocol.
Range Safety (ability to terminate any systems operation)	Command and control channel for range safety that all UAS systems can receive or able to retransmit to other UAS systems.
Multi-Vehicle Scripted Testing	Transceivers can be programmed to communicate with any other vehicle, sharing information, intelligence, status and range commands.

While this project potentially closes important technology gaps in software radios, actual applications of this technology remain outside the scope of this project. Three basic tasks defined the project activities:

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(1) *Design and construct a four-transceiver system based upon existing TSR™ chips and technology*. In order to facilitate as much parallel development (between hardware and software/firmware) as possible within the project, a hardware structure will be adopted that will enable testing of software/firmware on existing transmitter and receiver evaluation board designs and "ported" to the prototype design when the appropriate hardware is ready.

(2) *Integrate software and firmware to implement waveforms of interest to DoD and NASA at frequencies of interest*. These are representative waveforms and frequencies of interest to the test and evaluation communities, with emphasis on the needs of the uninhabited autonomous systems testing. Since software development for specific applications is a task that future users of the system would focus on, our task here is to demonstrate capabilities via leveraging existing work where possible. Waveforms of interest include but are not limited to FM, SOQPSK, WCDMA, OFDM, and AOFDM. Likely candidates for frequencies are 520 MHz, 1700 MHz, 2250 MHz, and 5100 MHz spectral bands. The 5100 MHz region is the new spectral band allocation approved in November 2007 at the World Radiocommunication Conference for "harmonized" worldwide

aeronautical telemetry. Pseudorandom noise and spread channel solutions are possible but implementation is outside the scope of this project.

(3) *Develop a demonstration that illustrates the key characteristics of TSR™ technology that make it appropriate for use in software-configurable multi-channel radios*. The simplest task is simply to configure one transceiver to operate independently from the others. Additional tests would be required to validate essential functions. These essential functions support applications such as store-and-forward, translation from one frequency/modulation channel to another, and coordinated actions. Coordinated behavior, if it involved scanning and adaptation based on the RF environment itself, would demonstrate the fundamental capability required to build beamformers, phased arrays, and cognitive radios.

In order to communicate the results of this work and support timely identification and prioritization of follow-on activities, an e-mail list "advisory board" consisting of representatives from academia, industry, and government was implemented.

System Architecture and Design

An existing set of transmitter and receiver evaluation boards offered a starting point for the SCMT radio design effort. These evaluation boards were designed as simple "electronic project" boards to showcase the operation of the chipset. Analysis of these boards identified aspects of the design that would require the most effort:

- The original evaluation board did not make provisions for the front-end circuitry necessary to interface with an antenna. Furthermore, the first generation chipset only has an abbreviated front end, which would be inadequate for direct interface with an antenna or band selection circuitry.
- The four-transceiver design requires a new approach to processing. In the original evaluation board design, each transmitter chip and each receiver chip fed a set of FPGA chips that were dedicated to processing the A/D and D/A signal I/Os. This approach is unacceptably inefficient in allocating processing resources.
- The interface to and from the four-channel transceiver must be compatible with equipment that will be encountered in the target applications.
- The AB version of the chipset is desired, but proper characterization of the AB chips requires effort and time that may be outside the schedule constraints. The AB version is functionally identical to the engineering validation version AA but contains improvements in certain chipset specifications.

The design that emerged addresses these challenges and has the following features:

- Four independently addressable transceiver "daughterboards." These include the RF circuitry, and some on-board FPGA processing.
- A baseband motherboard that exchanges commands and data with the four "daughterboards." Between the motherboard and "daughterboards" the system permits maximum flexibility on how the processing firmware is partitioned. For

simple waveforms such as SOQPSK or FM, the physical layer firmware can remain resident on the "daughterboard." For more complex waveforms such as COFDM, most or all of the firmware can be resident on the motherboard.

- A shielded case that provides the maximum possible isolation between each of the transceiver "daughterboards." With this approach, the user can determine whether a single antenna is shared between the four transceivers or individual antennas are used.
- An interconnection strategy to connect multiple four-channel transceiver units into larger arrays. This approach should enable transceivers to be addressed in local or global groups.
- Design details that permit transmitter and receiver daughterboards to be interchangeable. Thus, the four-channel transceiver unit could, if desired for a particular application, be an eight-channel receiver.

The physical dimensions of the shielded case initially converged on a package roughly the size of a 5.25 inch "low profile" disk drive (5.75 in × 1.0 in × 8 in). This preliminary design is illustrated in Figure 3. Inspection of the figure reveals two baseband processing boards sandwiched in between upper and lower assemblies of RF boards.

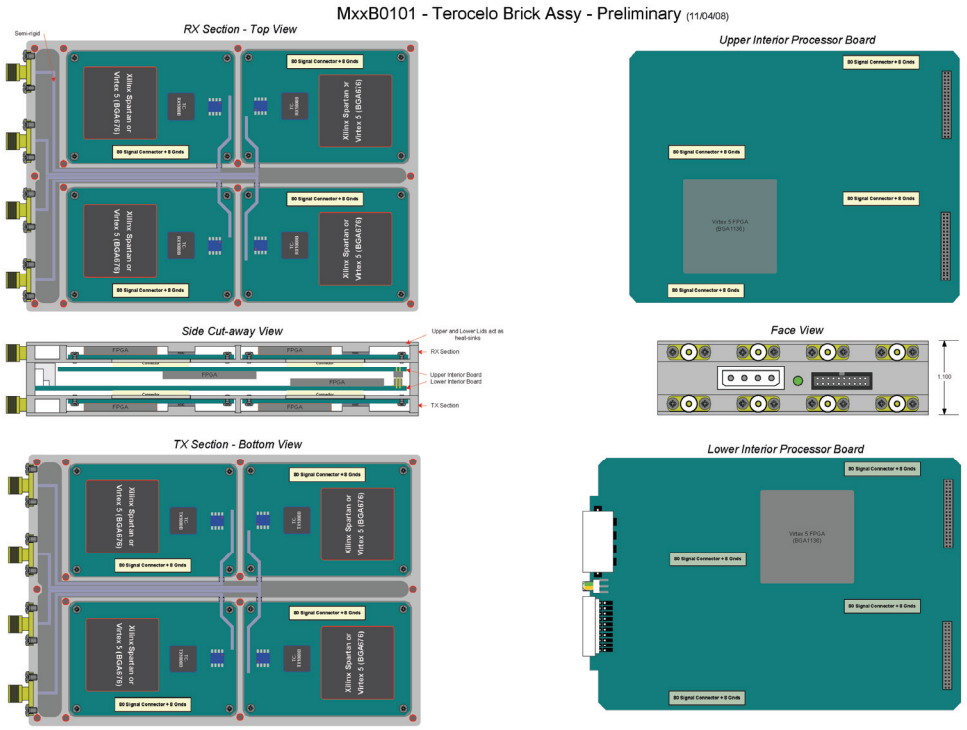

Figure 3. Preliminary design of four-transceiver SCMT system.

A key drawback of this preliminary design was quickly realized. Specifically, it is by design an all-digital radio that may in fact be programmable but has limited options for interfacing with existing equipment. This makes it challenging to test the frequency-agile

RF components independent from the baseband processing and makes it difficult to integrate this radio with existing technology. An innovation was introduced in the final design that mitigates this problem. Ironically, the innovation is to introduce a 70 MHz intermediate frequency (IF) signal as a standard analog interface. By bringing this analog signal outside the unit, testing with proven third-party digital receivers becomes straightforward.

Figure 4 illustrates the final design that accommodates the additional signal interfaces. The unit shown (5.75 in × 0.9 in × 7.0 in) only has four RF boards, but two of these units stacked together create a system that is still within the dimension constraints of a standard disk drive. A photograph of the unit as constructed is shown in Figure 5.

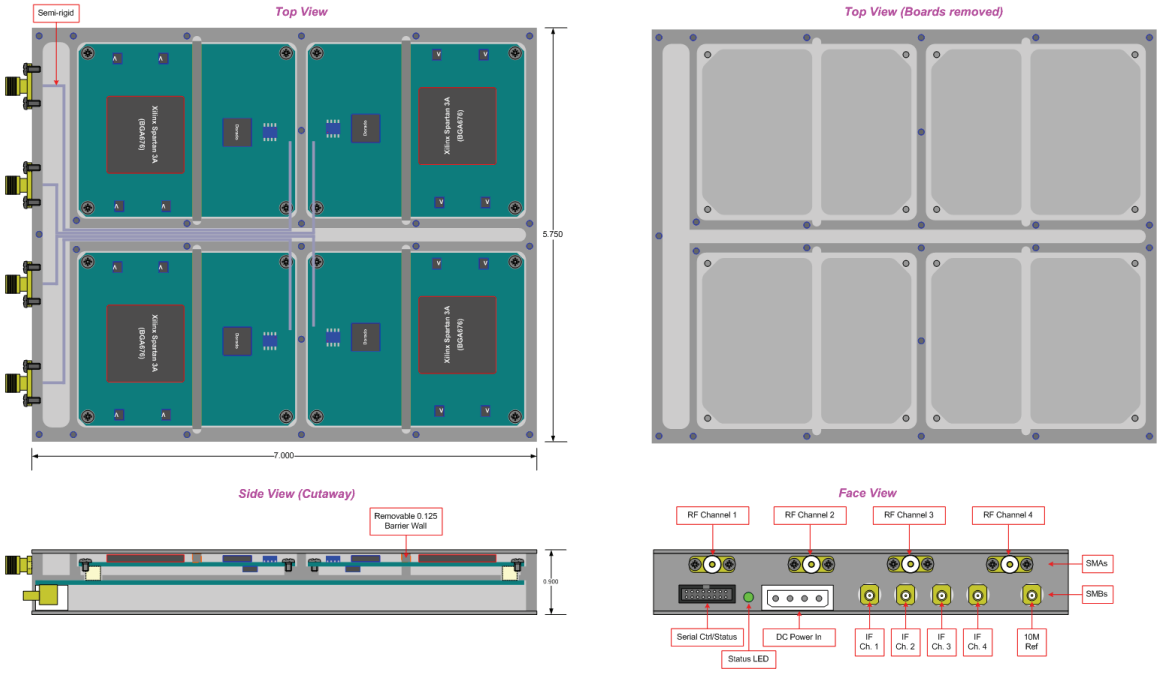

Figure 4. Final design of SCMT system showing half of the transceivers with intermediate frequency and reference clock outputs. Each RF module is 2.4 in by 3.0 in. The TSR chip is the small 1cm^2 chip, while the larger chip is an FPGA.

Figure 5. Photo of the SCMT prototype as used for testing. The final four-transceiver system is comprised of two of these units. (NASA photo ED09-0086-10).

The system architecture is depicted in Figure 6.

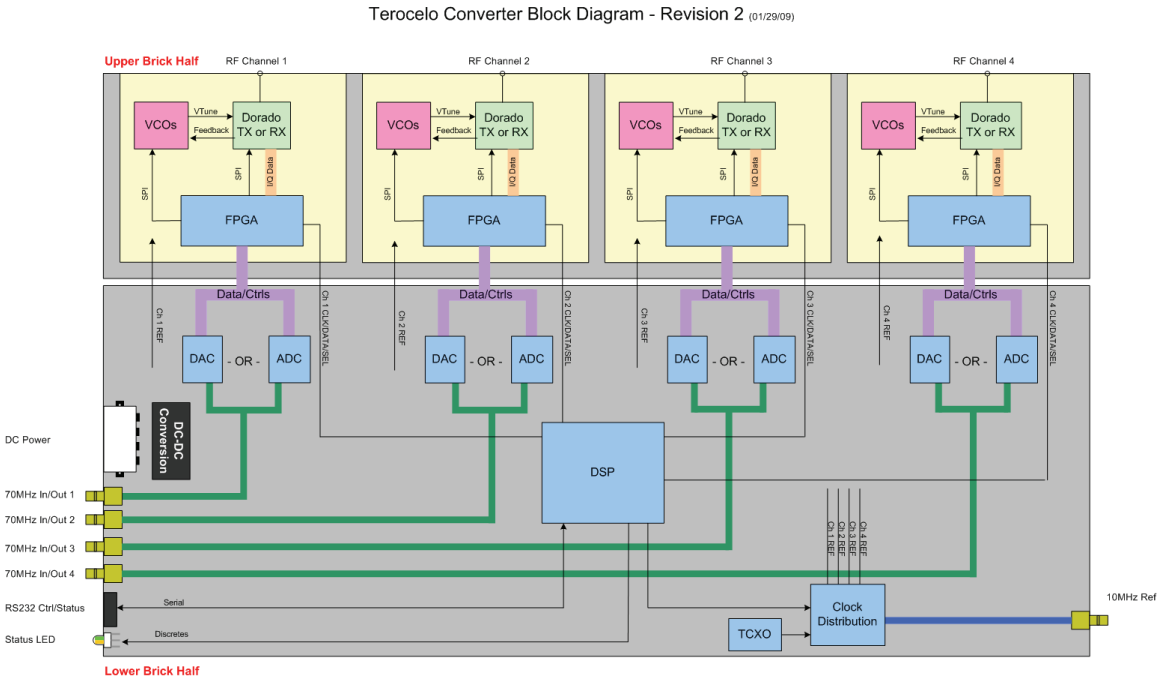

Figure 6. System architecture of the SCMT module. An upper brick half containing four RF modules is connected to a lower brick half containing a DSP and routing IF signals to and from external processing. The four-transceiver SCMT is comprised of two of these modules.

Project Status and Discussion

The design as shown is currently being assembled using the AA chipset, thus, formal system testing has not yet begun. The following test procedures will be taken after the initial tests of the demonstration modules have been performed. The tests will show the control, programmability and functionality of the SCMT transceiver.

- The RF section of the SCMT transceiver consists of four independent receive and four independent transmit channels. Each channel has its own FPGA.

- The Base band section of the SCMT for this project will be a standard product from Lumistar. It contains the FPGA resources and code to demodulate the SCMT RF channel I/Q output.

- In order to demodulate the RF board digital I/Q output it was necessary to convert the output to 70 MHz analog. This would allow the use of existing demodulation code.

- The tests will be conducted in a way that will verify the operation of the SCMT in all modes of operation.

Test modes

1. Power supply tests
2. Test equipment verification tests
3. RF boards tests
4. Baseband processing board tests
5. Software setup tests
6. RF display tests
7. CW modulation tests
8. TIER modulation tests and verification
9. BERT modulation tests
10. BERT reception test
11. Frequency setup test
12. Transmitter verification test
13. Transmitter frequency selection test
14. BERT transmit and reception tests
15. Channel selection test
16. RF level tests
17. Adjacent channel interference tests
18. Noise level tests.

Because the project lacked funding and schedule to implement fully-integrated baseband hardware, certain features for production units deemed necessary such as network stacks and wired network interfaces have not yet materialized.

Future Work

This project will conclude after testing and demonstration is completed in the coming months. A relatively large number of follow-on applications have been identified and are being pursued.

Concluding Comments

The SCMT phase I product is a prototype device that is in some ways less than the engineering team had hoped for due to cost and schedule constraints, yet much more useful than the notional design with which we started. As constructed, it is a four-transceiver system that leverages IF channel interfaces to communicate with and leverage existing external third-party receivers and other equipment. Future systems would incorporate an internal baseband processing board, but there are already a number of near-term ground and flight applications envisioned that leverage the IF interface in order to introduce frequency agility to existing products. Based on enthusiastic responses for these follow-on applications, we believe SCMT and its derivatives will have a significant impact on the evolution of telemetry and network communications used for test and evaluation.

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