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Customizable Digital Receivers for Radar

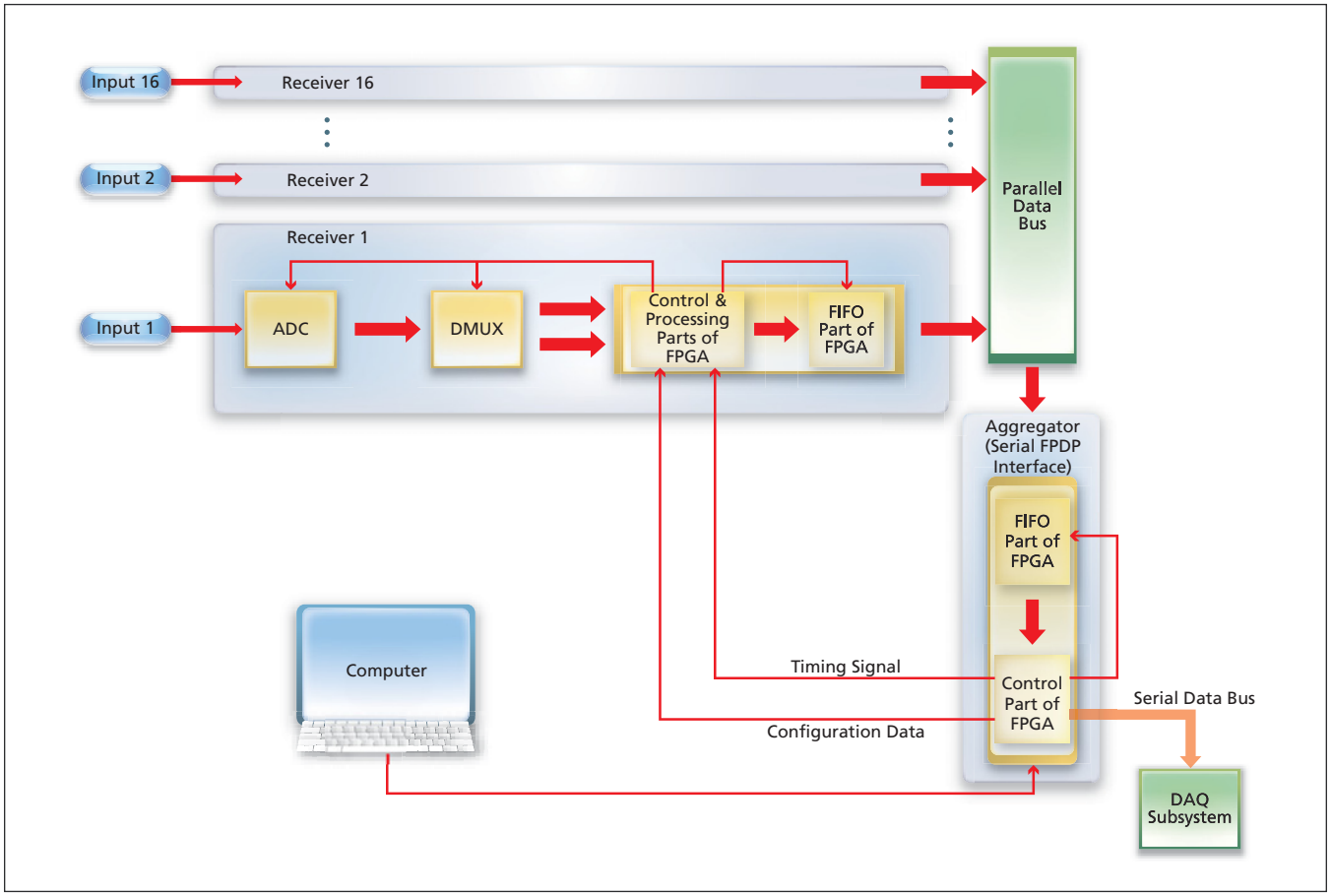
These receivers are unusually compact and versatile.

NASA's Jet Propulsion Laboratory, Pasadena, California

Compact, highly customizable digital receivers are being developed for the system described in "Radar Interferometer for Topographic Mapping of Glaciers and Ice Sheets" (NPO-43962), *NASA Tech Briefs*, Vol. 31, No. 7 (August 2007), page 72. In the original intended application, there is a requirement for 16 such receivers, each dedicated to, and mounted directly on, one antenna element in a 16-element array. The receivers are required to operate in unison, sampling radar returns received by the antenna elements in a digital beam-forming (DBF) mode. The design of these receivers could also be adapted to commercial radar systems. At the time of reporting the information for this article, there were no commercially available digital receivers capable of satisfying all of the operational requirements and compact enough to be mounted directly on the antenna elements.

The figure depicts the overall system of which the digital receivers are parts. Each digital receiver includes an analog-to-digital converter (ADC), a demultiplexer (DMUX), and a field-programmable gate array (FPGA). The ADC effects 10-bit band-pass sampling of input signals having frequencies up to 3.5 GHz. (In the original intended application, the input signals would be intermediate-frequency signals obtained through down-conversion of signals from a radio frequency of several tens of gigahertz.) The input samples are demultiplexed at a user-selectable rate of 1:2 or 1:4, then buffered in part of the FPGA that functions as a first-in/first-out (FIFO) memory. Another part of the FPGA serves as a controller for the ADC, DMUX, and FIFO memory and as an interface between (1) the rest of the receiver and (2) a front-panel data port (FPDP) bus, which is an industry-standard parallel data bus that has a high-data-rate capability and multichannel configuration suitable for DBF.

Still other parts of the FPGA in each receiver perform signal-processing functions. The design exploits the capability of FPGAs to perform high-speed processing and their amenability to customization. There is ample space available within the FPGA to customize it to



Digital Receivers in an array sample and preprocess input signals from antenna elements. The receiver outputs are coupled in turn onto the parallel data bus.

implement such application-specific, real-time processes as digital filtering and data compression. To afford additional operational flexibility and to enable use of a receiver in other applications, the design also includes a provision for an additional "drop-in" circuit board containing analog amplification and filtering circuitry. Such boards, which are relatively simple and inexpensive, can be easily exchanged by the user to modify center-frequency, bandwidth, and signal-level parameters.

The digital receivers can be configured to operate in a stand-alone mode, or in a multichannel mode as needed for DBF. In the multichannel/DBF mode, the receivers are made to take turns in transmitting sampled data onto the bus. The bus port on each receiver adheres to the FPDP-II standard, which supports an aggregate data rate of 400 MB/s. While the primary role of the FPDP bus is to transmit sampled data from receivers to a data-storage unit, the bus can also be used to transmit configuration data to the receivers. The bus also enables the receivers to communicate with one another — a capability that could be useful in some applications. Each receiver is also equipped with an RS-232 interface, through which configuration data can be communicated.

The data on the bus are aggregated and then sent to a data-acquisition (DAQ) subsystem by means of a serial FPDP interface that, like each receiver, contains an FPGA that serves partly as a FIFO memory and partly as a control unit. The DAQ subsystem stores the data onto a hard-disk array for postprocessing. In its role as a control unit, this FPGA sends timing and configuration information to each of the 16 receivers.

Although band-pass sampling is a widely applied technique, heretofore, it has been little used in radar systems. The use of band-bass sampling in the present receiver design is what makes it possible to achieve compactness: Band-pass sampling makes it possible to feed, as input to the ADC, signals having higher frequencies than could otherwise be utilized. In so doing, band-pass sampling enables elimination of an additional down-conversion stage that would otherwise be needed, thereby reducing the design size of the receiver. This design approach also eases filtering constraints and, in so doing, reduces the required sizes of filters.

The customizability of the receiver makes it applicable to a broad range of system architectures. The capability for operation of receivers in either a stand-alone or a DBF mode enables the use of the receivers in an unprecedentedly wide variety of radar systems.

This work was done by Delwyn Moller, Brandon Heavey, and Gregory Sadowy of Caltech for NASA's Jet Propulsion Laboratory. For more information, contact iaoffice@jpl.nasa.gov. NPO-45539

Two-Camera Acquisition and Tracking of a Flying Target

An unanticipated moving target can be automatically spotted and tracked.

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A method and apparatus have been developed to solve the problem of automated acquisition and tracking, from a location on the ground, of a luminous moving target in the sky. The method involves the use of two electronic cameras: (1) a stationary camera having a wide field of view, positioned and oriented to image the entire sky; and (2) a camera that has a much narrower field of view (a few degrees wide) and is mounted on a two-axis gimbal. The wide-field-of-view stationary camera is used to initially identify the target against the background sky. So that the approximate position of the target can be determined, pixel locations on the image-detector plane in the stationary camera are calibrated with respect to azimuth and elevation. The approximate target position is used to initially aim the gimballed narrow-field-of-view camera in the approximate direction of the target. Next, the narrow-field-of view camera locks onto the target image, and thereafter the gimbals are actuated as needed to maintain lock and thereby track the target with precision greater than that attainable by use of the stationary camera.

Figure 1 shows a prototype of the apparatus. The stationary, wide-field-of-view camera includes a fish-eye lens that projects a full view of the sky (the full 360° of azimuth and the full 90° of elevation) onto a 512×512-pixel image detector of the active-pixel-sensor type. The gimballed narrow-field-of-view camera contains a charge-coupled-device (CCD) image detector. The apparatus also includes circuitry that digitizes the image-detector outputs and a computer that processes the image data and generates gimbal-control commands.

The stationary, wide-field-of-view camera repeatedly takes pictures of the sky. In processing of the image data for each successive frame period, the immediately preceding frame is subtracted from the current frame, so that all that remains in the image is what has changed between the two successive frames. Hence, if there is a moving luminous target, it

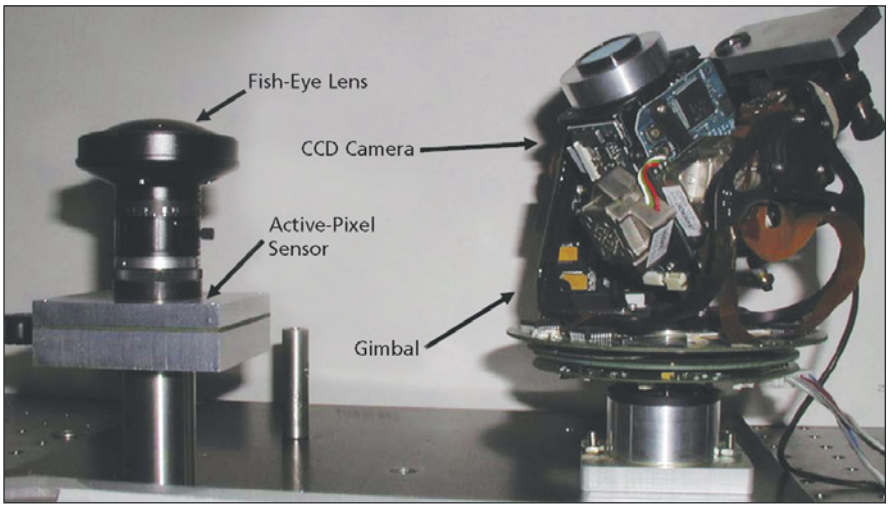

Figure 1. This **Prototype Apparatus** was built and tested, yielding the images shown in Figure 2.