

or lower trip-curve values to protect circuits during initial testing, and to set a default higher trip current during subsequent pre-launch and launch operations.

In the open state of the circuit breaker, one of the circuit-testing subsystems could obtain electrical-resistance readings on the load side as indications of whether faults are present, prior to switching the circuit breaker closed. Should a fault be detected, another circuit-testing subsystem could perform time-domain reflectometry, which would be helpful in locating the fault. On the power-line side, still another circuit-testing subsystem could take a voltage reading, as an indication

of whether the proper voltage is present, prior to switching the circuit breaker closed.

The system would be contained in a housing, with input, output, and data/control connectors on the rear surface. All monitoring, control, and programming functions would ordinarily be performed from a remote console. On the front surface, there would be a push-button switch for optionally locally setting the circuit breaker in the open or closed state, plus a lamp that would provide a local visual indication of whether the circuit breaker was in the open (initially set), closed, or open (tripped) state.

The aforementioned monitoring, testing, state-setting, and trip-current-setting functions would be effected by circuitry on an integrated-circuit card inside the housing. Also on the card would be (1) input and output circuitry for remote monitoring and control and (2) a tag random-access memory as an electronic means of identifying the system by serial number, location, a reference designation, and operational characteristics.

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## Electronic Switch Arrays for Managing Microbattery Arrays

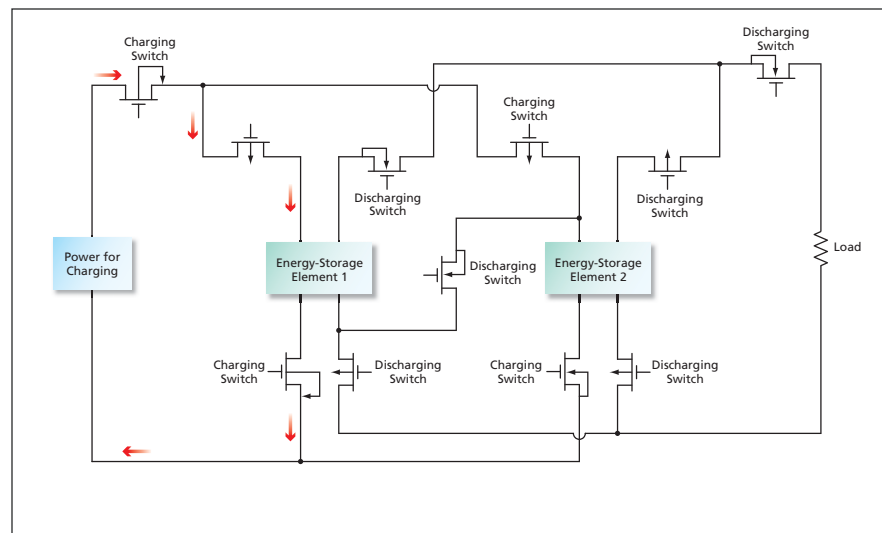
Array circuitry is dynamically configured to optimize performance and disconnect defective elements.

NASA's Jet Propulsion Laboratory, Pasadena, California

Integrated circuits have been invented for managing the charging and discharging of such advanced miniature energy-storage devices as planar arrays of microscopic energy-storage elements [typically, microscopic electrochemical cells (microbatteries) or microcapacitors]. The architecture of these circuits enables implementation of the following energy-management options:

- Dynamic configuration of the elements of an array into a series or parallel combination of banks (subarrays), each array comprising a series or parallel combination of elements;
- Direct addressing of individual banks for charging and/or discharging; and
- Disconnection of defective elements and corresponding reconfiguration of the rest of the array to utilize the remaining functional elements to obtain the desired voltage and current performance.

One of the reasons for fabricating microbattery and microcapacitor arrays is that the array form affords partial immunity to defects in individual energy-storage elements. Defective energy-storage elements act as loads on the functional ones, thereby reducing the capacity of an overall array. By enabling the disconnection of defective elements and reconfiguration of the rest of the array, the present invention offers practical means to realize this partial immunity. In addition, the invention provides for interrogating individual cells and banks in the



**Two Energy-Storage Elements** can be connected, individually or together in series or parallel, to the power source or the load by closing or opening the appropriate subset of switching transistors. This example has been greatly oversimplified for the sake of illustrating the basic principle; a typical practical circuit would contain many more energy-storage elements and switches.

array and charging them at the current-vs.-time or voltage-vs.-time characteristics needed for maximizing the life of the array.

An integrated circuit according to the invention consists partly of a planar array of field-effect transistors that function as switches for routing electric power among the energy-storage elements, the power source, and the load (see figure). To connect the energy-storage elements to the power source for charging, a specific subset of switches is closed; to connect the energy-storage el-

ements to the load for discharging, a different specific set of switches is closed.

Also included in the integrated circuit, but omitted from the figure for the sake of simplicity, is circuitry for monitoring and controlling charging and discharging. The control and monitoring circuitry, the switching transistors, and interconnecting metal lines are laid out on the integrated-circuit chip in a pattern that registers with the array of energy-storage elements. There is a design option to either (1) fabricate the energy-storage elements in the cor-

responding locations on, and as an integral part of, this integrated circuit; or (2) following a flip-chip approach, fabricate the array of energy-storage elements on a separate integrated-circuit chip and then align and bond the two chips together.

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*In accordance with Public Law 96-517, the contractor has elected to retain title to this invention. Inquiries concerning rights for its commercial use should be addressed to:*

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## Lower-Dark-Current, Higher-Blue-Response CMOS Imagers

Semiconductor junctions are relocated away from Si/SiO<sub>2</sub> interfaces.

NASA's Jet Propulsion Laboratory, Pasadena, California

Several improved designs for complementary metal oxide/semiconductor (CMOS) integrated-circuit image detectors have been developed, primarily to reduce dark currents (leakage currents) and secondarily to increase responses to blue light and increase signal-handling capacities, relative to those of prior CMOS imagers. The main conclusion that can be drawn from a study of the causes of dark currents in prior CMOS imagers is that dark currents could be reduced by relocating p/n junctions away from Si/SiO<sub>2</sub> interfaces. In addition to reflecting this conclusion, the improved designs include several other features to counteract dark-current mechanisms and enhance performance.

The left half of the figure illustrates two of the improved designs, in which p-

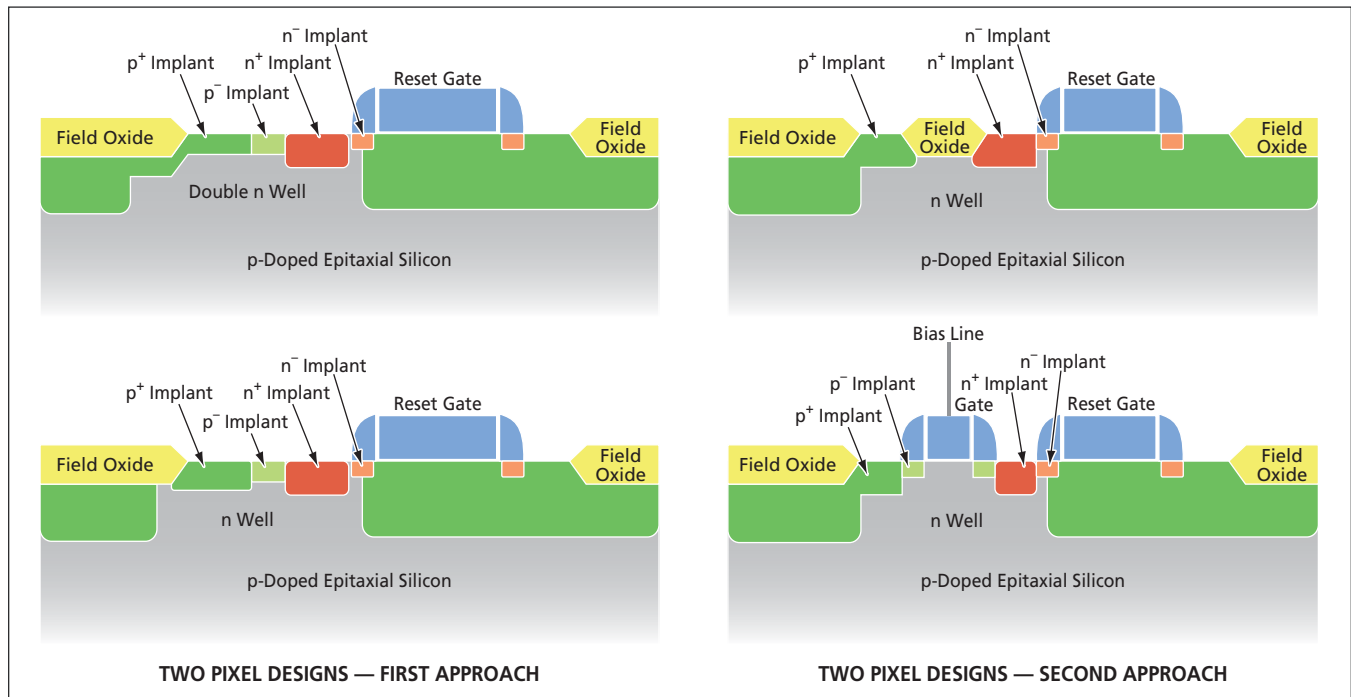
doped implants are added, variously, underneath and/or at the edges of the field oxide regions. These implants hold the Si/SiO<sub>2</sub> interfaces in thermal equilibrium and prevent generation of dark current at the interfaces. In covering the field oxide, the p implants separate the p/n junctions from the Si/SiO<sub>2</sub> interfaces, so that the interfacial component of the dark current (which is the major component) is greatly reduced.

Beyond a certain electric strength, the leakage current depends very strongly on the strength of the electric field. In order to reduce electric fields in the reverse-biased junctions, the p wells are separated from the n wells. A double n well in each pixel is preferred, both for increased photocarrier-collection efficiency and for tailoring the

doping so that the electric field in the transition region between p<sup>+</sup>-to-n-well region is low.

For electrical connections to the photodiodes, which also act as the sources of reset field-effect transistors, n<sup>+</sup> implants are necessary. Unfortunately, the p<sup>+</sup>/n<sup>+</sup> junctions heretofore associated with such implants are undesirable because they contain high electric fields, which give rise to significant tunneling currents, which, in turn, are components of dark currents. In these designs, p-implants are added at the surfaces to tailor the doping from p<sup>+</sup> accumulation layers to n<sup>+</sup> source layers, thereby reducing tunneling currents.

Two of the improved designs illustrated in the right half of the figure follow an alternative approach to tailoring



These Cross Sections of a Pixel in a CMOS imager represent four designs that provide for reduction of dark currents in different ways.