7. The thin top photoresist layer deposited in step 4 is removed.
8. A partly sacrificial layer of gold <0.01 μm thick is deposited to ensure uniform ECD in step 10.
9. A thicker top photoresist layer is deposited and patterned to form a mold for a top interconnection pattern of Ni contact pads.
10. The Ni contact pads, typically 3 μm thick, are electrodeposited in the holes in the mold. The electrodeposition parameters are chosen to keep stresses in the pads low so that the pads do not pull off the thermoelectric legs.
11. In a series of etches, the excess Cr between the bottom contact pads, the excess Au between the top contact pads, and the photoresist layers are removed.

A device containing 63 Bi_2Te_3 (n-type) and 63 Sb_2Te_3 (p-type) thermoelectric legs, each 20 μm tall and 60 μm in diameter, was fabricated by this method and demonstrated to be capable of thermoelectric cooling. This device can be considered a prototype of future devices for exerting precise thermal control in microscopic regions and for extracting small amounts of electric power from temperature gradients.

This work was done by James Lim, Chen-Kuo Huang, Margaret Ryan, G. Jeffrey Snyder, Jennifer Herman, and Jean-Pierre Fleurial of Caltech for NASA's Jet Propulsion Laboratory. For further information contact iaoffice@jpl.nasa.gov.
NPO-30797

Low-Temperature Supercapacitors

Electrolyte compositions are designed to extend the low-temperature operational limit.

NASA's Jet Propulsion Laboratory, Pasadena, California

An effort to extend the low-temperature operational limit of supercapacitors is currently underway. At present, commercially available non-aqueous supercapacitors are rated for a minimum operating temperature of –40 °C. A capability to operate at lower temperatures would be desirable for delivering power to systems that must operate in outer space or in the Polar Regions on Earth.

Supercapacitors (also known as double-layer or electrochemical capacitors) offer a high power density (>1,000 W/kg) and moderate energy density (about 5 to 10 Wh/kg) technology for storing energy and delivering power. This combination of properties enables delivery of large currents for pulsed applications, or alternatively, smaller currents for low duty cycle applications. The mechanism of storage of electric charge in a supercapacitor — at the electrical double-layer formed at a solid-electrode/liquid-electrolyte interface — differs from that of a primary or secondary electrochemical cell (i.e., a battery) in such a manner as to impart a long cycle life (typically >10^6 charge/discharge cycles).

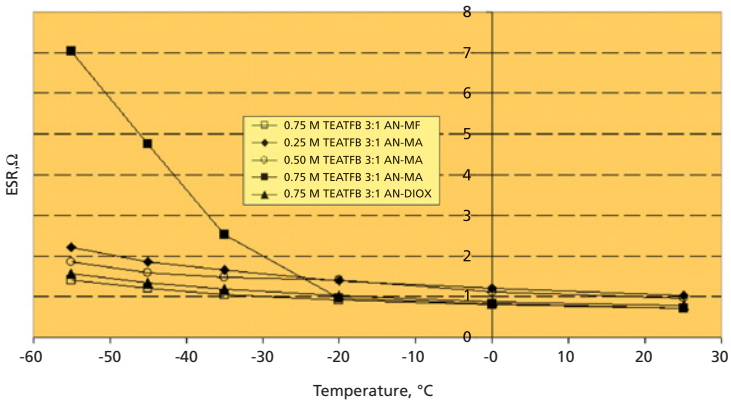
Co-Solvent	freezing point, °C
ethyl acetate	-72.0
methyl formate	-71.0
methyl acetate	-70.0
1,3–dioxolane*	-67.9
triethylamine	-62.3
* with 2% by volume triethylamine stabilizer	

Freezing Point of electrolyte solvent formulations in a 3:1 by volume ratio of acetonitrile to co-solvent.

Commercially available non-aqueous supercapacitors are limited in operation to temperatures ≈–40 °C due to the relatively high melting point of the solvent used. Typical electrolytes in commercially available supercapacitors consist of a tetraethylammonium tetrafluoroborate (TEATFB) salt dissolved in one or more solvent(s) that can include acetonitrile [AN (which freezes at –45.7 °C)] and/or propylene carbonate [PC (which freezes at –49 °C)]. Moreover, the viscosities of these solvents increase at lower temperatures, with a consequent increases in the equivalent series resistance (ESR) of the supercapacitor cell. This increase in ESR limits the power that can be delivered by the supercapacitor cell at low temperatures.

Therefore, efforts to enable operation at lower temperatures have focused on tailoring electrolytes with lower melting points (to extend the temperature range) and higher ionic conductivities and lower viscosities (to minimize increases in ESR). The approach followed thus far has targeted the use of co-solvents to depress the melting point of TEATFB/AN electrolytes while maintaining sufficient solubility of TEATFB at low temperature. These electrolytes are used in conjunction with appropriate electrode materials capable of exhibiting a suitable energy density.

The electrolytes investigated comprise the basic AN/TEATFB formulation in combination with various proportions of co-solvents that include methyl formate, methyl acetate, ethyl acetate, and 1,3-dioxolane (DX) (see table). Coin cells for evaluating the performance of these electrolytes have been fabricated using electrodes made of a commercially available high-surface-area porous carbon-based material. The electrodes were electrically isolated from each other by use of a polyethylene-based separator material. From measurements on these cells, it was concluded that the use of suitable co-solvents can enable retention, at temperatures <–45 °C, of room-temperature capacitance values. For one elec-



ESR of Supercapacitor Test Cells is shown down to –55 °C, using various low-temperature electrolytes.

trolyte formulation (comprised a 3:1 AN/DX blend), it was found that dc charging and discharging at a temperature as low as –75 °C is possible, albeit with capacitance reduced to about half its room-temperature value. By tailoring the nature of the co-solvent and the concentration of the salt used, the ESR can be minimized as well (see figure).

This work was done by Erik J. Brandon, William C. West and Marshall C. Smart of Caltech for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1).

In accordance with Public Law 96-517, the contractor has elected to retain title to this invention. Inquiries concerning rights for its commercial use should be addressed to:

Innovative Technology Assets Management
JPL
Mail Stop 202-233
4800 Oak Grove Drive
Pasadena, CA 91109-8099
E-mail: iaoffice@jpl.nasa.gov

Refer to NPO-44386, volume and number of this NASA Tech Briefs *issue, and the page number.*

Making a Back-Illuminated Imager With Back-Side Contact and Alignment Markers

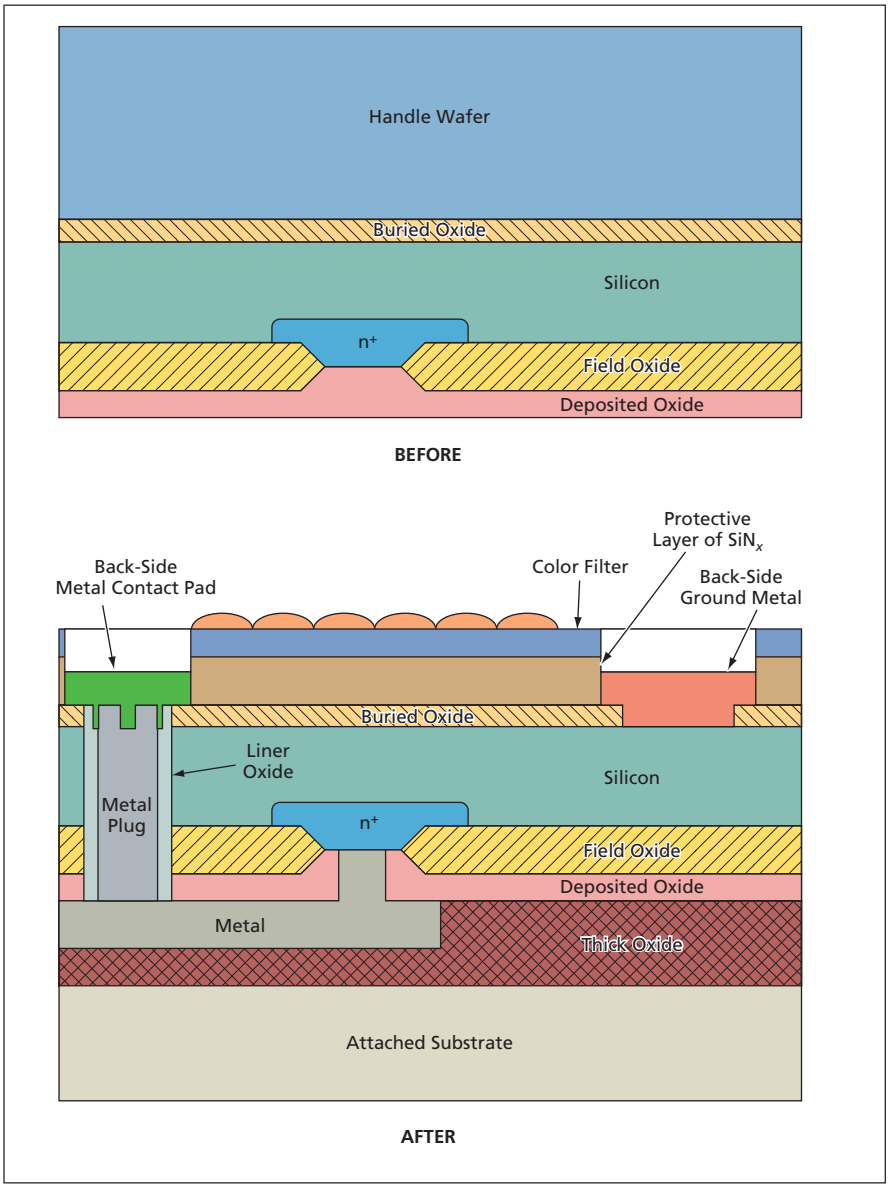
Metal plugs provide both electrical contact and alignment.

NASA's Jet Propulsion Laboratory, Pasadena, California

A design modification and a fabrication process that implements the modification have been conceived to solve two problems encountered in the development of back-illuminated, back-side-thinned complementary metal oxide/semiconductor (CMOS) image-detector integrated circuits. With respect to such an integrated circuit to be fabricated on a silicon substrate, the two problems are (1) how to form metal electrical-contact pads on the back side that are electrically connected through the thickness in proper alignment with electrical contact points on the front side and (2) how to provide alignment keys on the back side to ensure proper registration of back-side optical components (e.g., microlenses and/or color filters) with the front-side pixel pattern. (In this special context, "front side" signifies that face of the substrate upon which the pixel pattern and the associated semiconductor devices and metal conductor lines are formed.)

The essence of the design modification is to add metal plugs that extend from the desired front-side locations through the thickness and protrude from the back side of the substrate. The plugs afford the required front-to-back electrical conduction, and the protrusions of the plugs serve as both the alignment keys and the bases upon which the back-side electrical-contact pads can be formed.

The fabrication process for implementing this design modification would be complex and would be subject to variation as needed for different image-detector applications. Immediately before the beginning of this process, the integrated circuitry would already have been fabricated on the front side of the sub-



These **Simplified Cross Sections** (not to scale) depict the effect of the design modification and process on part of one pixel.