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Hayworth et al.

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(54) **MULTIPLE INTERNAL SEAL RING MICRO-ELECTRO-MECHANICAL SYSTEM VACUUM PACKAGING METHOD**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **11/850,458**

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Related U.S. Application Data

(62) Division of application No. 10/865,344, filed on Jun. 10, 2004, now Pat. No. 7,285,844.

(60) Provisional application No. 60/477,463, filed on Jun. 10, 2003.

(51) **Int. Cl.**
B44C 1/22 (2006.01)
H01L 21/00 (2006.01)

(52) **U.S. Cl.** **216/2**; 216/13; 216/41; 438/455; 438/456; 257/659; 257/660

(58) **Field of Classification Search** 257/659, 257/660; 438/455, 456; 216/2, 41, 13
See application file for complete search history.

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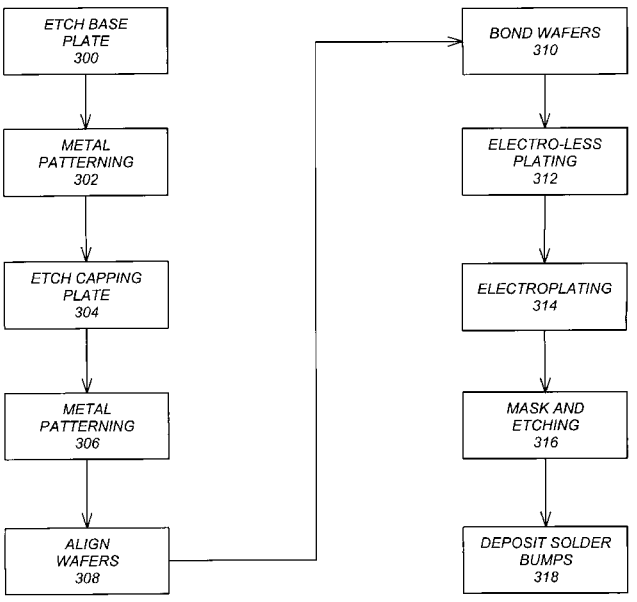
(57) **ABSTRACT**

A Multiple Internal Seal Ring (MISR) Micro-Electro-Mechanical System (MEMS) vacuum packaging method that hermetically seals MEMS devices using MISR. The method bonds a capping plate having metal seal rings to a base plate having metal seal rings by wafer bonding the capping plate wafer to the base plate wafer. Bulk electrodes may be used to provide conductive paths between the seal rings on the base plate and the capping plate. All seals are made using only metal-to-metal seal rings deposited on the polished surfaces of the base plate and capping plate wafers. However, multiple electrical feed-through metal traces are provided by fabricating via holes through the capping plate for electrical connection from the outside of the package through the via-holes to the inside of the package. Each metal seal ring serves the dual purposes of hermetic sealing and providing the electrical feed-through metal trace.

15 Claims, 10 Drawing Sheets



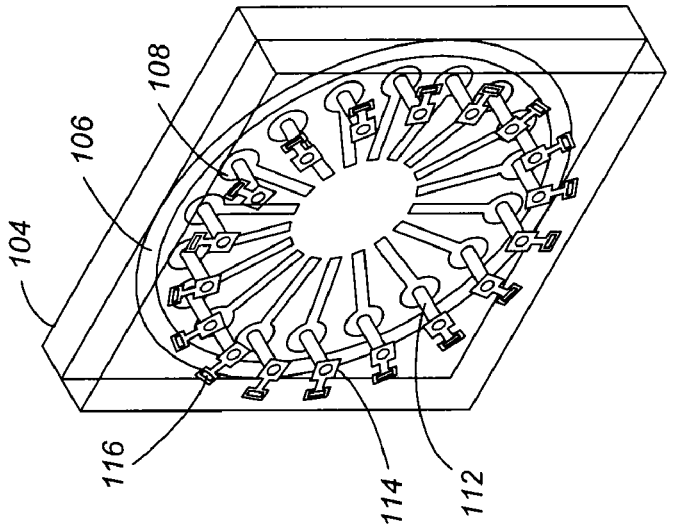


FIG. 1C

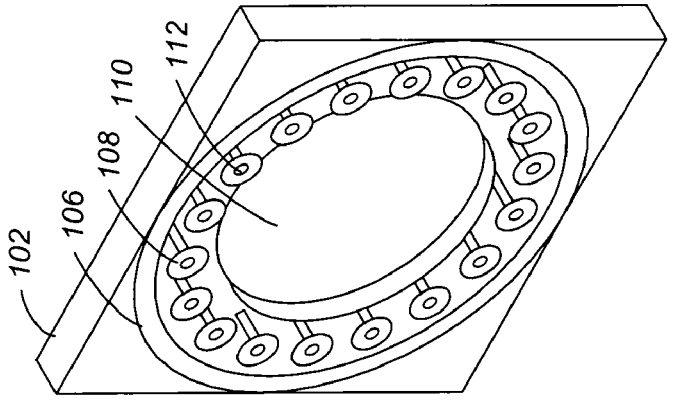


FIG. 1B

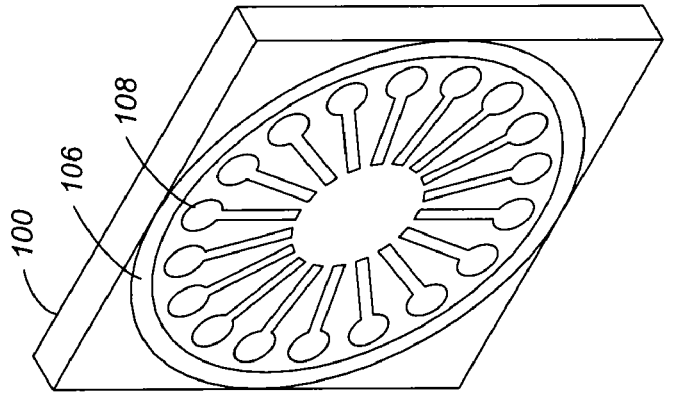


FIG. 1A

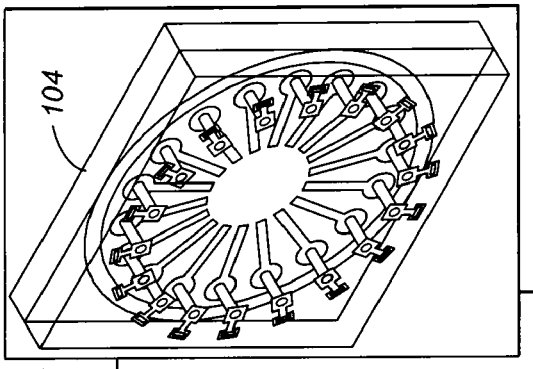


FIG. 2C

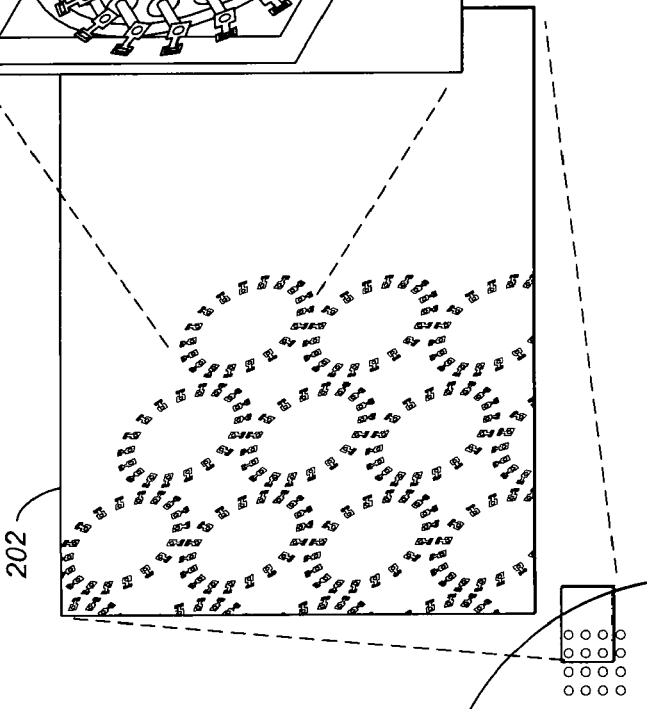


FIG. 2B

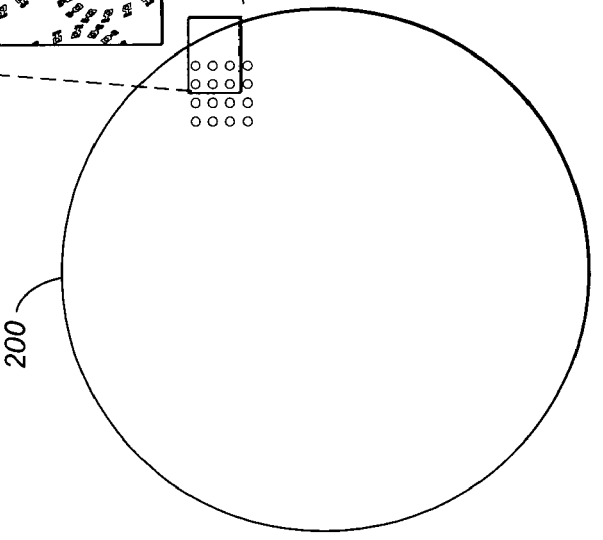


FIG. 2A

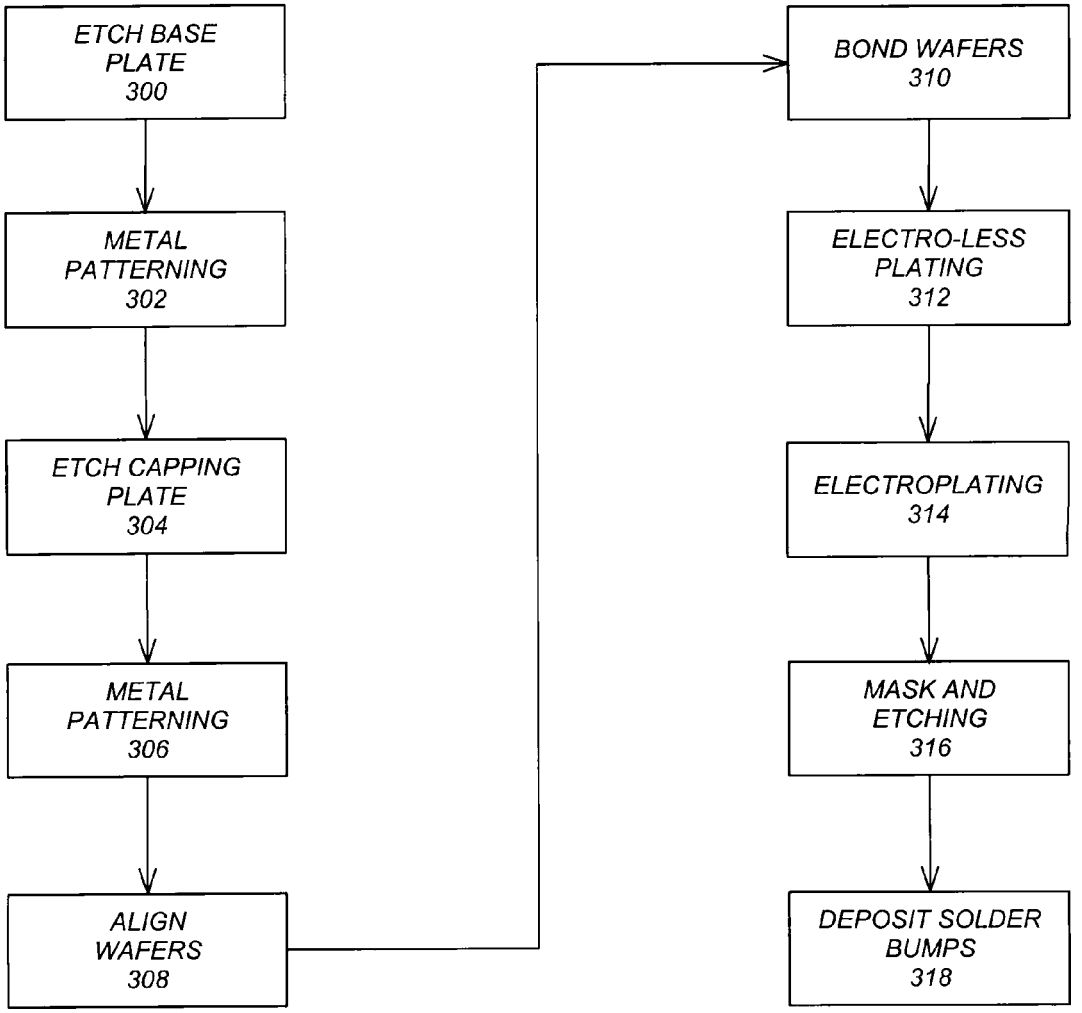

ETCH BASE PLATE 300
METAL PATTERNING 302
ETCH CAPPING PLATE 304
METAL PATTERNING 306
ALIGN WAFERS 308
BOND WAFERS 310
ELECTRO-LESS PLATING 312
ELECTROPLATING 314
MASK AND ETCHING 316
DEPOSIT SOLDER BUMPS 318

FIG. 3

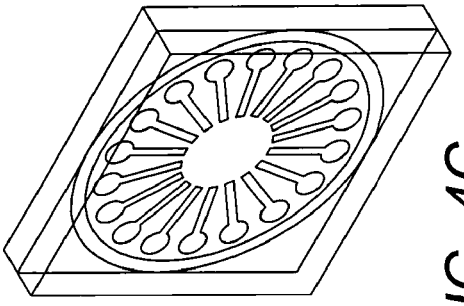


FIG. 4C

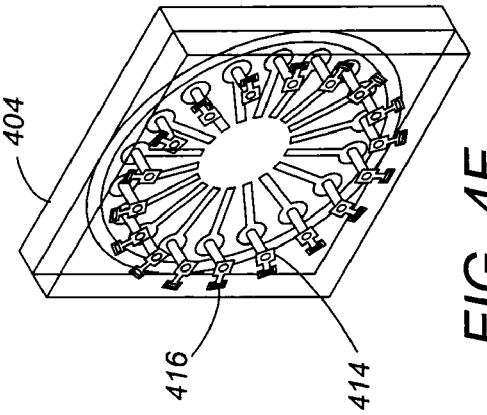


FIG. 4F

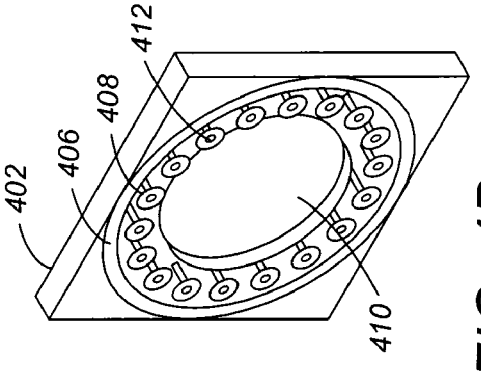


FIG. 4B

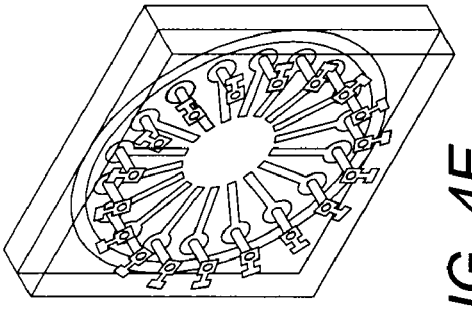


FIG. 4E

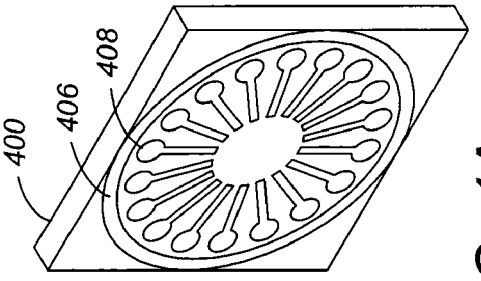


FIG. 4A

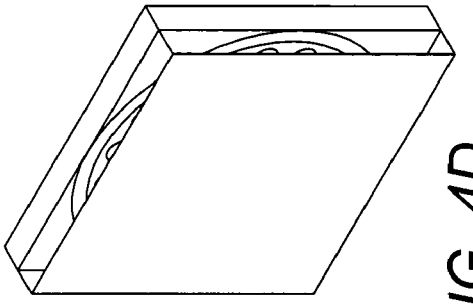
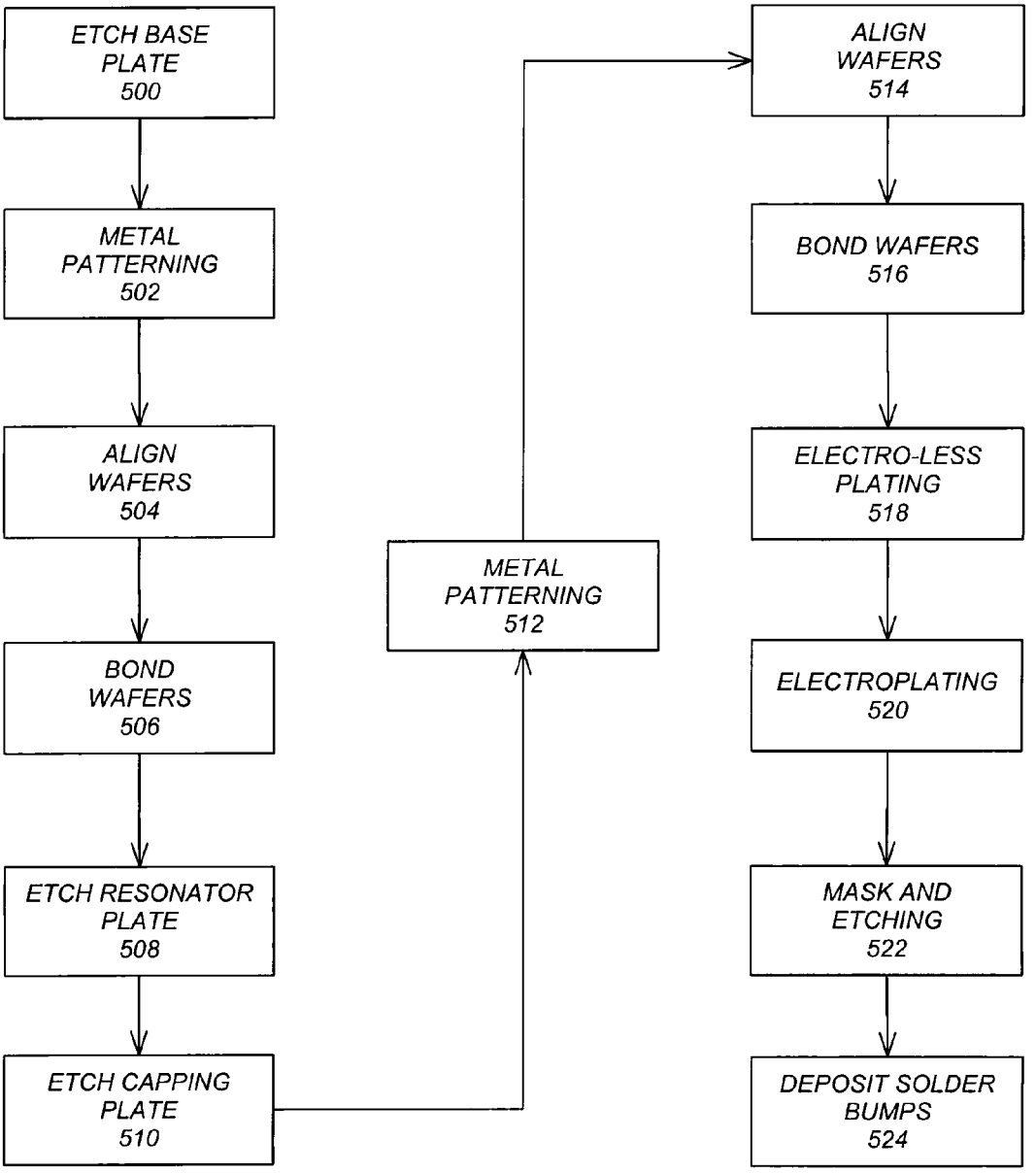


FIG. 4D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METAL PATTERNING 502
ALIGN WAFERS 504
BOND WAFERS 506
ETCH RESONATOR PLATE 508
ETCH CAPPING PLATE 510
METAL PATTERNING 512
ALIGN WAFERS 514
BOND WAFERS 516
ELECTRO-LESS PLATING 518
ELECTROPLATING 520
MASK AND ETCHING 522
DEPOSIT SOLDER BUMPS 524

FIG. 5

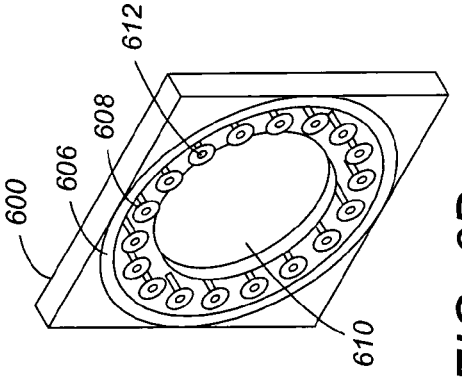


FIG. 6D

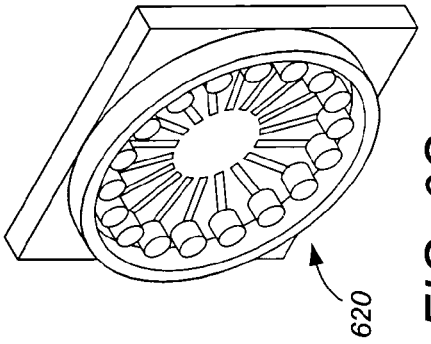


FIG. 6C

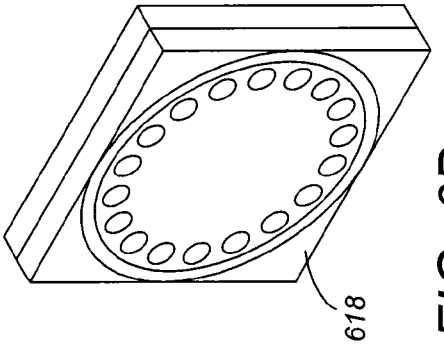


FIG. 6B

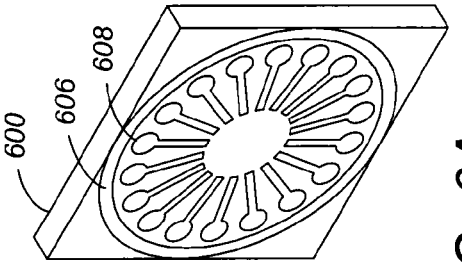


FIG. 6A

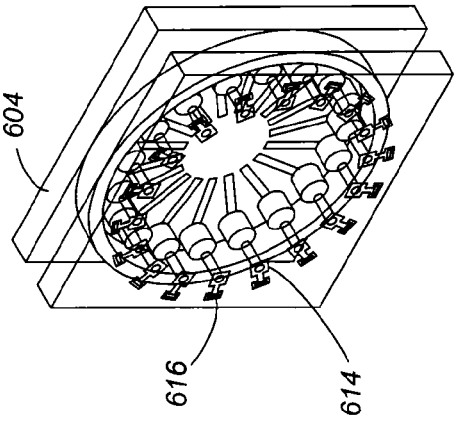


FIG. 6G

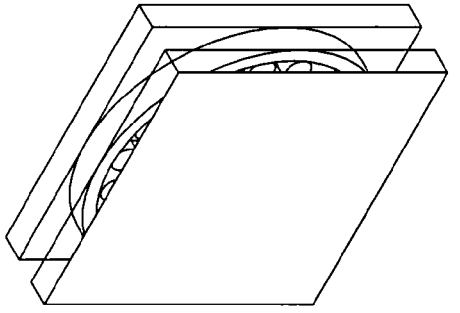


FIG. 6F

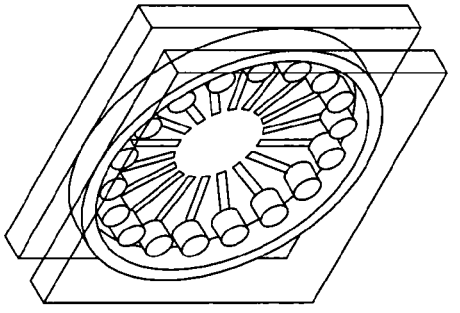


FIG. 6E

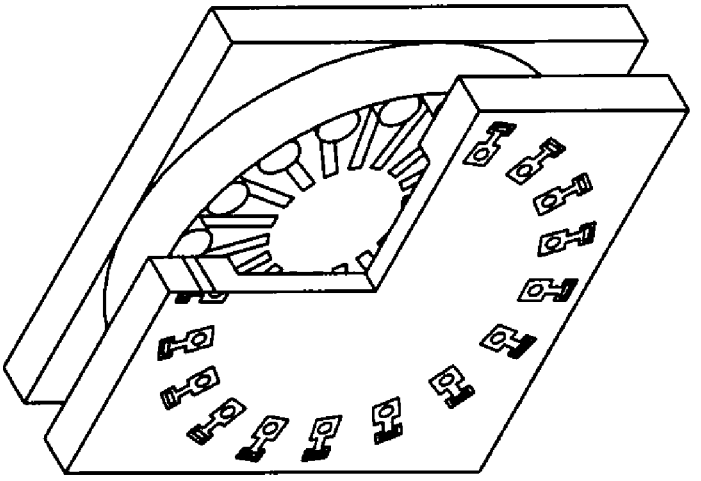


FIG. 7B

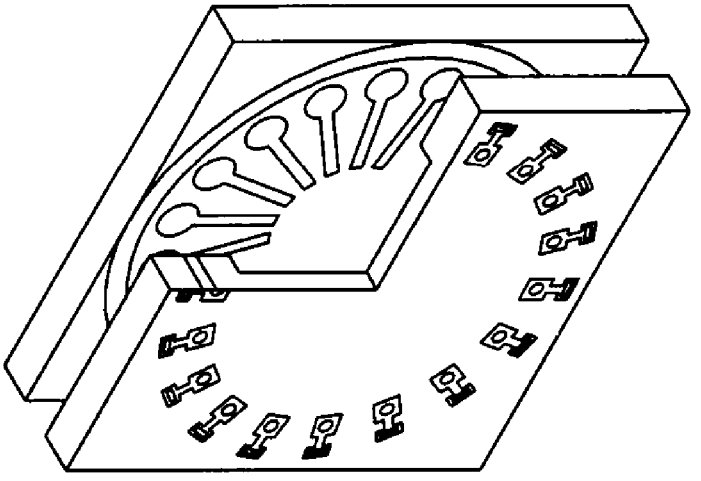
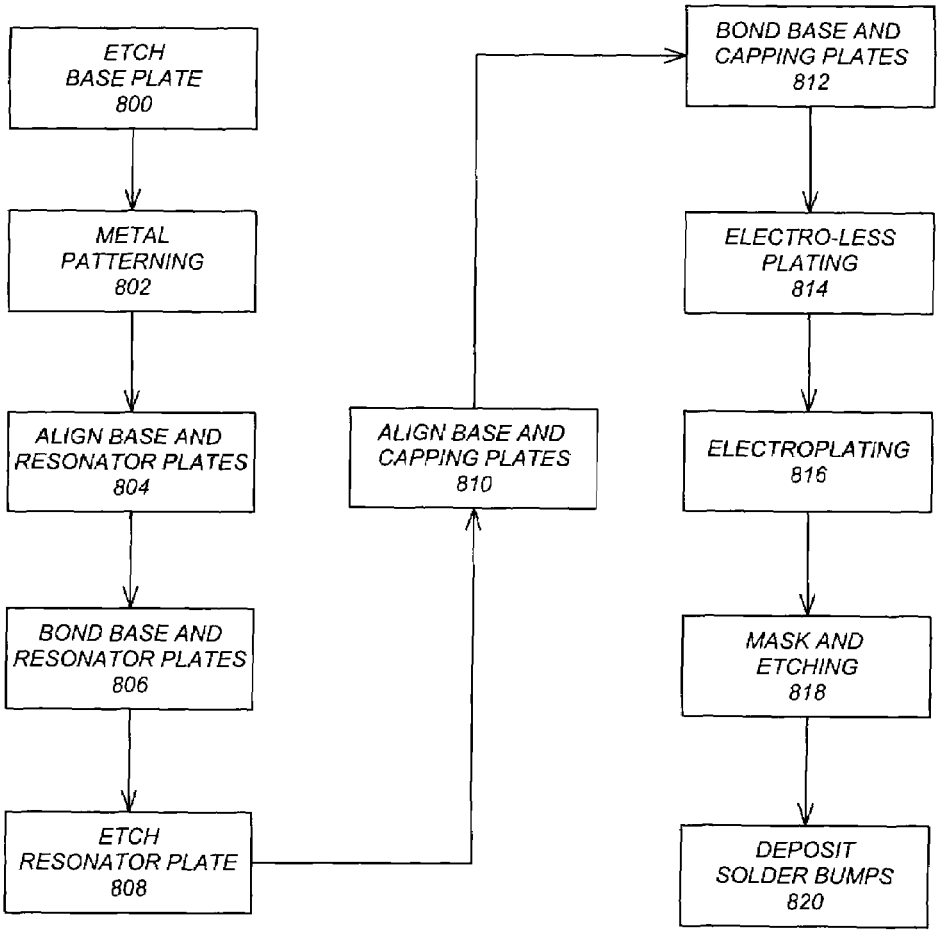


FIG. 7A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METAL PATTERNING 802
ALIGN BASE AND RESONATOR PLATES 804
BOND BASE AND RESONATOR PLATES 806
ETCH RESONATOR PLATE 808
ALIGN BASE AND CAPPING PLATES 810
BOND BASE AND CAPPING PLATES 812
ELECTRO-LESS PLATING 814
ELECTROPLATING 816
MASK AND ETCHING 818
DEPOSIT SOLDER BUMPS 820

FIG. 8

FIG. 9A

FIG. 9B

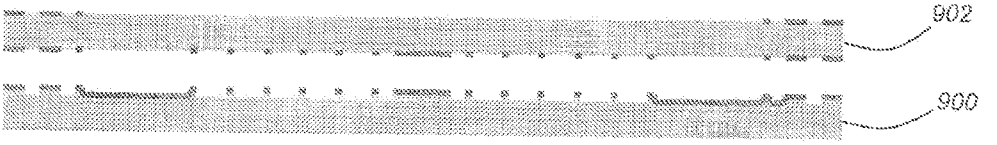

FIG. 9C

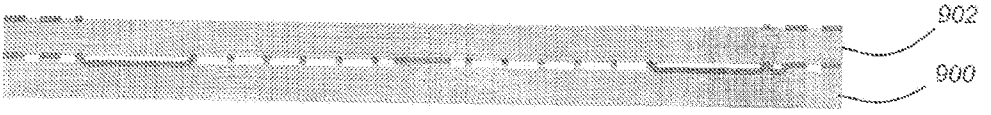

FIG. 9D

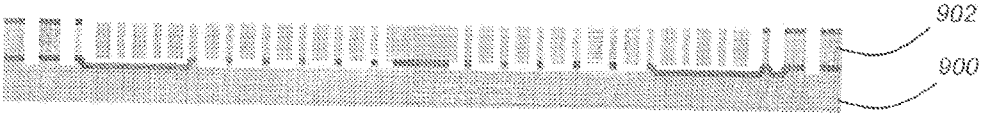

FIG. 9E

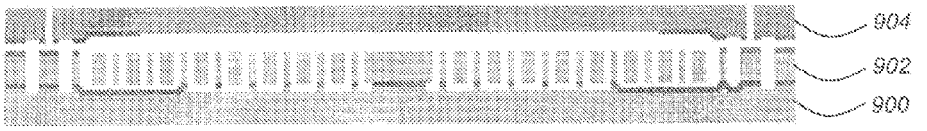

FIG. 9F

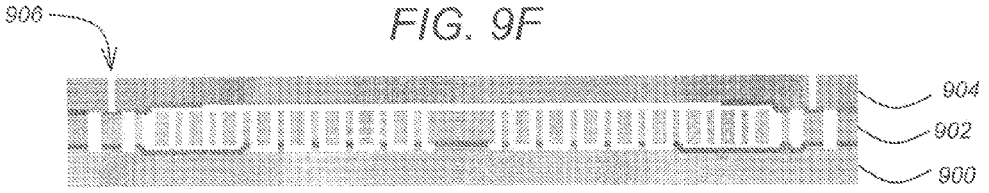

FIG. 9G

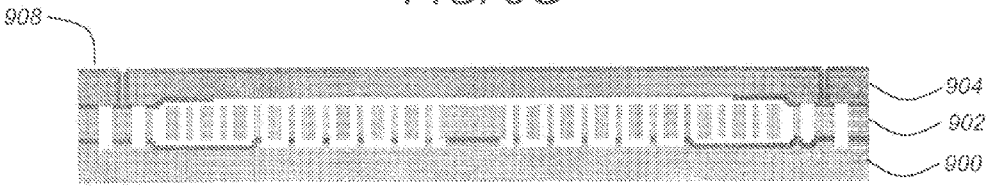

FIG. 9H

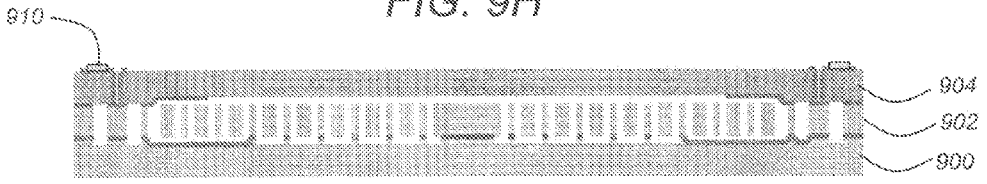

FIG. 9I

MULTIPLE INTERNAL SEAL RING MICRO-ELECTRO-MECHANICAL SYSTEM VACUUM PACKAGING METHOD

CROSS-REFERENCE TO RELATED APPLICATIONS

This divisional application claims the benefit under 35 U.S.C. §120 of the following U.S. patent application, which is incorporated by reference herein:

U.S. patent application Ser. No. 10/865,344, filed Jun. 10, 2004 now U.S. Pat. No. 7,285,844, by Hayworth et al., entitled "MULTIPLE INTERNAL SEAL RING MICRO-ELECTRO-MECHANICAL VACUUM PACKAGE," which claims the benefit of U.S. Provisional Application Ser. No. 60/477,463, filed on Jun. 10, 2003, by Ken J. Hayworth, Karl Y. Yee, Kirill V. Shcheglov, Youngsam Bae, Dean V. Wiberg, A. D. Challoner, and Chris S. Peay, entitled "MULTIPLE INTERNAL SEAL RING MEMS VACUUM PACKAGE."

This application is related to the following U.S. Patents, which are all incorporated by reference herein:

U.S. Pat. No. 7,040,163, issued May 9, 2006, by Shcheglov et al., entitled ISOLATED PLANAR GYROSCOPE WITH INTERNAL RADIAL SENSING AND ACTUATION, which claims the benefit of both U.S. Provisional Patent Application Ser. No. 60/402,681, filed Aug. 12, 2002, by Shcheglov et al. and U.S. Provisional Patent Application Ser. No. 60/428,451, filed Nov. 22, 2002, by Shcheglov et al.;

U.S. Pat. No. 6,944,931, issued Sep. 20, 2005, by Shcheglov et al., entitled METHOD OF PRODUCING AN INTEGRAL RESONATOR SENSOR AND CASE, which claims the benefit of both U.S. Provisional Patent Application Ser. No. 60/402,681, filed Aug. 12, 2002, by Shcheglov et al. and U.S. Provisional Patent Application Ser. No. 60/428,451, filed Nov. 22, 2002, by Shcheglov et al.;

U.S. Pat. No. 7,017,410, issued Mar. 28, 2006, by Challoner et al., entitled ISOLATED RESONATOR GYROSCOPE WITH A DRIVE AND SENSE PLATE, which is a continuation-in-part of U.S. Pat. No. 6,629,460, issued Oct. 7, 2003, to A. Dorian Challoner, entitled ISOLATED RESONATOR GYROSCOPE;

U.S. Pat. No. 6,990,863, issued Jan. 31, 2006, by Challoner et al., entitled ISOLATED RESONATOR GYROSCOPE WITH ISOLATION TRIMMING USING A SECONDARY ELEMENT, which is a continuation-in-part of U.S. Pat. No. 6,629,460, issued Oct. 7, 2003, to Challoner, entitled ISOLATED RESONATOR GYROSCOPE; and

U.S. Pat. No. 6,955,084, issued Oct. 18, 2005, by Challoner et al., entitled ISOLATED RESONATOR GYROSCOPE WITH COMPACT FLEXURES, which is a continuation-in-part of U.S. Pat. No. 6,629,460, issued Oct. 7, 2003, to Challoner, entitled ISOLATED RESONATOR GYROSCOPE.

STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT

The invention described herein was made in the performance of work under a NASA contract, and is subject to the provisions of Public Law 96-517 (35 USC 202) in which the Contractor has elected to retain title.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to vacuum packages, and particularly to multiple internal seal ring (MISR) micro-electro-mechanical (MEMS) vacuum packages.

2. Description of the Related Art

It is well known in the art to fabricate micro-electro-mechanical system (MEMS) devices. MEMS devices typically integrate both electronic and mechanical elements on a semiconductor wafer using semiconductor fabrication techniques. Generally, the electronic and mechanical elements are fabricated using a variety of integrated circuit (IC) processing and micromachining techniques, respectively.

In the fabrication of MEMS devices, it is not unusual to package or "cap" such devices to prevent damage or contamination to the MEMS devices. Often, the cap comprises a capping plate fabricated from a capping wafer that is bonded to a base plate before the base plate wafer is diced or singulated into individual devices. The capping plate thus hermetically seals the MEMS devices within the base plate.

Even though sealed by the capping plate, the MEMS devices require electrical connection to external circuits. However, the traces used for connection may create gaps where the capping plate and base plate are bonded. Generally, the surfaces where the capping plate wafer and the base plate wafer are bonded must be ultra-flat, i.e., polished. This flatness requirement is difficult to meet if additional processing steps are required for bringing electrical feed-through metal traces out through the bonded surfaces. Specifically, bringing electrical wires out through the bonded surfaces requires metal patterning and oxide growth on the wafers' surfaces. Achieving a bond or seal on top of these uneven surfaces is much more difficult.

Accordingly, what is needed, therefore, is an improved method for sealing and packaging MEMS devices that allows for electrical connection to external circuits.

SUMMARY OF THE INVENTION

To minimize the limitations in the related art described above, and to minimize other limitations that will become apparent upon reading and understanding the present specification, the present invention discloses a Multiple Internal Seal Ring (MISR) Micro-Electro-Mechanical System (MEMS) vacuum package that hermetically seals MEMS devices using MISR. The method bonds a capping plate having metal seal rings to a base plate having metal seal rings by wafer bonding the capping plate wafer to the base plate wafer. Bulk electrodes may be used to provide conductive paths between the seal rings on the base plate and the capping plate. All seals are made using only metal-to-metal seal rings deposited on the polished surfaces of the base plate and capping plate wafers. However, multiple electrical feed-through metal traces are provided by fabricating via holes through the capping plate for electrical connection from the outside of the package through the via-holes to the inside of the package. Each metal seal ring serves the dual purposes of hermetic sealing and providing the electrical feed-through metal trace.

BRIEF DESCRIPTION OF THE DRAWINGS

Referring now to the drawings in which like reference numbers represent corresponding parts throughout:

FIGS. **1**A, **1**B and **1**C are perspective views of an embodiment of the present invention, wherein FIG. **1**A comprises a base plate, FIG. **1**B comprises a capping plate and FIG. **1**C shows the final sealed multiple internal seal ring vacuum package;

FIGS. **2**A, **2**B and **2**C are perspective views of the results of wafer scale processing of the vacuum package before singulation, wherein FIG. **2**A illustrates bonded wafers containing a plurality of micro-electro-mechanical system devices that

are vacuum sealed simultaneously during wafer bonding of a wafer containing the base plates and a wafer containing the capping plates, FIG. **2**B is a magnified view of a portion of the bonded wafers, and FIG. **2**C is a magnified view of the final sealed multiple internal seal ring vacuum package comprised of the joined base plate and capping plate found in the portion of the bonded wafers.

FIG. **3** is a flowchart that illustrates the steps of a first general micro-electro-mechanical system processing paradigm for a surface processed micro-electro-mechanical system device etched directly from the base plate wafer that is vacuum packaged using the capping plate wafer;

FIGS. **4**A-**4**F illustrate the results of the flowchart of FIG. **3**;

FIG. **5** is a flowchart that illustrates the steps of a second general micro-electro-mechanical system processing paradigm for a two-wafer bulk silicon etched micro-electro-mechanical system device etched from a bonded base plate wafer and resonator wafer that is vacuum packaged using the capping plate wafer;

FIGS. **6**A-**6**G illustrate the results of the flowchart of FIG. **5**;

FIGS. **7**A and **7**B illustrate a comparison of the multiple internal seal ring vacuum package design for the two-wafer (surface processed micro-electro-mechanical system device) and three-wafer (bulk processed micro-electro-mechanical system device) designs, wherein FIG. **7**A is a partially-cutaway view of the two-wafer multiple internal seal ring vacuum package and FIG. **7**B is a partially-cutaway view of the three-wafer multiple internal seal ring vacuum package;

FIG. **8** is a flowchart that illustrates the steps of the three-wafer design packaging a planar gyroscope; and

FIGS. **9**A-**9**I illustrate the results of the flowchart of FIG. **8**.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

In the following description of the preferred embodiment, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration a specific embodiment in which the invention may be practiced. It is to be understood that other embodiments may be utilized and structural changes may be made without departing from the scope of the present invention.

Overview

The present invention discloses a method of vacuum sealing or hermetically sealing Micro-Electro-Mechanical Systems (MEMS) devices using MISR at a wafer level before singulation or dicing. The method bonds a capping plate having metal seal rings to a base plate having metal seal rings by wafer bonding the capping plate wafer to the base plate wafer. Bulk electrodes may be used to provide conductive paths between the seal rings on the base plate and the capping plate. This method works best if the bonding surface of the base plate wafer and the bonding surface of the capping plate wafer are ultra-flat (i.e., polished) before the metal seal rings are deposited on each surface.

This flatness requirement is difficult to meet if additional processing steps are required for bringing electrical feed-through metal traces out underneath the seal rings. Specifically, bringing electrical feed-through metal traces out under the seal rings requires metal patterning and oxide growth on the wafer's surface, which results in an uneven surface. Achieving a metal-to-metal vacuum seal on top of this uneven surface is much more difficult than achieving a metal-to-metal vacuum seal between polished, ultra-flat surfaces.

All seals are made using only metal-to-metal seal rings deposited on the polished surfaces of the base plate wafer and the capping plate wafer. However, the package still enables multiple electrical feed-through metal traces by fabricating multiple via holes through the capping plate for electrical connection from the outside of the vacuum package through the via-holes to the inside of the vacuum package. Each metal seal ring serves the dual purposes of hermetic sealing and providing an electrical feed-through metal trace.

FIGS. **1**A, **1**B and **1**C are perspective views of an embodiment of the present invention, wherein FIG. **1**A comprises a base plate **100**, FIG. **1**B comprises a capping plate **102** and FIG. **1**C shows a final, vacuum-sealed, MISR device package **104** comprised of the bonded base plate **100** and capping plate **102**, wherein the capping plate **102** is flipped before being bonded to the base plate **100**, and the capping plate **102** is shown semi-transparently to better illustrate the components of the package **104**. The base plate **100** and the capping plate **102** each include a large periphery seal ring **106** that is used to create one large metal-to-metal seal surrounding the periphery of the package **104** when the base plate **100** and the capping plate **102** are bonded together. In addition, the base plate **100** and the capping plate **102** each include a plurality of small internal seal rings **108**. The seal rings **108** of the base plate **100** each provide an independent electrical path from a cavity **110** of the capping plate **102** where the MEMS device (not shown) resides outward towards the periphery of the package **104**, but not crossing the seal ring **106**. Each of the seal rings **108** of the capping plate **102** surround and electrically connect to one of a plurality of via holes **112** on a bottom surface of the capping plate **102**. Each via hole **112** extends through the capping plate **102** to a top surface of the capping plate **102**, where the via hole **112** electrically connects to an electrical trace pattern **114** and solder bump **116** on the top surface of the capping plate **102**. The package **104** is sealed by compression bonding of the metal-to-metal seal rings **106** and **108**, which is followed by singulation to separate the multiple packages **104** on the bonded wafers.

Although FIGS. **1**A, **1**B and **1**C illustrate only a single package **104**, the potential benefits (cost savings and simplified, more reliable manufacturing process) of the MISR device package **104** are most dramatic when performed by wafer scale processing. FIGS. **2**A, **2**B and **2**C are perspective views of the results of wafer scale processing of the package **104** before singulation, wherein FIG. **2**A illustrates bonded wafers **200** containing a plurality of MEMS devices that are sealed simultaneously during wafer bonding of a wafer containing the base plates **100** and a wafer containing the capping plates **102**, FIG. **2**B is a magnified view of a portion **202** of the bonded wafers **200**, and FIG. **2**C is a magnified view of final, vacuum-sealed, MISR device package **104** comprised of the joined base plate **100** and capping plate **102** found in the portion **202** of the bonded wafers **200**.

Process Steps

There are two general MEMS processing paradigms to which the package is aimed.

In the first general MEMS processing paradigm, a surface-processed MEMS device is packaged according to the steps outlined in FIG. **3** and illustrated in FIGS. **4**A-**4**F, wherein FIGS. **4**A-**4**F show a base plate **400**, capping plate **402**, package **404**, large external seal rings **406**, small internal seal rings **408**, etched cavity **410** of the capping plate **402**, etched via holes **412** in the capping plate **402**, electrical trace patterns **414** and solder bumps **416**.

Blocks **300** and **302** of FIG. **3** illustrate the processing of the base plate **400**, which is generally comprised of silicon or other semiconducting material, and which is illustrated in

FIG. **4**A. Block **300** represents the etching of the base plate **400** in a manner that avoids etching under seal rings **406** and **408**. Block **302** represents the metal patterning of the seal rings **406** and **408**.

Blocks **304** and **306** of FIG. **3** illustrate the processing of the capping plate **402**, which is generally comprised of glass or other non-conducting material, and which is illustrated in FIG. **4**B. Block **304** represents the etching of the via holes **412** and cavity **410** (if needed) in the capping plate **402**. Block **306** represents the metal patterning of the seal rings **406** and **408** on the bottom surface of the capping plate **402**.

Blocks **308** and **310** of FIG. **3** illustrate the bonding of the base plate **400** and the capping plate **402**, which is illustrated in FIG. **4**C. Block **308** represents the aligning of the base plate **400** and capping plate **402** wafers, which includes the aligning of the seal rings **406** and **408** of the base plate **400** and capping plate **402**. Block **310** represents the bonding of the base plate **400** and capping plate **402** wafers using heat and pressure in an evacuated chamber.

Blocks **312** and **314** of FIG. **3** illustrate the plating of the capping plate **402**, which is illustrated in FIG. **4**D. Block **312** represents the electro-less plating of a thin metal layer on the top surface of the capping plate **402**, including inside the via holes **412**. Block **314** represents the electroplating of a thicker metal layer on top of the thin metal layer.

Block **316** of FIG. **3** illustrates the patterning of the electrical trace patterns **414** on the surface of the capping plate **402**, which is illustrated in FIG. **4**E. Block **316** represents the masking and etching of the electrical trace patterns **414** on the top surface of the capping plate **402**.

Block **318** of FIG. **3** illustrates the final processing prior to singulation, which is illustrated in FIG. **4**E. Block **318** represents the depositing of the solder bumps **416** at one end of the electrical trace patterns **414** etched on the top surface of the capping plate **402**, in order to complete the package **404**.

In the second general MEMS processing paradigm, a two-wafer bulk-silicon-etched MEMS device is packaged according to the steps outlined in FIG. **5** and illustrated in FIGS. **6**A-**6**G, wherein FIGS. **6**A-**6**G show a base plate **600**, capping plate **602**, package **604**, large external seal rings **606**, small internal seal rings **608**, etched cavity **610** of the capping plate **602**, etched via holes **612** in the capping plate **602**, electrical trace patterns **614** and solder bumps **616**. In this embodiment, there is also a resonator plate **618** that is used to create a MEMS device resonator (not shown), wherein the resonator plate **618** includes bulk electrodes **620** that provide conductive paths between the seal rings **606** and **608** on both the base plate **600** and capping plate **602**.

Blocks **500** and **502** of FIG. **5** illustrate the processing of the base plate **600**, which is generally comprised of silicon or other semiconducting material, and which is illustrated in FIG. **6**A. Block **500** represents the etching of the base plate **600** in a manner that avoids etching under seal rings **606** and **608**. Block **502** represents the metal patterning of the seal rings **606** and **608**.

Blocks **504** and **506** of FIG. **5** illustrate the vacuum bonding of the base plate **600** and the resonator plate **616**, which is illustrated in FIG. **6**B. Block **504** represents the aligning of the base plate **602** and resonator plate **616** wafers. Block **506** represents the bonding of the base plate **602** and resonator plate **618** wafers using heat and pressure in an evacuated chamber.

Block **508** of FIG. **5** illustrates the etching of the resonator plate **616**, which is generally comprised of silicon or other semiconducting material, and which is illustrated in FIG. **6**C. Block **508** represents the etching of the MEMS resonator (not shown) and bulk electrodes **620**, wherein the doped silicon or a metalization of the resonator plate **618** provides conductive paths for the electrodes **620**.

Blocks **510** and **512** of FIG. **5** illustrate the processing of the capping plate **602**, which is preferably comprised of glass or other non-conducting material, and which is illustrated in FIG. **6**D. Block **510** represents the etching of the via holes **612** and cavity **610** (if needed) of the capping plate **602**. Block **512** represents the metal patterning of the seal rings **606** and **608** on the bottom surface of the capping plate **602**.

Blocks **514** and **516** of FIG. **5** illustrate the bonding of the resonator plate **616** and capping plate **602** wafers, which is illustrated in FIG. **6**E. Block **514** represents the aligning of the resonator plate **618** and capping plate **602** wafers, and more specifically, the aligning of the bulk electrodes **620** of the resonator plate **618** with the seal rings **606** and **608** of the capping plate **602**. Block **516** represents the bonding of the resonator plate **618** and capping plate **602** wafers using heat and pressure in an evacuated chamber.

Blocks **518** and **520** of FIG. **5** illustrate the metal plating of the capping plate **602**, which is illustrated in FIG. **6**F. Block **518** represents the electro-less plating of a thin metal layer on a top surface of the capping plate **602** including inside the via holes **612**. Block **520** represents the electroplating of a thicker metal layer on the thin metal layer.

Blocks **522** and **524** of FIG. **5** illustrate the final processing, which is illustrated in FIG. **6**G. Block **522** represents the masking and etching of the electrical trace pattern **614** on the top surface of the capping plate **602**. Block **524** represents the depositing of the solder bumps **616** at one end of the electrical trace pattern **614** etched on the top surface of the capping plate **602**, in order to complete the package **604**.

A comparison of the MISR vacuum package design for the two-wafer (surface processed MEMS device) and three-wafer (two-wafer bulk-silicon-etched MEMS device) are shown in the cutaway views of FIGS. **7**A and **7**B, wherein FIG. **7**A is a partially-cutaway view of the two-wafer MISR package and FIG. **7**B is a partially-cutaway view of the three-wafer MISR package.

The three-wafer MISR package of FIG. **5**, FIGS. **6**A-**6**G and **7**B may be used to vacuum package a planar gyroscope described in U.S. Pat. No. 7,040,163, issued May 9, 2008, by Shcheglov et al., entitled ISOLATED PLANAR GYROSCOPE WITH INTERNAL RADIAL SENSING AND ACTUATION, which is incorporated by reference herein. However, certain modifications to the package are required.

The planar gyroscope has a large total number of electrodes (48 individual electrode elements). If all of these electrodes were brought out of the package through individual seal rings, the increase in total die area would be prohibitive. This is because a "sealing bulk electrode" must have a large enough diameter to support a good vacuum seal. To avoid having 48 sealing bulk electrodes, electrical connections crisscrossing inside the package are used to connect common sets of electrodes. In the planar gyroscope design, the 48 individual electrodes are reduced to only 12 electrode sets requiring individual package feed-throughs. Thus only 12 sealing bulk electrodes are needed in the final design, and these easily fit into the unused corners of the square planar package.

The internal wire routing (connecting the 48 individual electrodes into 12 sets) requires crossing some wires, and thus requires at least two metal routing layers. The design of the MISR package allows this to be achieved without requiring an extra metalization and oxide growth process (which would interfere with the surface flatness required for good sealing). This crisscrossing of wires is achieved by using small "bridging bulk electrodes" to act as vias between the base plate's

metal patterning and the capping plate's internal metal pattern. In the current design, 48 of these small bridging bulk electrodes are used (to connect each individual electrode with a circular shorting pattern on the capping plate) and 12 sealing bulk electrodes are used to provide the final package feedthroughs for each electrode set.

As noted above, the processing steps used to create such an MISR package are generally reflected in FIG. **5** and FIGS. **6**A-**6**G. However, some of the steps are further described in FIG. **8** and illustrated as cross-sectional views in FIGS. **9**A-**9**I.

Block **800** represents the etching of the base plate **900**, which is illustrated in FIG. **9**A.

Block **802** represents the metal patterning of the base plate **900**, which is illustrated in FIG. **9**B.

Block **804** represents the aligning of the base plate **900** and resonator plate **902**, which was processed separately, and which is illustrated in FIG. **9**C.

Block **806** represents the bonding of the base plate **900** and resonator plate **902**, which is illustrated in FIG. **9**D.

Block **808** represents the deep silicon etching of the resonator plate **902**, which is illustrated in FIG. **9**E.

Block **810** represents the aligning of the base plate **900** and capping plate **904**, which was processed separately, and which is illustrated in FIG. **9**F.

Block **812** represents the bonding of the base plate **900** and capping plate **904**, which is illustrated in FIG. **9**G.

Block **814** represents the electro-less plating of the capping plate **904**, including its via holes **906**, which is illustrated in FIG. **9**H.

Block **816** represents the electroplating of the capping plate **904**, including its via holes **906**, which is also illustrated in FIG. **9**H.

Block **818** represents the masking and etching of the electrical trace pattern **908** on the top surface of the capping plate **904**, which is illustrated in FIG. **9**I.

Block **820** represents the depositing of the solder bumps **910** at one end of the electrical trace pattern **908** etched on the top surface of the capping plate **904**, which is also illustrated in FIG. **9**I.

CONCLUSION

This concludes the description of the preferred embodiment of the present invention. The following describes some alternative embodiments for accomplishing the present invention.

For example, although specific structures are described in this specification, other structures could be used as well without departing from the scope of the present invention. Variations in the components used in the present invention are possible.

Further, the specific logic or steps performed by the present invention are described for illustration purposes only, and other logic or steps could be used as well. Many variations of the logic and steps performed by the present invention are possible.

The foregoing description of one or more embodiments of the invention has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed. Many modifications and variations are possible in light of the above teaching. It is intended that the scope of the invention be limited not by this detailed description, but rather by the claims appended hereto.

What is claimed is:

1. A method of fabricating a device package, comprising:
(a) metal patterning of at least one seal ring on a base plate;
(b) etching of via holes in a capping plate;
(c) metal patterning of at least one seal ring on a bottom surface of the capping plate;
(d) aligning of the base plate and capping plate;
(e) bonding of the base plate and capping plate;
(f) electro-less plating of a thin metal layer on a top surface of the capping plate, including inside the via holes;
(g) electroplating of a thicker metal layer on top of the thin metal layer; and
(h) masking and etching of electrical trace patterns on the top surface of the capping plate.

2. The method of claim **1**, further comprising etching of a cavity in the base plate.

3. The method of claim **1**, wherein the aligning of the base plate and capping plate further comprises aligning of the seal rings of the base plate and capping plate.

4. The method of claim **1**, wherein the bonding of the base plate and capping plate wafers uses heat and pressure in an evacuated chamber.

5. The method of claim **1**, further comprising depositing of the solder bumps at one end of the electrical trace patterns etched on the top surface of the capping plate.

6. A method of fabricating a device package, comprising:
(a) metal patterning of at least one seal ring on a base plate;
(b) aligning of the base plate and a resonator plate;
(c) bonding of the base plate and resonator plate using heat and pressure in an evacuated chamber;
(d) etching of bulk electrodes on the resonator plate, wherein the doped silicon or a metalization of the resonator plate provides a conductive path for the electrodes;
(e) etching of at least one via hole in a capping plate;
(f) metal patterning of at least one seal ring on a bottom surface of the capping plate;
(g) aligning of the resonator plate and capping plate, and more specifically, the aligning of the bulk electrodes of the resonator plate with the seal rings of the capping plate;
(h) bonding of the of the resonator plate and capping plate using heat and pressure in an evacuated chamber.
(i) electro-less plating of a thin metal layer on a top surface of the capping plate including inside the via holes;
(j) electroplating of a thicker metal layer on the thin metal layer;
(k) masking and etching of an electrical trace pattern on the top surface of the capping plate.

7. The method of claim **6**, wherein the bonding of the base plate and resonator plate uses heat and pressure in an evacuated chamber.

8. The method of claim **6**, wherein doping or metalization of the resonator plate provides a conductive path for the bulk electrodes.

9. The method of claim **6**, further comprising etching a cavity in the base plate.

10. The method of claim **6**, wherein the aligning of the resonator plate and capping plate wafers comprises aligning of the bulk electrodes of the resonator plate with the seal rings of the capping plate.

11. The method of claim **6**, wherein the bonding of the base plate and capping plate uses heat and pressure in an evacuated chamber.

12. The method of claim **6**, further comprising depositing of the solder bumps at one end of the electrical trace pattern etched on the top surface of the capping plate.

13. The method of claim 6, further comprising using internal wire routing to reduce the number of bulk electrodes.

14. The method of claim 6, wherein the internal wire routing comprises criss-crossing wires and a plurality of metal routing layers.

15. The method of claim 6, wherein the crisscrossing wires use bridging bulk electrodes that act as vias between the base plate's metal patterning and the capping plate's internal metal pattern.

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