



Electronics/Computers

Spaceborne Hybrid-FPGA System for Processing FTIR Data

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Progress has been made in a continuing effort to develop a spaceborne computer system for processing readout data from a Fourier-transform infrared (FTIR) spectrometer to reduce the volume of data transmitted to Earth. The approach followed in this effort, oriented toward reducing design time and reducing the size and weight of the spectrometer electronics, has been to exploit the versatility of recently developed hybrid field-programmable gate arrays (FPGAs) to run diverse software on embedded processors while also taking ad-

vantage of the reconfigurable hardware resources of the FPGAs.

The specific FPGA/embedded-processor combination selected for this effort is the Xilinx Virtex-4 FX hybrid FPGA with one of its two embedded IBM PowerPC 405 processors. The effort has involved exploration of various architectures and hardware and software optimizations. By including a dedicated floating-point unit and a dot-product coprocessor in the hardware and utilizing optimized single-precision math library functions and a modified PowerPC performance library

in the software, it has been possible to reduce execution time to an eighth of that of a non-optimized software-only implementation. A concept for utilizing both embedded PowerPC processors to further reduce execution time has also been considered.

This work was done by Dmitriy L. Bekker, Jean-Francois L. Blavier, and Paula J. Pingree of Caltech and Marcin Lukowiak and Muhammad Shaaban of Rochester Institute of Technology for NASA's Jet Propulsion Laboratory. For more information, contact iaoffice@jpl.nasa.gov. NPO-45957

FPGA Coprocessor for Accelerated Classification of Images

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An effort related to that described in the preceding article focuses on developing a spaceborne processing platform for fast and accurate onboard classification of image data, a critical part of modern satellite image processing. The approach again has been to exploit the versatility of recently developed hybrid Virtex-4FX field-programmable gate array (FPGA) to run diverse science applications on embedded processors while taking advantage of the reconfigurable hardware resources of the FPGAs. In this case, the FPGA serves as a coprocessor that implements legacy C-language support-vector-machine (SVM) image-classification algorithms to detect and identify natural

phenomena such as flooding, volcanic eruptions, and sea-ice break-up. The FPGA provides hardware acceleration for increased onboard processing capability than previously demonstrated in software.

The original C-language program — demonstrated on an imaging instrument aboard the Earth Observing-1 (EO-1) satellite — implements a linear-kernel SVM algorithm for classifying parts of the images as snow, water, ice, land, or cloud or unclassified. Current onboard processors, such as on EO-1, have limited computing power, extremely limited active storage capability and are no longer considered state-of-the-art. Using commercially available software

that translates C-language programs into hardware description language (HDL) files, the legacy C-language program, and two newly formulated programs for a more capable expanded-linear-kernel and a more accurate polynomial-kernel SVM algorithm, have been implemented in the Virtex-4FX FPGA. In tests, the FPGA implementations have exhibited significant speedups over conventional software implementations running on general-purpose hardware.

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SiC JFET Transistor Circuit Model for Extreme Temperature Range Simple modifications of common silicon model provide reasonable approximation from 25 to 500 °C.

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A technique for simulating extreme-temperature operation of integrated circuits that incorporate silicon carbide (SiC) junction field-effect transistors (JFETs) has been developed. The technique involves modification of NGSPICE, which is an open-source version of the popular Simulation Program

with Integrated Circuit Emphasis (SPICE) general-purpose analog-integrated-circuit-simulating software. NGSPICE in its unmodified form is used for simulating and designing circuits made from silicon-based transistors that operate at or near room temperature.

Two rapid modifications of NGSPICE

source code enable SiC JFETs to be simulated to 500 °C using the well-known "Level 1" model for silicon metal oxide semiconductor field-effect transistors (MOSFETs). First, the default value of the MOSFET surface potential must be changed. In the unmodified source code, this parameter has a value of 0.6,