TID and SEE Response of an Advanced Samsung 4G NAND Flash Memory

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Abstract

Initial total ionizing dose (TID) and single event heavy ion test results are presented for an unhardened commercial flash memory, fabricated with 63 nm technology. Results are that the parts survive to a TID of nearly 200 krad (SiO_2), with a tractable soft error rate of about 10^{-12} errors/bit-day, for the Adams Ten Percent Worst Case Environment.

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To be presented at the IEEE Nuclear and Space Radiation Effects Conference (NSREC), July 23-27, 2007 and to be published in the IEEE Transaction on Nuclear Science, Dec. 2007 and on http://rahome.gsfc.nasa.gov

Introduction

In recent years, flash memory, and especially NAND flash memory, has been the fastest growing segment of the semiconductor industry, both in terms of market share and actual sales. This is primarily due to the fact that NAND flash is used extensively in mobile, hand-held consumer electronics, such as cell phones, iPods™, and digital cameras, which are all rapidly growing markets. Flash is nonvolatile, meaning that it maintains stored information, even with no power, which also means that it is extremely low in power consumption most of the time – an obvious advantage in a battery-driven system. NAND flash has a serial organization, which allows a higher bit density than the alternative NOR architecture, and, therefore a lower cost per bit. This is an obvious advantage to manufacturers trying to squeeze every possible dollar out of the price of high volume consumer items. The same features that make flash attractive commercially also make it attractive for space systems—nonvolatile, low power, low cost, low weight, etc. However, for a space system, one also has to consider the radiation response of a flash memory.

This poster presents radiation response for both TID and single event effects (SEE) for a Samsung 4G (512Mx8) NAND flash. This was the first 63 nm flash product available in the market. We note that, according to the Samsung website, Samsung currently holds 31% of the total memory market, 30% of the total flash market, and 61% of the NAND flash market. Samsung also claims to have held the number one position in each of these market segments for several years. Therefore, this is an important product, commercially.

Description of Samples

The device under test (DUT) is a 4G NAND flash (part number K9F4G08U0A), which operates at 3.3 V, nominal, within the allowed range 2.7-3.6 V. These parts are single level cells (SLC). The parts have a single power supply, which means there is an on-chip charge pump to produce the higher voltages needed to write and erase. The parts have 4096 blocks, of which up to 80 can be "bad" initially—the manufacturer identifies the bad blocks, so that they can be screened out. In our samples, all had a few bad blocks, but none came close to 80. Within each block, the organization was 128Kx8, with 64 pages per block, each 2Kx8. Maximum operating frequency is 40 MHz.

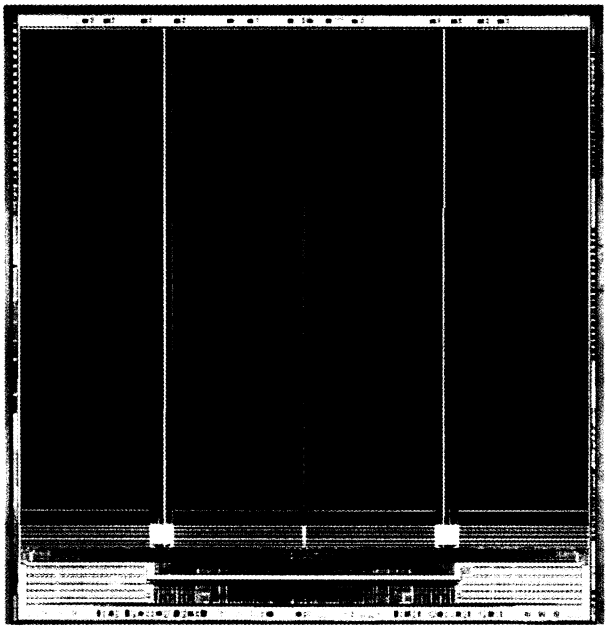

Figure 1. Picture of Samsung K9F4G08U0A chip.

Experimental Procedure

TID testing was at the Co-60 Radiation Effects Facility (REF) at NASA/GSFC. This is a room air source, where the pencils are raised up out of the floor, during exposures. Active dosimetry was performed, using air ionization probes. Testing was done in a step/stress manner, using a standard Pb/Al filter box. Dose rate typically varies slightly from one exposure to the next, up to 30 rads(SiO_2)/s. Exposures to the NAND flash were near the maximum dose rate, as required by MIL-STD Test Method 1019.7. Time intervals for testing between exposures are also within the limits stated in 1019.7 (one hour after exposure to start electrical characterization, two hours to begin the next exposure). Parts were under DC bias during exposures, but not actively exercised. Eight test devices were programmed with a checkerboard pattern (AA) during exposures, and biased at 3.6 V (3.3 V nominal power supply, plus 10%). Four parts were read (only) between exposures, to look for problems related to the integrity of the individual bits. The other four parts were exercised between exposures—read, erased, and written into four different patterns. The patterns were checkerboard (AA), checkerboard complement (55), all ones, and all zeroes. In each of these tests, the entire memory is read, or erased, or programmed in one operation, with the commands entered manually. There was also a dynamic test mode, where each block was read, erased, and programmed, then the next block, and so on until the entire memory was completed.

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Table I: Ions/Energies and LETs for this test.

LBNL Ions	**Energy (MeV)**	**Effective LET (MeV•cm^2/mg) (Normal Incidence)**
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1) Static/Unbiased irradiation, in which a pattern was written and verified, and then bias was removed from the part and the part was irradiated. Once the irradiation reached the desired fluence, it was stopped, bias was restored, and the memory contents were read and errors tallied.
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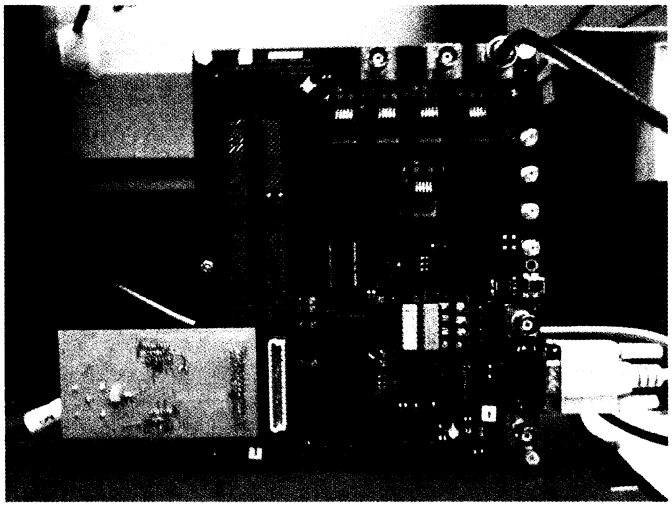
3) Dynamic Read, in which a pattern was written to memory and verified, then subsequently read continuously during irradiation. This condition allows determination of functional, configuration and hard errors, as well as bit errors.

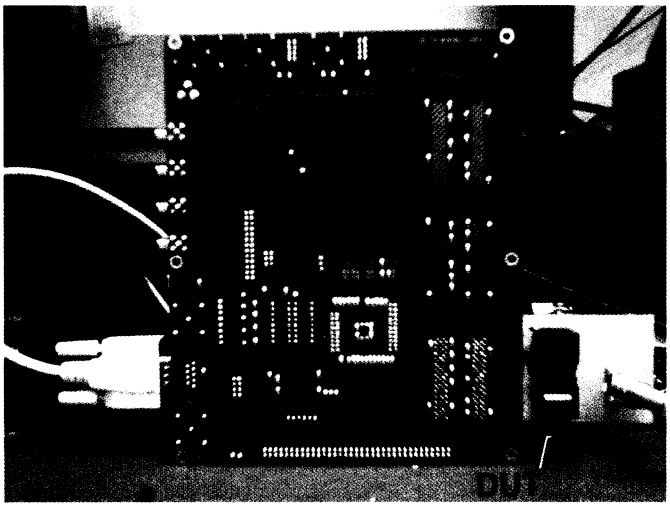
4) Dynamic Read/Write, which was similar to the Dynamic Read, except that a write operation is performed on each word found to be in error during the previous Read.

5) Dynamic Read/Erase/Write, which again was similar to the Dynamic Read and Read/Write, except that a word in error was first erased and then rewritten. Because the Erase and Write operations use the charge pump, it is expected that the Flash could be more vulnerable to destructive conditions during these operations.

The test boards, both motherboard and daughter board, are shown front and back in Figure 2.



(a)



(b)

Figure 2. Pictures of test board. (a) front of mother board, (b) front of daughter board, showing DUT.

Results

In the TID test, eight parts were tested along with an unirradiated control sample. DUTs 1-4 were tested in read-only mode, while DUTs 5-8 were exercised in all the test patterns and the dynamic mode, as described above. All the DUTs had some bad blocks, initially. At the 10, 20, and 30, 50, 75, and 100 krad (SiO_2) exposure levels, there were no errors in any device, in any test mode, except those identified in the bad blocks prior to irradiation, with three exceptions. First, DUT 5, after 75 krads(SiO_2), had three errors which were reset successfully, and which did not repeat in the next exposure. DUT 5 failed between 100 and 125 krads(SiO_2), due to failure of the erase circuit. Second, three of the read-only DUTs had errors after 75 krads(SiO_2). These were reset successfully and did not recur. Starting at 75 krads (SiO_2), the DUTs that were testedwith the dynamic mode had errors, but only in that test mode. We will discuss these errors further, below. The other seven devices had no new errors at 125 or 150 krads(SiO_2), but they all failed at 200 krads(SiO_2). The DUTs that were cycled passed the initial read test, but they could not be erased. The r DUTs 1-4 that were read only had an increase in the number of pre-rad errors. When we tried to reset these, the erase operation also failed. Leakage current was monitored throughout the test. Total current during exposure was 30 mA initially, for all eight samples, or an average of about 4 mA each. This current level, 4 mA per device, was confirmed for each device, when they were tested individually. At the end of the test, when the devices failed, leakage current had not increased for any device. In the dynamic mode, errors were detected, but only in block zero. These parts all had a few bad blocks pre-rad, which had to be screened out. If one more block, block zero, were screened out, it would appear to be a simple work-around for this problem.

For the heavy ion SEE test, static error cross section results are shown in Figure 3.

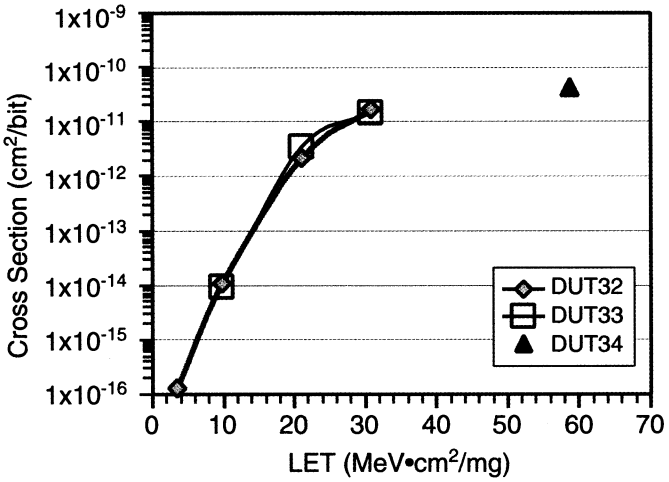


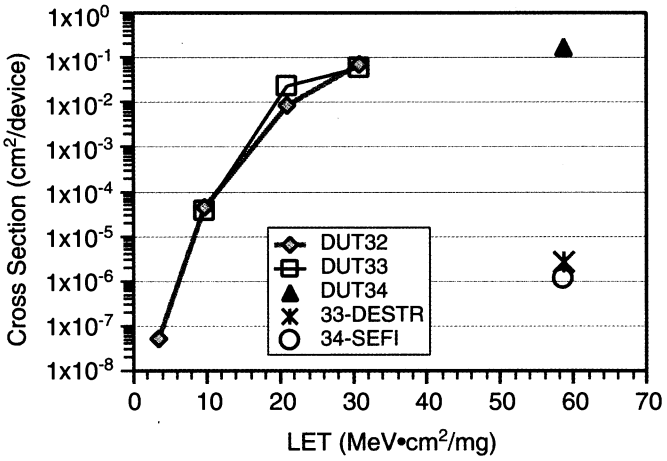
Figure 3: Error cross-sections observed in static testing.

The results in Figure 3 were fitted with Weibull parameters, threshold LET=3.5, saturation cross section=5E-11 cm^2/bit, width=27, exponent=5, and Creme96 was used to calculate the bit error rate for geosynchronous orbit at solar minimum. The result was 1E-12 errors/bit-day, which is equivalent to about 1.5 bit errors per year for a 4G, from heavy ions. The proton contribution would increase this rate if included. The data in Figure 3 is normalized per bit, but the same data is normalized per device in Figure 4, so that the SEFI and destructive effects can be shown on the same scale. Obviously, the SEFI and destructive error cross sections are orders of magnitude less than the bit upset cross section, and the error rate expected in space will scale with the cross section. However, we have not calculated this error rate, because there are so few SEFI or destructive events that there is large statistical uncertainty associated with

them. Most of the SEFIs are page errors or block errors, where an entire page or block was detected as being in error. These errors could be corrected by resetting the DUT.

For the dynamic test modes, results for bit errors are qualitatively similar to those in Figure 3, but the error rate is marginally higher for the dynamic read test, because the incident ions also generate transient noise in the read circuits, in addition to flipping bits. Dynamic read results are shown in Figure 5.

When dynamic write and/or erase operations are performed, some errors are reset before they are detected, which tends to offset the increased errors observed in the dynamic read-only test. Dynamic Read/Write results are shown in Figure 6, and Dynamic Read/Write/Erase/Read results are shown in Figure 7.



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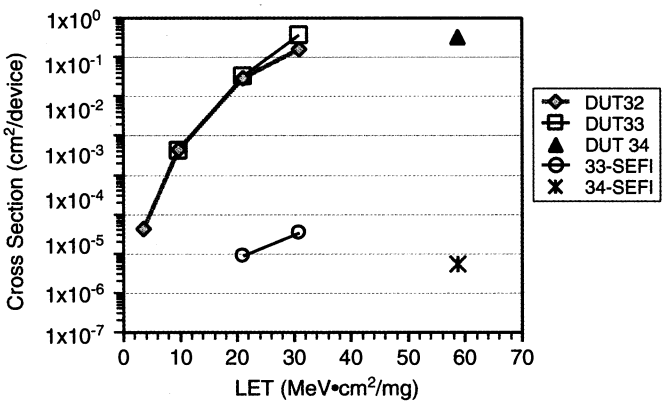

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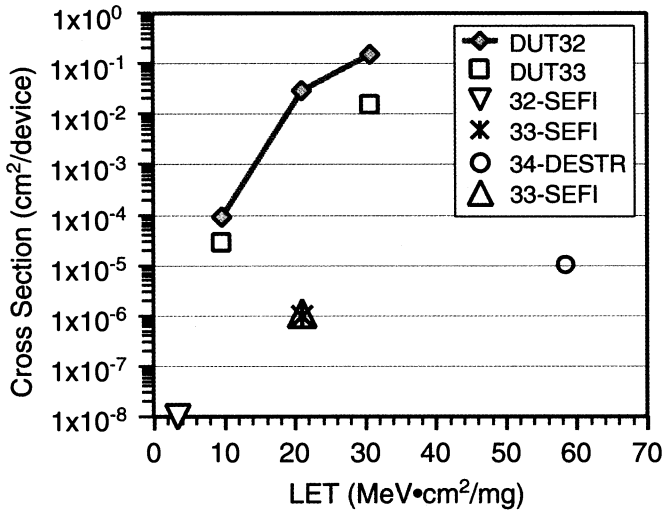

Figure 6: Error cross sections observed in dynamic read/write testing.

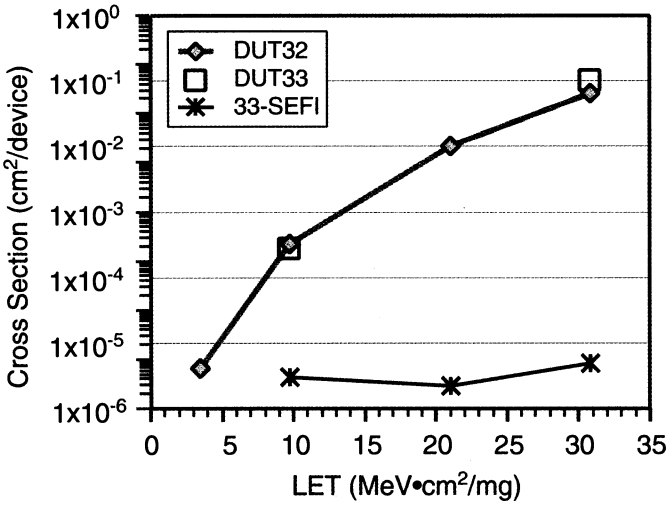

Figure 7: Error cross sections observed in dynamic Read/Write/Erase testing.

However, the SEFI rate is higher during the high-voltage read and write operations. Most of the SEFIs are either page errors or block errors. In these cases, an entire page (2Kx8), or a large part of one will be detected as simultaneous errors. A block error is similar, only bigger (128Kx8). These errors are thought to be due to an ion upsetting a configuration register. A number of these errors were observed, but they were nondestructive.

The parts were tested for latchup at 70° C, and 3.6 V. High temperature and high voltage are worst-case conditions for latchup, and 70° C is the maximum rated operating temperature for these parts. Nominal voltage plus 10% is 3.6 V, which is also the maximum rated voltage for these parts. No latchup was observed in any exposure. However, there were high current excursions in some shots that might be taken for latchup – an example is shown in Figure 8. The current goes up enough to possible trigger a latch detection circuit (if we had been using one), but then the DUT corrects itself. This kind of result suggests a localized micro-latch or some kind of bus contention or SEFI, rather than a full SEL condition. A generalized SEL condition would not be expected to correct itself, as obviously happens in Figure 8. For the shot illustrated in Figure 5, there was a SEFI, which was corrected with a DUT reset.

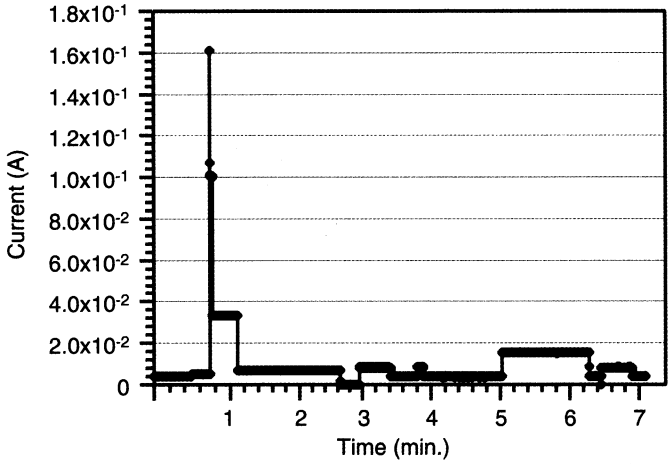

Figure 8. Power supply current during one exposure, with SEFI.

Conclusions

The Samsung 4G, part number K9F4G08U0A, has been tested for TID and SEE effects. Total dose response is that parts all survived past 100 krad (SiO_2) and most survived almost to 200 krad (SiO_2). These levels are suitable for many space systems. The SEE error rate is projected to be quite low when compared to most competing commercial technologies.

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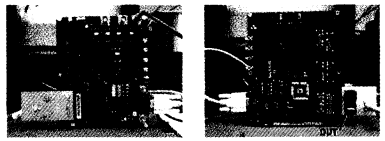

(a) (b)

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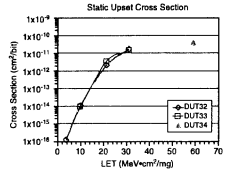

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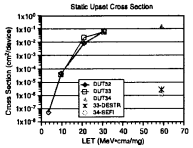

Figure 4. Measured static error cross section.

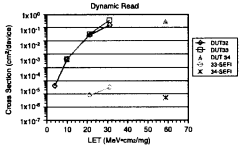

Figure 5: Dynamic read upset cross section.

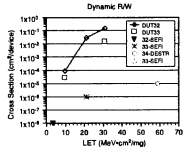

Figure 6: Error cross sections observed in dynamic read/write testing.

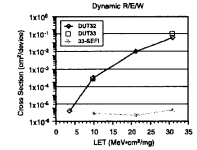

Figure 7: Error cross sections observed in dynamic Read/Erase/Write testing.

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The parts were tested for latchup at 70° C, and 3.6 V. High temperature and high voltage are worst-case conditions for latchup, and 70° C is the maximum rated operating temperature for these parts. Nominal voltage plus 10% is 3.6 V, which is also the maximum rated voltage for these parts. No SEL was observed in any exposure. However, there were anomalous high current excursions in some shots that might be taken for SEL - an example is shown in Figure 8. The current goes up enough to possible trigger a latch detection circuit (if we had been using one), but then the DUT corrects itself. This kind of result suggests a localized micro-latch or some kind of bus contention or SEFI, rather than a full SEL condition. A generalized SEL condition would not be expected to correct itself, as obviously happens in Figure 8. For the shot illustrated in Figure 8, there was a SEFI (detected by reading after the exposure), which was corrected with a DUT reset.

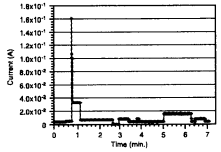

Figure 8. Power supply current during one exposure, with anomalous high current excursion. SEFI was detected after exposure.

Conclusions

The Samsung 4Gb part number K9F4G08U0A has been tested for TID and SEE effects. Total dose response is that parts all survived past 100 krad (SiO_2) and most survived almost to 200 krad (SiO_2). These levels are suitable for many space systems. The SEE error rate is projected to be quite low when compared to most competing commercial technologies.

Acknowledgment

The Authors gratefully acknowledge the sponsors of this effort: NASA Electronic Parts and Packaging Program (NEPP) and the Defense Threat Reduction Agency (DTRA) under IACRO# 07-42071.

Poster layup for presentation at NSREC07 Data Workshop