Developments in Radiation-Hardened Electronics Applicable to the Vision for Space Exploration

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The Radiation Hardened Electronics for Space Exploration (RHESE) project develops the advanced technologies required to produce radiation hardened electronics, processors, and devices in support of the anticipated requirements of NASA's Constellation program. Methods of protecting and hardening electronics against the encountered space environment are discussed. Critical stages of a spaceflight mission that are vulnerable to radiation-induced interruptions or failures are identified. Solutions to mitigating the risk of radiation events are proposed through the infusion of RHESE technology products and deliverables into the Constellation program's spacecraft designs.

Nomenclature

°C = Temperature (degrees Celsius)

I. Introduction

NASA has embarked on a new initiative that is designed to return humans to the lunar surface and to subsequently establish a lunar infrastructure that will enable sustained human presence there. This lunar exploration effort is performed in preparation for human exploration of Mars and potentially other Solar System destinations. Known as the Vision for Space Exploration[1] (VSE), this endeavor has as its fundamental goal the advancement of scientific, security, and economic interests within the United States of America through a robust space exploration program. To fulfill the VSE, NASA must not only invest in the flight vehicles required to return man to the moon, but must also invest in the advanced technologies and capabilities required to enable these flight vehicles and their missions.

The Radiation-Hardened Electronics for Space Exploration (RHESE) project is one of many technology development projects within the Exploration Technology Development Program (ETDP). The ETDP supports a wide array of technology development efforts needed for accomplishing the goals of the VSE. The RHESE project

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is managed by NASA's Marshall Space Flight Center (MSFC), while the ETDP is managed by NASA's Langley Research Center (LaRC).

RHESE endeavors to advance the current state-of-the-art in radiation hardened electronics by developing high performance devices robust enough to withstand the extreme radiation and temperature levels encountered within the space and lunar environments. The primary customers of RHESE technologies will be the flight projects being developed in fulfillment of the goals of the VSE. Collectively known as NASA's Constellation program, these flight projects include the Orion Crew Exploration Vehicle, the Ares V Crew Launch Vehicle, the Lunar Lander project, the Lunar Outpost project, and the Extra-Vehicular Activity (EVA) hardware required for Personal Life Support Systems. Secondary customers for RHESE technologies include NASA science missions, collaborative efforts with other agencies of the US Government, and commercial applications.

II. Radiation Hardening for the Space Environment

It has long been known that the space environment poses a particular radiation hazard to both organic and inorganic materials. In general, the high energy particles that constitute the radiation hazard within the space environment originate from three sources[2]:

- Proton and electron radiation trapped within the Earth's magnetic field,
- Solar coronal mass ejections,
- Galactic cosmic rays (GCRs).

The high energy particles encountered in the space environment typically possess energies that range from the lower level of less than one MeV as possessed by particles in the Earth's radiation belts to beyond the predicted upper limit of ~$5x10^{19}$ MeV (known as the Greisen-Zatsepin-Kuzmin (GZK) limit[3,4]) as inexplicably possessed by extremely energetic galactic cosmic rays. At these energies, the particles are capable of passing deep into, and in some cases completely through, the encountered material, causing localized ionization and occasional atomic displacement. Because electronics operate based on the principle of controlled carrier diffusion within the semiconductor material, the flood of ions produced by a localized passing of a single high energy particle easily causes the electronic device to perform unpredictably. This occurrence is generally known as a Single Event Effect (SEE).

Though sources of space radiation are well understood and characterized, the problem still remains of how to protect the spacecraft, its occupants, and its electronics from the deleterious effects experienced when encountering space radiation. Multiple solutions exist that provide some level of protection from space radiation. The most basic solution is the matter of shielding the radiation-sensitive portions of the spacecraft with additional material. By including additional material around the component to be protected, there is a much greater chance that the high energy particle will be stopped via its interaction with the shielding material prior to reaching the component. The obvious problem with using shielding on a spacecraft is the mass penalty paid when attempting to place the entire system in orbit. One interesting approach to shielding includes the strategy for a manned mission to carry the potable and waste water in locations that provide maximal radiation shielding[5] - thus serving two purposes. It should also be realized that shielding will protect from lower energy particles, but higher energy particles may penetrate the shielding regardless of its practical thickness.

Another consideration in protecting a spacecraft from radiation damage includes the aspect of mission design. If it is possible to select a mission profile that minimizes the exposure of a spacecraft to the environmental radiation and damage from thermal conditions, then this should be included in the mission design trade space. As an example, if a spacecraft's orbit can be placed such that it minimizes its encounters with the trapped radiation of Earth's radiation belts, then this should be considered as a factor in the design trade space. By a similar argument, if a lunar landing location may be selected such that it minimizes direct exposure to the sun by allowing the landing site to spend half a lunar orbit with the lunar body acting as a shield from potential solar particles, then this too should be considered. However, this trade must be made against the benefits of solar exposure to power generation systems and thermal regulation considerations.

Another approach to providing operational assurance is the process of designing critical systems to include redundant electronic strings of components, thereby reducing the change that space radiation will cause adverse effects in the final expected performance of the system. The spacecraft designer may choose to implement triple module redundancy (TMR) within the logic circuits of the flight electronic component[6]. This approach involves using three strings of logic circuitry that all feed a voting string of logic circuitry. Between the three voting circuits, the majority digital state is forwarded as the solution while the minority digital state is discarded. The practice of TMR may be extended beyond the digital circuitry level to including multiple components, processors[7], and even subsystems[8] that feed an overlying layer of voting logic to determine the majority answer. This approach to

radiation hardening can be loosely identified as Radiation Hardening by Architecture (RHBA). One could argue in an extreme case of redundant system engineering that multiple and totally redundant spacecraft would statistically improve the chances of mission success[9]. However, in the case of manned missions, there are no redundant crews. Even in the case of an unmanned mission, redundant spacecraft are expensive. The process of assembly, verification and validation of flight hardware, launch services, and operations, could nearly double a mission's cost.

Radiation Hardening By Design (RHBD) is the next level of hardening of electronic components. RHBD implies that an electronic part or board has been radiation-hardened by virtue of the component layout and circuit architecture of on-chip gates, devices, and interconnects independent of any special fabrication process or technique. Examples of RHBD techniques include using TMR strategies within the chip layout, designing dopant wells and isolation trenches into the chip layout, implementing error detecting and correction circuits[10], and device spacing and decoupling. Disadvantages to these techniques include the extra devices required to implement TMR, the extra power load these devices consume, and the extra chip area required to isolate devices, gates, and latches.

Radiation Hardening By Process (RHBP) is the final and lowest level of hardening where the actual electronic transistor components of the electronic device have been fabricated with process techniques that temper the component against a SEE radiation event. Material selection, insulation layers, doping levels, and proprietary processing steps are a part of RHBP. Unfortunately, this is an expensive method for radiation hardening as the process that hardens the part is dependent on dedicated foundry lines and part runs. The market for radiation hardened devices is very limited and the expense of developing a new component using a RHBP usually does not justify the effort – particularly when the part is customized for a spacecraft application where a run of approximately ten to twenty parts would completely satisfy the spacecraft's test and assembly needs. Because of the expense and special foundry requirements to produce electronics that utilize RHBP techniques, the capabilities of these RHBP radiation-hardened electronics (power consumption, processor speed, feature size, etc.) tends to lag the commercial electronics capabilities by a decade or more.

Of course, the spacecraft designer has the option of implementing any or all of these radiation damage mitigation techniques in any combination. Depending on the criticality, value, and acceptable risk associated with the mission being developed, the specified hardness of the onboard electronics may range from commercial-grade parts arranged with no redundancy under minimal shielding to parts that are radiation hardened via RHBP techniques running in a TMR voting configuration under heavy localized material shielding. It is therefore obvious that the process of developing a flight system, complete with modern electronics and avionics, capable of continual operation within the extreme environments of space, is not a trivial task.

III. Constellation Customer Requirements and Needs

Developers of the projects comprising NASA's Constellation program must define the trade space associated with the required hardness of the avionics and electronics that will eventually return humans to the moon. In fact, so critical is this process to NASA's success in spaceflight that spacecraft developers have defined a Radiation Hardness Assurance (RHA) methodology process[11]. In general, the process may be described by the following steps:

1) define the radiation hazard,
2) evaluate the hazard,
3) define the requirements to be met by the spacecraft's electronics,
4) evaluate the electronics to be used,
5) engineer processes to mitigate hazard damage, and
6) iterate on the methodology, if and when necessary.

To promote the successful implementation of RHA for NASA missions, the RHESE project aims to deliver products that assist in mitigating the hazard damage. However, it is not acceptable to wait until all requirements have been established before this task is undertaken. The RHESE project is therefore supplementing the known requirements of the Constellation Program with derived requirements of electronic performance and capability metrics based on multiple inputs, including architecture studies, working group discussions, interchange discussions, and RHESE team-resident knowledge of system and architecture objectives. These project-level capabilities drive the goals of the RHESE project tasks and are listed in Table 1.

Not all of the listed capabilities and performance parameters will be applicable to all RHESE project tasks. But they do provide a metric for measuring the maturity of a particular technology. Measuring the performance value through test provides a method of determining the Technology Readiness Level (TRL)[12]. TRL levels are discussed further in Section IV of this paper.

Table 1. Key Performance Parameters for RHESE Technology Development Tasks

Key Performance Parameters	Units	Threshold Value	Goal Value	TRL
Total Ionizing Dose (TID)	Mrad	0.1 (Si)	0.3 (Si)	6
Single Event Upset Rate	errors/bit-day	1.00E-12	1.00E-13	6
Single Event Latch-Up Threshold	MeV-cm^2/mg	100	Immune	6
Sustained Processor Performance	MIPS	500	3000	6
Sustained Processor Efficiency	MIPS/W	500	2000	6
Speed of Dynamic Reconfiguration	sec	1	1.00E-03	6
Temperature Range	C	-180	-230	6
Redundancy and Reconfigurability	Levels of Reconfigurability	3	4	6
Radiation Model Accuracy	Number of Technologies Included	2	4	6
Storage Density	GB/cm^2	1	100	6
Storage Efficiency	%	95	100	6

The following examples of Constellation program mission concepts exemplify the need for advanced radiation-hardened electronics and processors. The examples are primary drivers of the derived requirements and key performance parameters defined for RHESE in Table 1.

A. Autonomous Landing and Hazard Avoidance

Exploration missions will be required to deploy resources to execute or sustain missions at lunar or Martian sites. Although numerous vision system options exist, all of the systems require computationally-intensive routines such as map matching and real-time feature tracking. The ability to implement autonomous landing and hazard avoidance technology (ALHAT) and the resultant precision with which resources are deployed to the lunar surface is directly affected by the performance of the data processor. Designers have expressed concerns that the currently available state-of-the-art radiation-hardened processors may not have sufficient processing speeds for appropriately hosting and running the vision system-based hazard avoidance algorithms. And because of the critical nature of landing resources, commercial or "soft" processors are not acceptable solutions.

B. Autonomous Vehicle Operations

Exploration requirements document the need for autonomous vehicle operations. Round-trip signal times between ground controllers and any unmanned rovers would create real-time navigation delays and inefficient operations. This paradigm requires autonomous surface systems capable of independently navigating unknown terrain, recording the terrain observation, and storing the information for future playback. Processors with increased capabilities are accordingly needed to implement these requirements. RHESE deliverables will increase the performance of capabilities required for autonomous surface mobility, such as rover stereo vision, hazard avoidance, and path planning.

C. Critical Mission Stages

Certain stages of a spaceflight mission are extremely critical in their execution and timing. Examples include launch sequences, course trajectory correction firings, and entry, decent and landing sequences. An untimely radiaiton event striking a critical electronic part could cause an entire mission to fail should the event occur during one of the critical mission stages. Designers of the Constellation projects must consider the risks of such an event occuring and the mitigation of the risk through the use of radiation-hardened parts and radiation hardened assurance methodologies.

D. Distributed System Architectures within long duration, extreme radiation

When developing the avionics and electronics for surface systems designed to endure harsh environments, the current method of protecting the electronics is to cocoon them in a heated and insulated "warm box" central to the system's architecture. From this box, primary and redundant cabling is strung between the control electronics and all sensors, cameras, detectors, motors, actuators, and other components located at the extremities of the system architecture. This design limits the ability to create a truly distributed, modular electronics system, resulting in excessive point-to-point wiring, increased system weight, increased system complexity, and reduced reliability. This problem is anticipated to grow more challenging as larger more complex rovers are developed.

RHESE proactively responds to these anticipated Constellation mission concepts by formulating the development of advanced materials, processors, reconfigurable computers, and models of the effects radiation produces within modern electronics. The following section summarizes these RHESE technology development products.

IV. RHESE Project Overview

In response to the Constellation Program's anticipated requirement for radiation-hardened electronics, the ETDP office established the RHESE project. RHESE provides a broad-scoped approach to providing hardened space electronics. Investment areas include new materials, design processes, reconfigurable hardware techniques, and software techniques. Near-term emphasis within the multiple RHESE tasks focuses on hardening Field Programmable Gate Arrays (FPGA)s for use in reconfigurable architectures and on developing electronic components using semiconductor materials (such as Silicon Germanium (SiGe)) to enhance a devices tolerance to radiation events and low temperature environments. As these technologies mature, the project shifts its focus to efforts encompassing total processor hardening techniques. This phased approach to distributing emphasis between technology developments allows RHESE to provide hardened FPGA devices and environmentally hardened electronic units for mission infusion into early Constellation projects such as the Orion Crew Exploration Vehicle and the Ares V Launch Vehicle. Once these technologies begin the infusion process, the RHESE project then shifts its technology development focus to hardened, high speed processors with associated memory elements and high density storage for the longer duration missions, such as the Lunar Lander, the Lunar Outpost, and eventual Mars Exploration missions occurring later in the Constellation schedule.

To ensure any new advanced technology being developed for use on a flight vehicle is sufficiently mature, NASA employs a technology rating standard - known to technologists as the Technology Readiness Level (TRL) scale - to assist with the assessment of a technology's maturation and test. Figure 1 shows the standard definitions NASA uses to rate a technology's TRL. By meeting the requirements of each level within the TRL scale, a technology advances in rank and maturity until it is ready for flight. The ETDP fosters the development of advanced

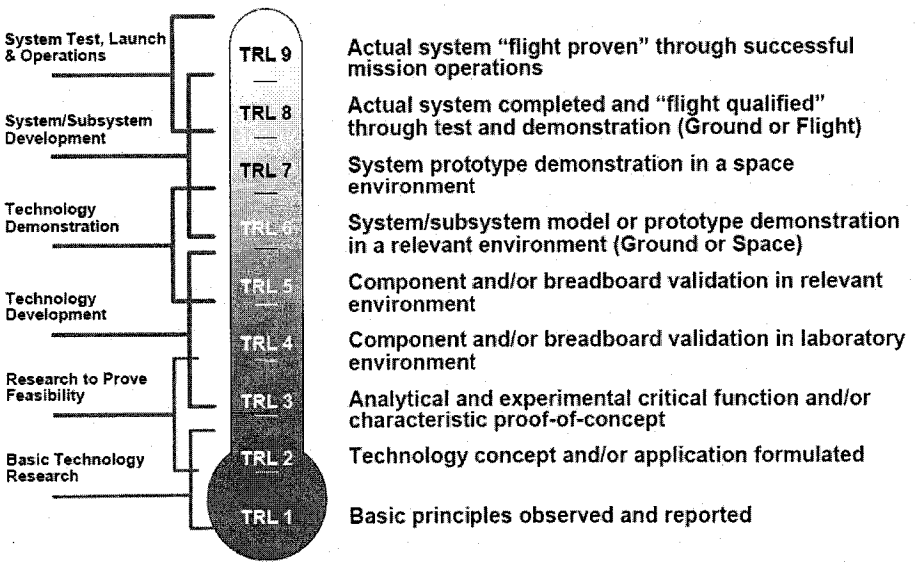

Figure 1. Technology Readiness Level Definitions.

technologies through the TRL 6 level. Once this level of maturity is attained, the technology is "graduated" to be infused into a flight project where it continues to mature through the TRL 9 level. RHESE complies with the technology maturity approach in that all of the products developed under the RHESE project have goals of TRL 6 maturity prior to delivery to an application.

The tasks within RHESE are broad-based and diverse. They collectively include the development of: total dose radiation tolerant electronics, Single Event Upset (SEU)-tolerant electronics, latch-up tolerant electronics, high performance processors, low temperature electronics, reconfigurable robust electronics, and updated models capable of predicting the effects of radiation on electronics. Specifically, the RHESE tasks are:

- Model of Radiation Effects on Electronics (MREE),
- Single Event Effects (SEE) Immune Reconfigurable Field Programmable Gate Array (FPGA) (SIRF),
- Radiation Hardened High Performance Processors (HPP),
- Reconfigurable Computing (RC),
- Silicon-Germanium (SiGe) Integrated Electronics for Extreme Environments.

Each of these tasks will be summarized in the following sections.

A. Model of Radiation Effects on Electronics (MREE)

RHESE's MREE task is focused on developing an updated model of radiation effects on electronics. The previously used model, CREME96[13], has been for years the industry standard modeling tool for radiation effects on electronics. However, over the past eleven years since its release, the state-of-the-art in microelectronics has continued to advance toward architectures that incorporate smaller feature sizes, multilayered electronic structures, and metals containing heavy elements – all of which make today's modern electronic architectures more susceptible to radiation damage. Because the CREME96 model is deficient in accounting for an increasing number of features common to modern electronic architectures, the MREE task is developing an update to this model.

The new model being developed is critically needed to guide the selection of modern radiation hard components for use in space systems. Designers will employ this updated model to predict the mean-time-between-failure (MTBF) of their circuit designs when they choose to use state-of-the-art commercial grade or radiation hardened parts. This modeling effort will also develop a tool designed to estimate the frequency of the various single event effects such as logic upsets and circuit latch-up as well as the total radiation dose effects in microelectronic devices operated in the space environment.

The modeling tool will possess the additional feature of being capable of considering the vehicle's exact structure for purposes of calculating the shielding effect provided when assessing the susceptibility of a particular microelectronic circuit to high energy particle radiation. This approach also allows the exact physical structure of the microelectronic circuit and the exact pattern of hole-electron creation within that circuit structure to be taken into account so that the resulting charges and currents within the circuit can be determined accurately. The model employs a Monte Carlo method of simulation to evaluate the electronic architecture under radiation conditions. These codes will propagate individual particles, selected at random from the external particle environment striking the spacecraft, to the chip. During propagation the effects of nuclear interactions and energy loss by ionization will be taken into account. By propagating a large sample of particles from the external environment though the vehicle and the device under evaluation, the model makes an estimate of the device's accumulated total dose and the single event rate probability, all while considering the device's location within the space vehicle under any external environment model and in any orbit that is chosen.

The MREE task is jointly developed by NASA's Marshall Space Flight Center and Vanderbilt University. MSFC provides the models for the radiation environments to be used for the estimation of single event effects and total dose under various space weather conditions. MSFC also provides Monte Carlo computer code to propagate the external radiation environment through the actual design of the spacecraft structure to the microelectronic chip that is being investigated. The result will be a list of individual particle descriptions and coordinates at the chip which are fed into the code generated by Vanderbilt University. These particle lists will also be used to predict the total radiation dose to the electronics.

Vanderbilt University models the physical structure of the microelectronic circuit within the semiconductor material of the chip and propagates the individual particles from the list prepared by MSFC through the device structure. The Vanderbilt code will account for nuclear reactions, energy loss and hole-electron pair creation within and nearby the microelectronic circuit components. Vanderbilt will also develop classes to track the collection of charge onto the nodes of the microcircuit from the distribution of hole-electron pairs created by the ionizing particle. There will also be code that examines how the circuit responds both to the charges collected on various nodes and to

the currents resulting from the rates of charge collection at various points in the circuit. In particular, there will be code that predicts whether the passage of the charged particle through the chip leads to any single event effects.

Finally, just as the model's predecessors, CREME96, and CREME86 before that, were all available for use on the internet, so will this model be available. Anticipated release of the first version of the MREE tool is in 2009.

B. Single Event Effects (SEE)-Immune Reconfigurable Field Programmable Gate Array (FPGA) (SIRF)

The FPGA is an electronic component that has experienced widespread usage in multiple applications due to its ease of programmability. Because the FPGA can be customized, it is also an inexpensive, and therefore attractive, alternative to the design and development of a non-programmable, hardwired application-specific integrated circuit (ASIC). FPGAs are available in multiple architectures. The most common is the SRAM-based FPGA, which is reprogrammable within an active system to perform a large variety of functions. But they are much like volatile memory in that they require reconfiguration after each power cycle. Also, due to their CMOS-based architecture, they are susceptible to radiation events. Antifuse FPGAs solve the volatility and radiation susceptibility problem by allowing a single configuration to be permanently programmed onto the device. The nature of the antifuse architecture makes it intrinsically radiation-hardened, but the main disadvantage of this architecture is that it can only be programmed once prior to use.

In an effort to address the radiation hardness of a SRAM-based FPGA, the RHESE project is teaming with multiple government and industry partners to support the development of a radiation-tolerant version of the Xilinx Vertex-5 FPGA. The resulting device will yield the benefits of reconfigurable hardware without requiring the encumbrances typically required to harden reconfigurable devices to radiation effects, such as chip area, speed, power, and complexity. SIRF FPGAs can be used to implement systems that incorporate radiation-tolerant reconfigurable interfaces and digital interconnects. This capability will facilitate design of common 'plug-and-play' modular, adaptive and reconfigurable subsystems. Such subsystems can be field programmed and reprogrammed to implement multiple functions in diverse systems.

A SIRF-based processor board could, for example, be removed from a lunar storage depot and inserted into a rover navigation system. Upon insertion, the board will autonomously download configuration data, configure its electrical interfaces and internal interconnects, and execute the desired functionality. It will also continuously monitor its performance and self-reconfigure to mitigate faults, should they occur.

The same board can, should the need arise, be removed from the rover and be used to replace a malfunctioning board in an oxygen generating system. Once inserted, it will be autonomously configured for this application. Significant systems efficiencies including development, fault-tolerance, maintenance, repair, and inventory control will result from this capability.

In addition, SIRF-based technologies can be used for high-bandwidth sensor back-end applications, e.g. vision processing, radar and LIDAR, since gate array-based processors demonstrate significant performance advantages over serial processors when implementing tasks that can be parallelized. SIRF will have the additional advantage of being able to realize this performance advantage without the inefficiencies associated with single-event effect mitigation techniques.

Though the effort is primarily supported by the SIRF task partners, NASA will provide complimentary analysis of these technologies to determine applicability to future space systems. NASA's Goddard Space Flight Center is responsible for managing NASA's involvement in the SIRF task.

C. High Performance Processors (HPP)

Capabilities that can increase the effectiveness or the efficiency with which Exploration Systems challenges are addressed can be data processing intensive. Among these capabilities are autonomous systems involving spacecraft operations, surface mobility, and hazard avoidance and landing. Whereas numerous systems with these capabilities have been deployed, their requirements and implementations are typically constrained by data processing throughput, power resources, and radiation effects. The RHESE High Performance Processors for Space Environments (HPP) task will expand the capabilities of data processing-intensive spaceflight systems by significantly advancing the sustained throughput and processing efficiency of high-performance radiation-hardened processors.

The performance of processors developed with technologies appropriate for aerospace environments lags that of commercial processors by multiple performance generations. For example, one of the "flagship" radiation-tolerant processors— the RAD750— exhibits a sustained throughput rate that is approximately two-orders of magnitude less than the commercially available Intel Centrino processor, used in many desktop and laptop computers.

Whereas radiation tolerant COTS-based boards that offer increased performance are available, the performance is offered at expense of reduced power efficiency. This HPP task seeks to concurrently advance the state-of-the-art of two metrics (sustained throughput and processing efficiency) of high-performance radiation-hardened processors.

The need for power-efficient high-performance radiation-tolerant processors and the peripheral electronics required to implement functional systems is not unique to NASA; this capability could also benefit commercial aerospace entities and other governmental agencies that require highly-capable spaceflight systems. This task will therefore leverage to the extent practical, relevant external technology- and processor-development projects sponsored by other organizations. Accordingly, important factors in defining and implementing the HPP strategy and implementation are the investment plans of these organizations and cognizance of relevant prior and ongoing NASA investments. The HPP team is address both of these factors.

This effort will be addressed from a system-level perspective; meeting the objectives will require peripheral devices that exhibit performance and environmental characteristics consistent with the processor. This task will therefore also investigate the availability and development status of components required to realize nominal high-performance spaceflight systems architectures.

Although the primary discriminating factors, sustained processor performance, power efficiency, and radiation tolerance, are among the metrics identified in Table 1, an equally important factor is the availability of tools to support the software development flow. A very capable component will not be accepted by the community if its tool flow is considered inadequate. Furthermore, software tools development can be a very expensive endeavor; any significant effort would be beyond the scope of the HPP task.

The deliverables from this task will be validated in realistic system- and architectural-contexts to ensure the projected performance advances can be realized not just at the component level but, most importantly, at a flight system level.

Processor verification plans will ensure the deliverables map to detailed customer requirements. These requirements will address several issues, including performance characteristics, environmental susceptibilities, physical characteristics, and compatibility with targeted software compilers, development systems and operating systems. Management board reviews and peer reviews will be conducted on a regular and as-needed basis to assess compliance with requirements. Each plan will follow a consistent framework but incorporate sufficient flexibility to accommodate the specific tasks associated with the HPP task.

In the end, the task deliverables shall include a high-performance, radiation-hardened general-purpose processor and a high-performance, radiation-hardened special-purpose processor. Not that these specific processors are the only ones required. The task objective may be accomplished with multiple types of processors or processor cores, given the broad range of applications that will require significant processing capability. Targeted classes include high-capability general purpose processors (e.g. a RAD750-type technology), instrument-level general purpose processors (e.g. ColdFire or microcontroller technology), and special purpose processors (e.g. FPGA-resident soft- or hard-core, reconfigurable processor, DSP, host processor/coprocessor).

This task is lead by NASA's Goddard Space Flight Center, with support from Marshall Space Flight Center, Langley Research Center, and the Jet Propulsion Laboratory.

D. Reconfigurable Computing (RC)

The concept of RC offers the promise of new capabilities within any particular plan of exploration that involves multiple complex spacecraft. These new capabilities focus on the reduction of subsystem level flight spares inventories for long-duration missions, adaptability to system failures, and flexibility in connecting components through a variety of data interfaces. The RC task proposes a new paradigm for circuitry to respond to failures other than by redundancy voting schemes alone. This new paradigm will not only better detect failed circuitry, but will accomplish actual repair or replacement of defects, adapting circuitry to accommodate system failures. The paradigm also provides the concept of requiring a single configurable processor to autonomously conform to multiple configurations. Accomplishment of this goal yields a reduction in spares required to be carried on long-duration missions, since a single spare would then fit many processing functions. Such architecture adaptability will provide a great saving in spares volume and weight required by extended duration missions.

Cyclical and/or selective periodic testing will mitigate radiation damage and other commonly-feared failures. Reserve copies of circuitry will be generated and tested in order to bring them online in functional condition without interrupting system tasks. Then, the subsystem to be evaluated will be taken offline and tested with known inputs for known expected outputs in order to isolate possible undesirable response. Provided the subsystem checks out as functionally correct, it can be returned to service, held in reserve for the next cycle of checks, or disassembled so that its circuitry may be returned to overall system reserve. If the subsystem fails verification, the portions of

circuitry causing the failure may be further isolated to mark those parts of the circuitry as defective and return the remainder to reserve, much as blocks of a computer hard disk are marked bad and ignored during future operations.

Life limitations on electronics can be mitigated by these same means. Circuitry which becomes unstable and unreliable after extended active lifetime can be retired and new reserve circuitry powered up and configured into service, thus extending overall lifetime of the system.

Flexibility is also bolstered by reconfigurable computing. Interface reconfiguration can allow a single processor make connections through different networks as needed, providing more options in overall system configuration. This supports vehicle system integrity by allowing processors to be transferred among busses and networks to replace lost functionality, and supports the concept of reduced flight spares required to maintain long duration missions.

Three areas of focus have been identified for the RC task; internal modularity, external modularity, and fault detection and mitigation. The first involves ability of the core processor to emulate any form of computing resource as needed to serve all of the capacities required. The second enables the first by providing a capability to interface resources to any target system, by adapting communication standards, physical and electrical interconnections, and other parameters of the host system to hook up to the computing resource. The final allows the detection of an internal fault and autonomous isolation and recovery from the fault without required external involvement.

Verification of the capabilities produced will be accomplished by two means, both involving testing. First, since exposure to harsh environments will not necessarily guarantee errors, and even supposing errors do result, their nature and behavior cannot be rigorously controlled, it will be necessary to induce known errors. Various means for inducing these errors in a methodical manner, in order to cover the full spectrum of foreseeable malfunctions, will have to be devised. Second, testing in actual environmental chambers will be carried out to simply satisfy the validity of the schemes under harsh conditions representative of planned target flight environments.

Finally, increasingly complex forms of fault identification and response are to be studied and applied; those relying particularly on the strengths of RC itself will allow substitution of tested computing resources for those in line for maintenance to allow removal, testing, and refurbishment of the latter without interruption of system operation.

The RC task plans to have as deliverables the following items:

- Reconfigurable computers supporting multiple architectures to enable single spares to fulfill multiple electronic functions,
- Reconfigurable computers supporting avionics redundancy by providing adaptable spares,
- Reconfigurable computers supporting recovery from component damage by radiation strikes and other events, and
- Reconfigurable computers supporting multiple interfacing and interconnection options.

This task is managed by NASA's Marshall Space Flight Center with support from NASA's Langley Research Center.

E. Silicon-Germanium (SiGe) Integrated Electronics for Extreme Environments

The RHESE SiGe task has as its goal the development and demonstration of extreme environment electronic components required for lunar robotic systems with distributed architecture, using low-cost, commercial SiGe BiCMOS technology[14-18]. The SiGe BiCMOS offers unparalleled low temperature performance, wide temperature capability, and optimal mixed-signal design flexibility at the monolithic level by offering power efficient, high speed devices (SiGe HBTs) and high density Si CMOS.

The approach to implementing this task is to demonstrate system-critical SiGe BiCMOS mixed-signal integrated circuit components capable of operating reliably from -180°C to +120°C while under radiation exposure. In addition to the electronics, the packaging of the developed part is also required to be reliable for the specified temperature range. The SiGe development effort culminates in the development and test of a flight-ready remote electronics unit (REU) system prototype to serve as a general purpose, extreme environment ready, sensors and control interface system-in-package for NASA missions. The planned verification and testing strategy will consist of characterization of the various SiGe mixed-signal components as a function of temperature, from -180°C to 120°C. Tests will also include radiation characterization to a total dose of at least 100 krad, life testing at the temperature extremes (-180°C and 120°C), and over-temperature part and package thermal cycle testing. Additional testing of components at cryogenic temperatures under radiation exposure will be used to evaluate the combined effects of temperature and radiation. When complete, the SiGe task will have matured a critical technology allowing many electronic components and data devices to be mounted such that they are exposed to the extremes of the space environment and no longer require the conditioning provided by the system's warm box.

The contract for this task is managed by NASA's Langley Research Center with support from the Jet Propulsion Laboratory. The Georgia Institute of Technology is the prime contractor and leads a team made of multiple academic and industrial partners.

V. Conclusion

NASA is currently in the process of developing the spacecraft and missions that will fulfill the goals of the VSE, with a primary emphasis on long duration lunar missions. Because of the known radiation hazard within space and on the lunar surface, radiation hardened electronics are anticipated to be required in the avionics and processors flown aboard the spacecraft being developed under the Constellation program. Designers of spacecraft that must face the radiation hazard should follow the methodology of RHA. To successfully implement RHA for the electronic systems on a spacecraft, there are multiple levels of design that may be influenced with techniques to improve a part's performance within the radiation environment. These techniques include RHBA, RHBD, and RHBP methodologies. They may be used independently or in combination - depending on the level of risk acceptance and funding available to the spacecraft designer. The RHESE project proactively responds to the anticipated requirements of these spacecraft through the development of materials, processors, reconfigurable systems, and models of the effects radiation will produce within these electronics, thereby assisting the eventual spacecraft designer with the ability to implement RHA.

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