MSFC-193 _ ABSTRACT

High-Performance, Radiation-Hardened Electronics
for Space Environments

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The Radiation Hardened Electronics for Space Environments (RHESE) project endeavors to advance the current state-of-the-art in high-performance, radiation-hardened electronics and processors, ensuring successful performance of space systems required to operate within extreme radiation and temperature environments. Because RHESE is a project within the Exploration Technology Development Program (ETDP), RHESE's primary customers will be the human and robotic missions being developed by NASA's Exploration Systems Mission Directorate (ESMD) in partial fulfillment of the Vision for Space Exploration[1]. Benefits are also anticipated for NASA's science missions to planetary and deep-space destinations.)

As a technology development effort, RHESE provides a broad-scoped, full spectrum of approaches to environmentally harden space electronics, including new materials, advanced design processes, reconfigurable hardware techniques, and software modeling of the radiation environment. The RHESE sub-project tasks are:

- Self Reconfigurable Electronics for Extreme Environments,
- Radiation Effects Predictive Modeling,
- Radiation Hardened Memory,
- Single Event Effects (SEE) Immune Reconfigurable Field Programmable Gate Array (FPGA) (SIRF),
- Radiation Hardening by Software,
- Radiation Hardened High Performance Processors (HPP),
- Reconfigurable Computing,
- Low Temperature Tolerant MEMS by Design, and
- Silicon-Germanium (SiGe) Integrated Electronics for Extreme Environments.

These nine sub-project tasks are managed by technical leads as located across five different NASA field centers, including Ames Research Center, Goddard Space Flight Center, the Jet Propulsion Laboratory, Langly Research Center, and Marshall Space Flight Center. The overall RHESE integrated project management responsibility resides with NASA's Marshall Space Flight Center (MSFC).

Initial technology development emphasis within RHESE focuses on the hardening of Field Programmable Gate Arrays (FPGA)s and Field Programmable Analog Arrays (FPAA)s for use in reconfigurable architectures. As these component/chip level technologies mature, the RHESE project emphasis shifts to focus on efforts encompassing total processor hardening techniques and board-level electronic reconfiguration techniques featuring spare and interface modularity. This phased approach to distributing emphasis between technology developments provides hardened FPGA/FPAAs for early mission infusion, then migrates to hardened, board-level, high speed processors with associated memory elements and high density storage for the longer duration missions encountered for Lunar Outpost and Mars Exploration occurring later in the Constellation schedule.

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1. National Aeronautics and Space Administration, *The Vision for Space Exploration*, Feb. 2004 from
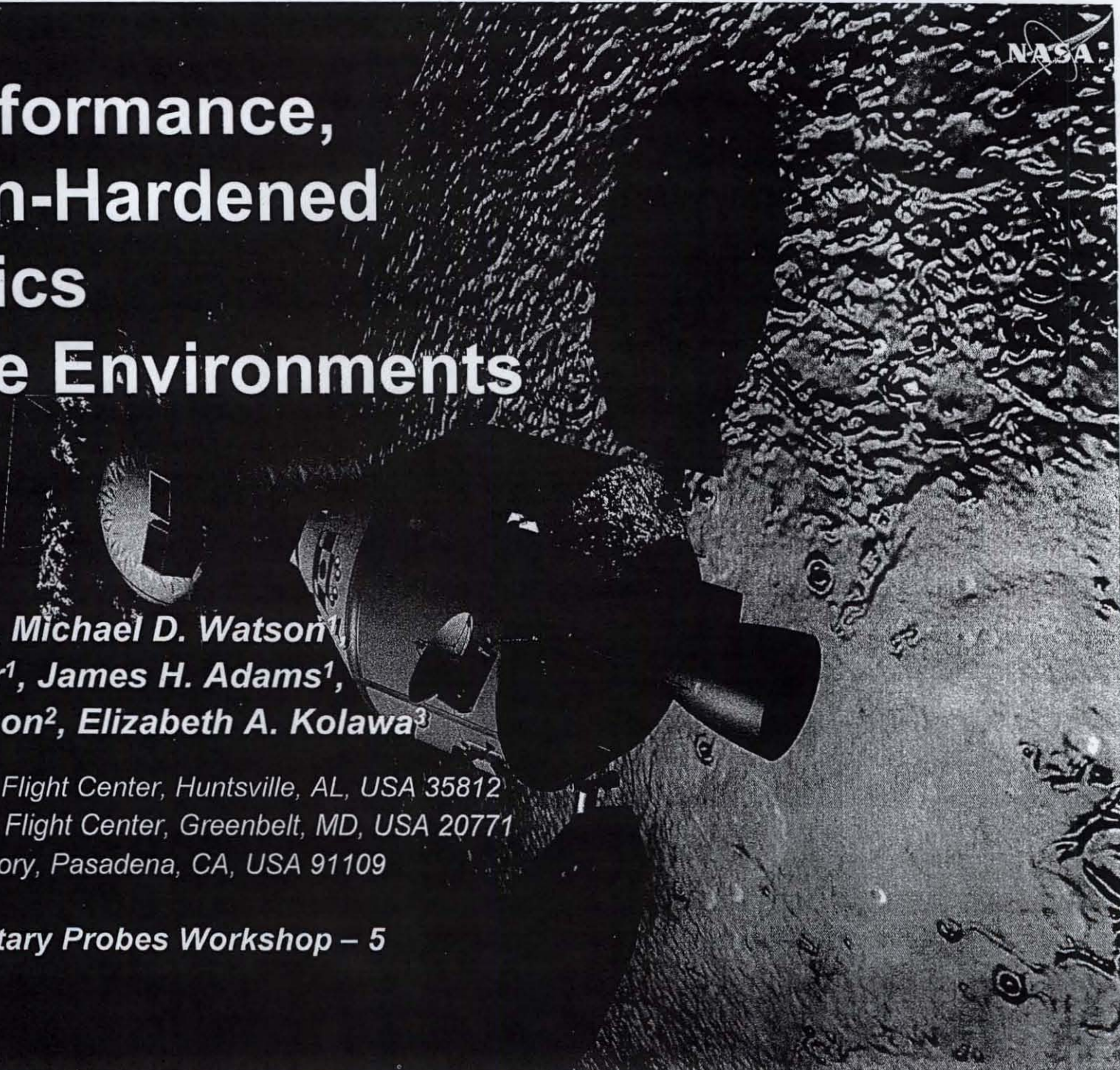   http://history.nasa.gov/Vision_For_Space_Exploration.pdf

National Aeronautics and Space Administration

NASA

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International Planetary Probes Workshop – 5
*Bordeaux, France*
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Presentation Order

- **Establishment of the Space Radiation Environment**
- Radiation Hardened Electronics for Space Environments (RHESE) Project Overview
- Silicon Germanium (SiGe) Integrated Electronics for Extreme Environments
- Self-Reconfigurable Electronics for Extreme Environments
- Radiation Effects Predictive Modeling
- Radiation Hardened High Performance Processors
- Reconfigurable Computing
- Single Event Effects (SEE)-Immune Reconfigurable Field Programmable Gate Array (FPGA) (SIRF)
- Radiation Hardened Memory
- Radiation Hardened by Software
- Low Temperature Tolerant MicroElectroMechanical Systems (MEMS)
- Exploration Systems Mission Directorate's (ESMD's) Constellation Program Support
- Summary

The Space Radiation Environment

- ◆ Space Radiation affects **all spacecraft.**
    - o Spacecraft electronics have a long history of power resets, safing, and system failures due to:
        - – Long duration exposures,
        - – Unpredictable solar proton activity,
        - – Ambient galactic cosmic ray environment.

- ◆ **Three approaches** may be employed (independently or in combination) to protect electronic systems in the radiation environment:
    - o Shielding,
    - o Commercial parts in redundant and duplicative configurations,
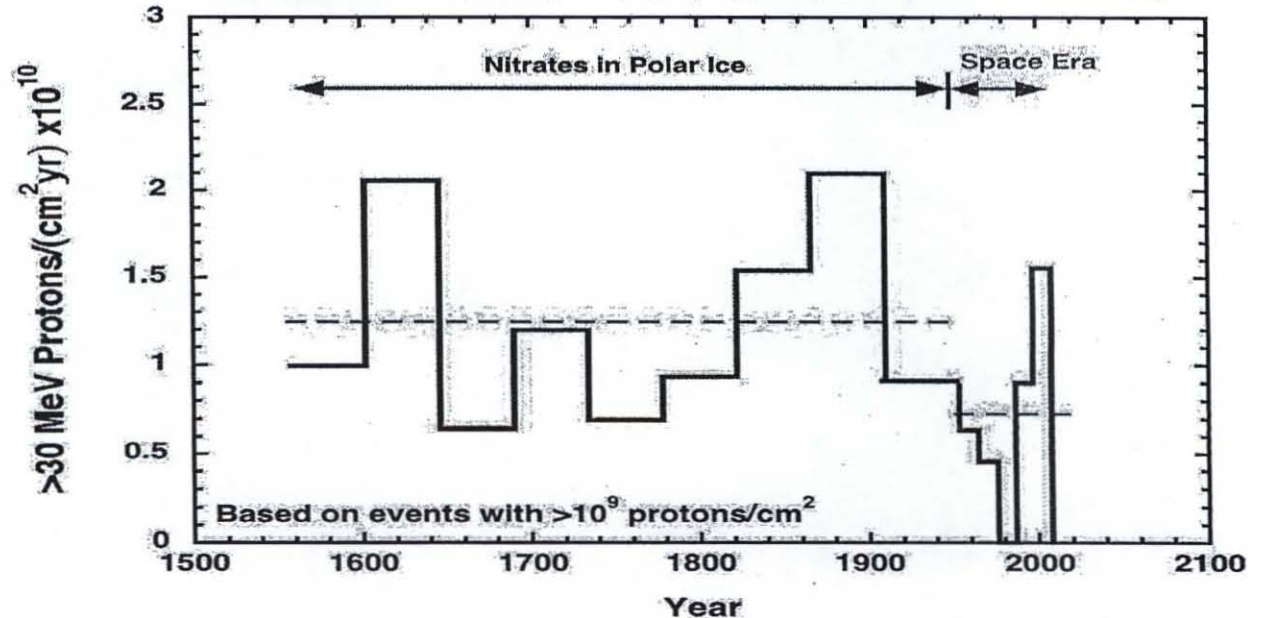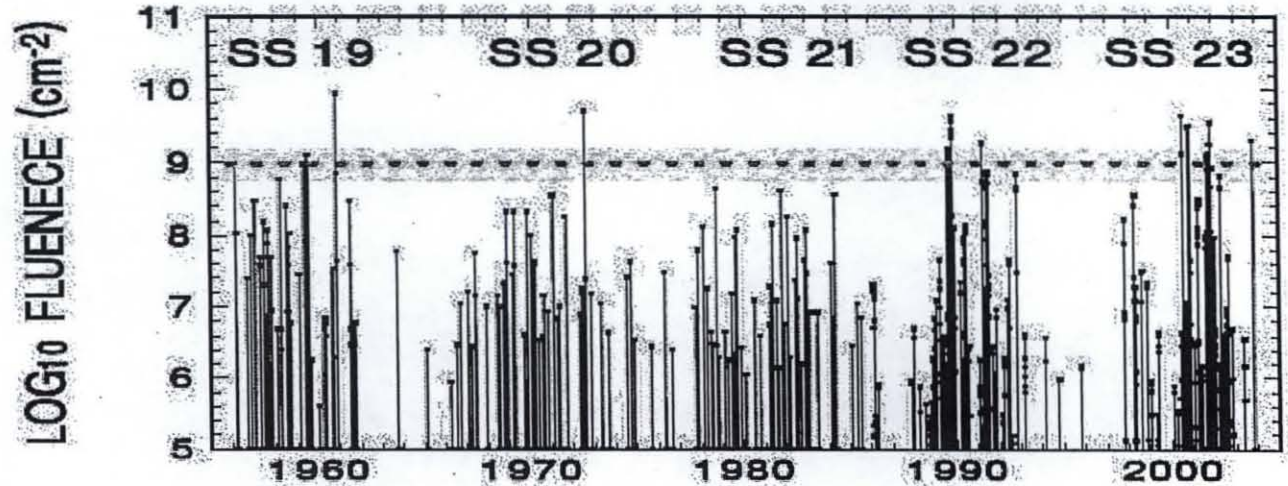   - o Electronics hardened for radiation and environmental exposure.
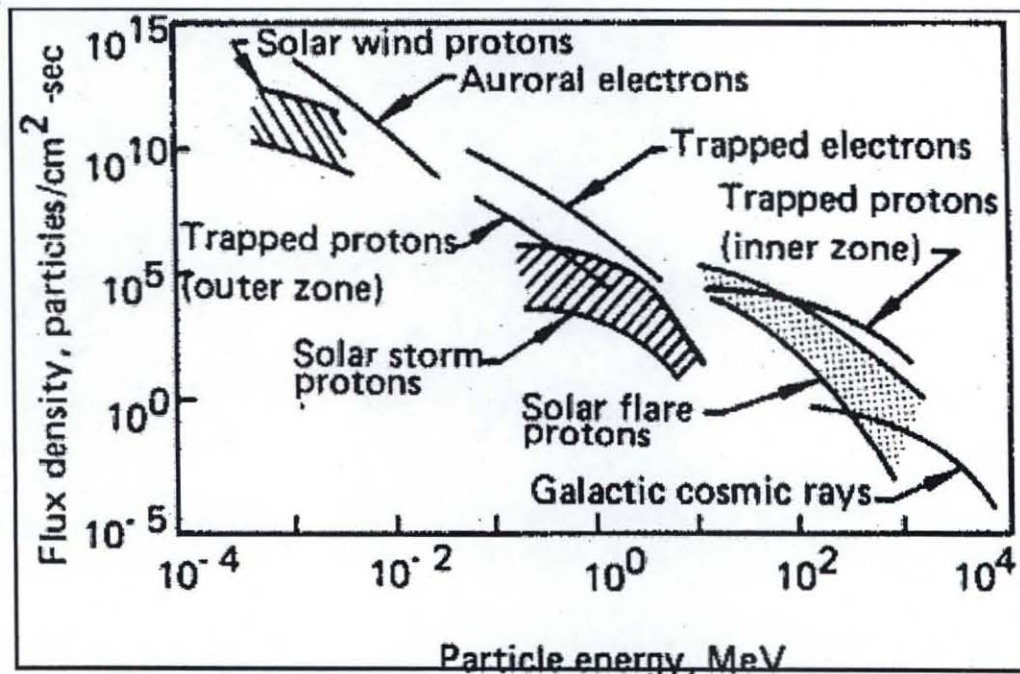
Record of Solar Particle Events

- Several large solar particle events typically occur in each solar cycle.

- They occur most frequently, though not exclusively, during solar maximum.

- Typically several spacecraft are disrupted, damaged or lost with each event.

>30 MeV SOLAR PROTON EVENTS
OMNIDIRECTIONAL EVENT FLUENCE

SS 19   SS 20   SS 21   SS 22   SS 23

LOG_{10} FLUENECE (cm^{-2})

1960   1970   1980   1990   2000

>30 MeV Protons/$(cm^2 \cdot yr) \times 10^{10}$

Nitrates in Polar Ice   Space Era

Based on events with >10^9 protons/cm^2

Year

1500   1600   1700   1800   1900   2000   2100

Solar Coronal Mass Ejection Event: 27 Oct. – 04 Nov. 2003

- In Oct-Nov of 2003, a series of X-class solar events took place
  - High particle fluxes were noted
  - Many spacecraft performed safing maneuvers
  - Many systems experienced higher than normal (but correctable) data error rates
  - Several spacecraft had anomalies causing spacecraft safing
  - Increased noise seen in many instruments
  - Drag and heating issues noted
  - Instrument FAILURES occurred
  - Two known spacecraft FAILURES occurred
- Power grid systems affected,
- Communication systems affected
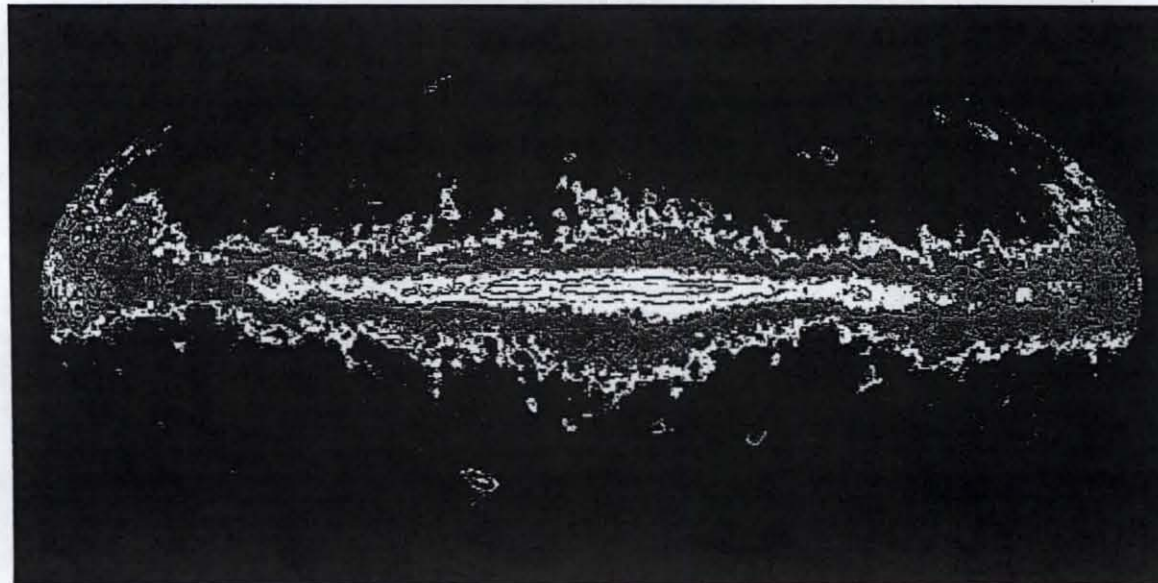

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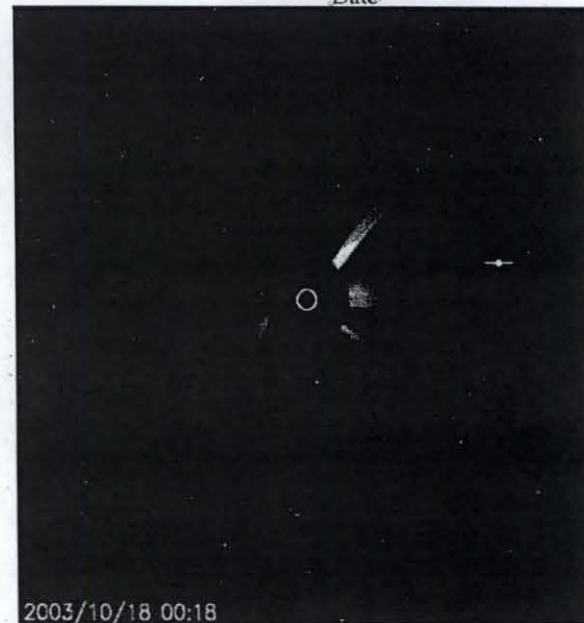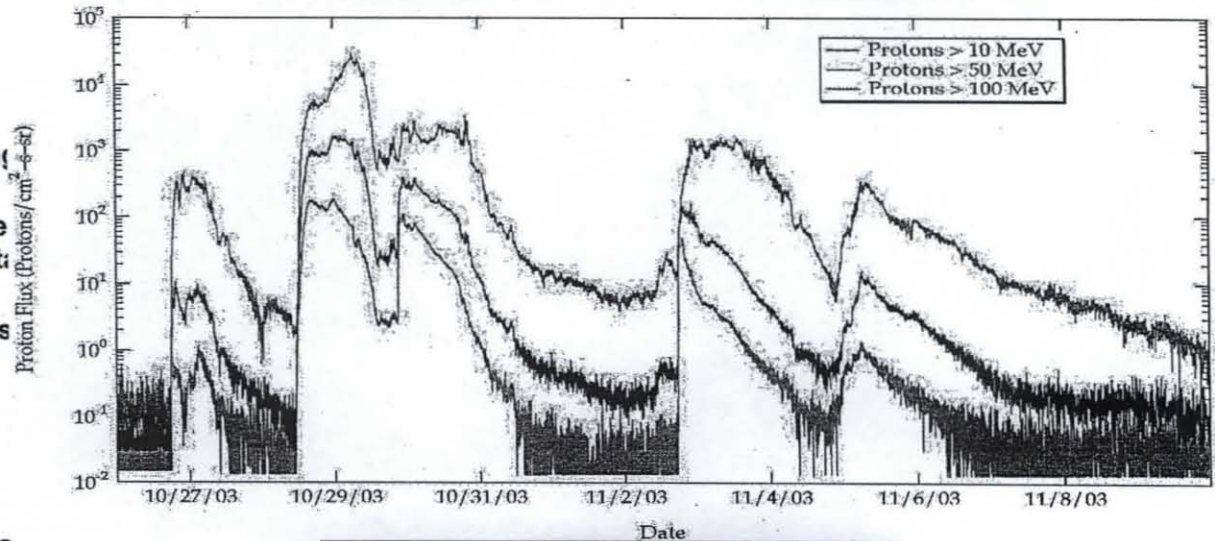
Video from Large Angle Spectrometric Coronagraph (LASCO)

Galactic Cosmic Rays

◆ High energy particles causing electronic Single Event Effects (SEEs) are Galactic Cosmic Rays (GCRs).

◆ GCRs are atomic nuclei from which all of the surrounding electrons have been stripped away during their high-speed passage through the galaxy.

◆ GCRs come from outside the solar system but generally from within our Milky Way galaxy where they are probably accelerated by supernovae blast waves.

◆As GCRs travel through interstellar space, some of them interact with the ambient interstellar gas and emit **gamma rays** as mapped by this EGRET all-sky survey.

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◆ Radiation Hardened High Performance Processors

◆ Reconfigurable Computing

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RHESE Project Overview

RHESE Project Description:

- The Radiation Hardened Electronics for Space Environments (RHESE) project seeks to advance the current state-of-the-art in **environmentally hardened electronics** for use in Constellation Program and Lunar (and Mars) Architecture applications.
- RHESE investigates a full spectrum of approaches to harden space electronics against **extreme radiation environments**, including:
  - Assessment of new materials
  - Layout design processes
  - Hardware reconfigurability techniques, and
  - Software design techniques that improve radiation tolerance.
- RHESE additionally investigates rad-hard methods and devices facilitating operation in **low temperature environments** (down to -180C), including:
  - SiGe materials,
  - reconfiguration to counter low-temperature effects, and
  - design approaches to improve low temperature operation.
- **Analog**, **digital** and **mixed-mode** electronic systems all benefit from RHESE investments.
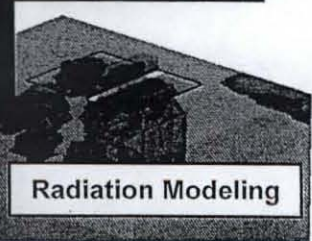
CRYO-I Circuit Design from GA Tech
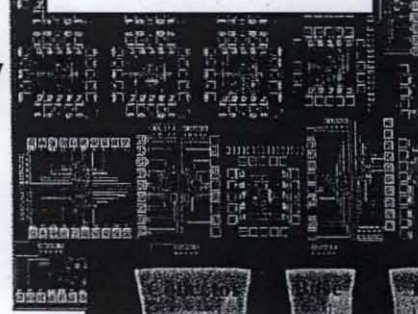
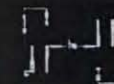CRYO-T Center-of-Excellence at GA Tech

SiGe Transistor Cross-Section

Radiation Modeling

Low Temp Micro-Electromechanical Systems (MEMS)

RHESE Project Tasks:
(Managing Center and Task Implementers)

(1.2.1.1) Self Reconfigurable Electronics for Extreme Environments
JPL, US Navy SPAWAR, LaRC, Arizona State University

(1.2.1.2) Radiation Effects Predictive Modeling
MSFC, Vanderbilt University

(1.2.1.3) Radiation Hardened Memory
MSFC

(1.2.2.1) Single Event Effects (SEE) Immune Reconfigurable Field Programmable Gate Array (FPGA) (SIRF)
GSFC, AFRL, SNL, University of Idaho, MDA

(1.2.3) Radiation Hardened by Software
ARC

(1.2.4) Radiation Hardened High Performance Processors (HPP)
GSFC, JPL, LaRC, MSFC

(1.2.5) Reconfigurable Computing
MSFC, LaRC

(1.3.2) Low Temperature Tolerant MEMS by Design
ARC

(1.3.1) Silicon-Germanium (SiGe) Integrated Electronics for Extreme Environments
LaRC, Georgia Institute of Technology, JPL, Auburn University, BAE Systems, Boeing, IBM, Lynquent Corporation, University of Arkansas, University of Maryland, University of Tennessee, Vanderbilt University

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"SiGe Integrated Electronics for Extreme Environments"
## John D. Cressler, Georgia Tech (PI)

Goal:

Develop Electronic Components Required for Lunar Robotic & Vehicular Systems Using SiGe Technology That Operate Reliably Under Lunar Ambient Conditions

Extreme Environment Requirements:
- **Must Withstand +120C (day) to -180C (night) + cycling**
- **Must Be Radiation Tolerant** (total dose + single event upset)

• Major Project Objectives:
- develop SiGe electronic components with extreme environment capability
- **deliver** compact modeling tools for circuit design (**design suite**)
- **deliver** requisite mixed-signal circuit components (**component library**)
- **deliver** robust packaging for these circuits (**integrated multi-chip modules**)
- demonstrate reliability per NASA specs & robust insertion path for LPRP
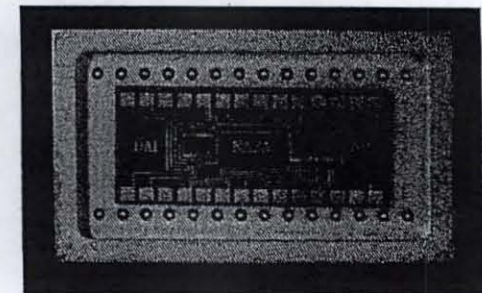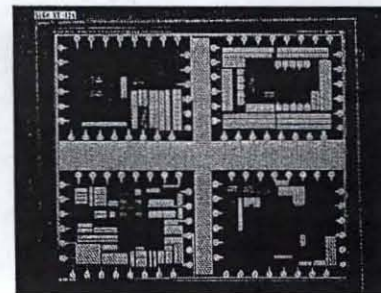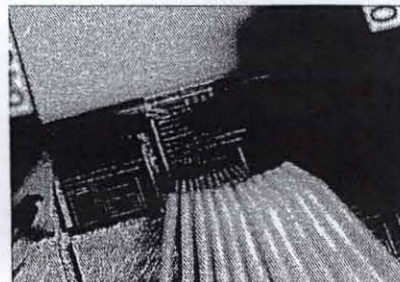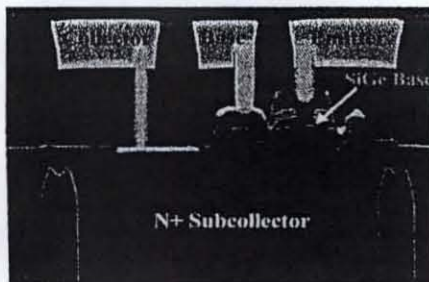
SiGe Integrated Electronics

- ◆ OBJECTIVES: **Develop and Demonstrate Extreme Environment Electronic Components Required for Distributed Architecture Lunar / Martian Robotic / Vehicular Systems Using SiGe HBT BiCMOS Technology**
- ◆ Extreme Environment Requirements:
  - o **+120C (day) to -180C (night) + cycling (main focus)**
  - o **radiation (TID + SEU tolerant)**
- ◆ Major Project Goals / Approach:
  - o prove SiGe BiCMOS technology for +120C to -180C applications
  - o develop mixed-signal electronics with proven extreme T + rad capability
  - o develop best-practice extreme T range circuit design approaches
  - o deliver compact modeling tools for circuit design (design suite)
  - o deliver requisite mixed-signal circuit components (component library)
  - o deliver robust packaging for these circuits (integrated multi-chip module)
  - o demonstrate device + circuit + package reliability per NASA specs
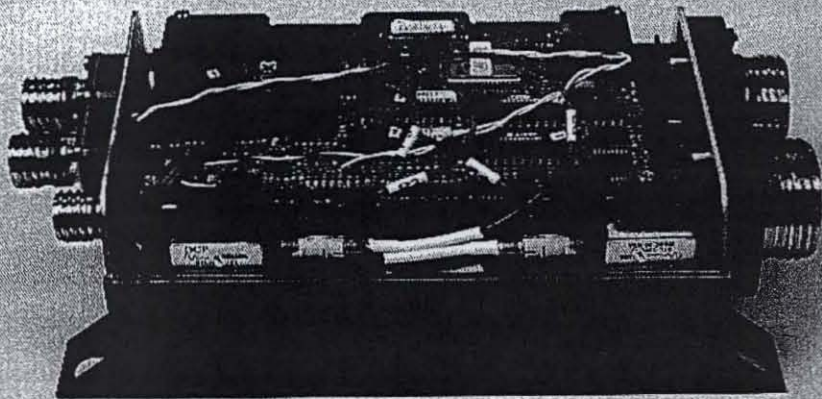 - o develop a robust maturation path for NASA mission insertion (TRL-6)
- ◆ Goal: Be Ready for NASA Insertion in 2009
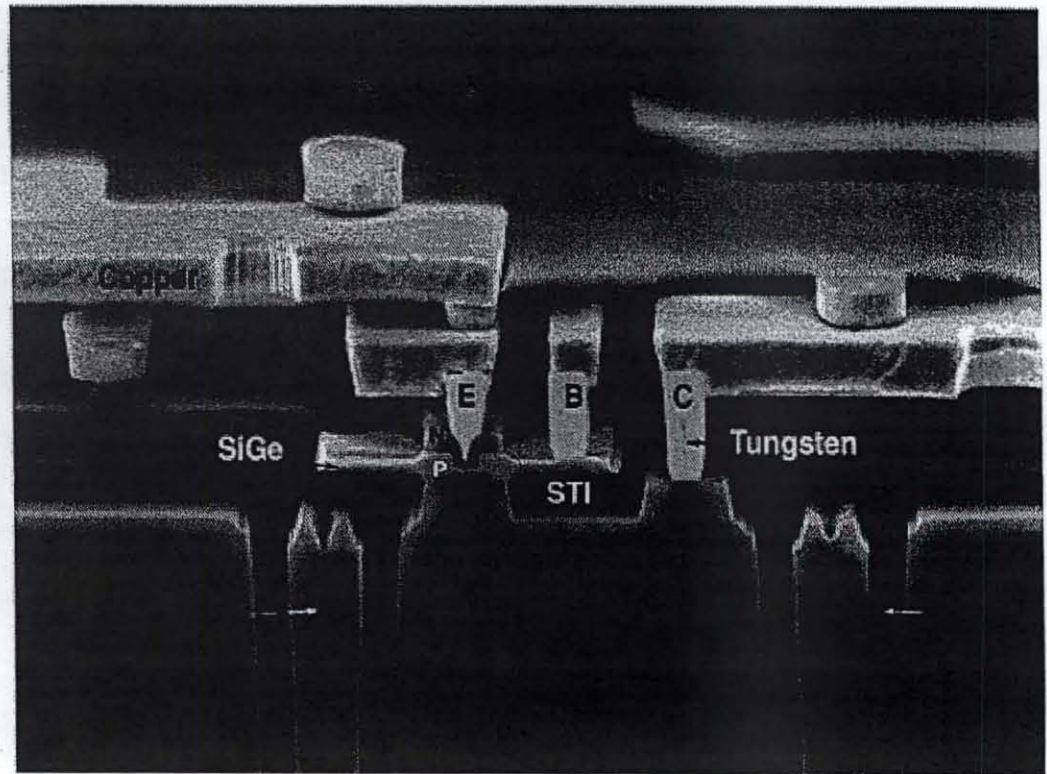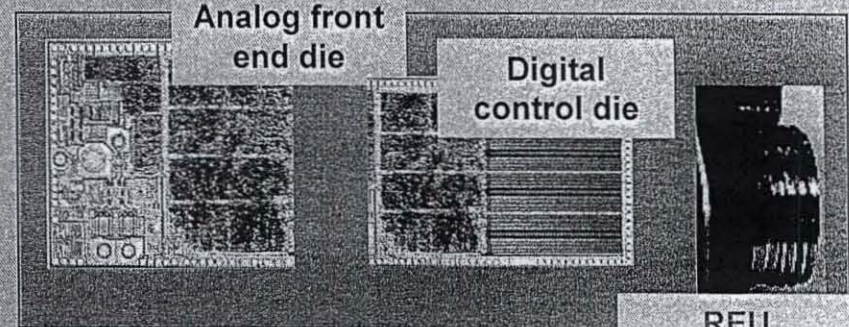
SiGe Integrated Electronics

The X-33 Remote Health Unit (circa 1998)

Remote Electronics Unit (circa 2009)

Analog front end die

Digital control die

Conceptual integrated REU system-on-chip SiGe BiCMOS die

REU connector housing

X-33 Remote Health Unit SPECIFICATIONS:

◆ 5" wide by 3" high by 6.75" long = 101 in^3
◆ 11 kg
◆ 17.2 Watts dissapated
◆ -55oC to +125oC

SiGe Application GOALS:

◆ 1.5" high by 1.5" wide by 0.5" long = 1.1 in^3
◆ < 1 kg
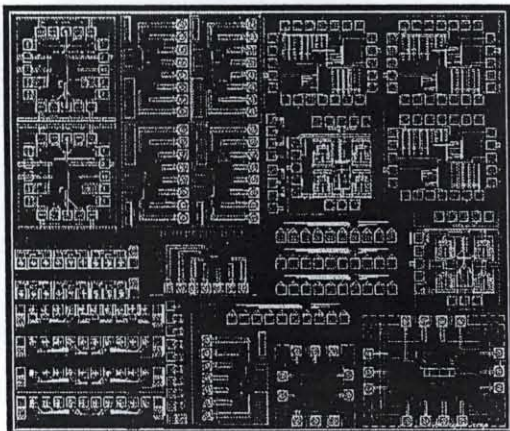◆ < 2-3 Watts dissapated
◆ -180°C to +125°C, radiation tolerant

ETDP Technology Development

SiGe Hardware Fabrication Path

CRYO-1

proof of concept
V references
op amps
DAC
VGA
HV device
digital blocks
test structures
modeling
MUXs

CRYO-2

refined CRYO-1
2 ADCs
more op amps
drivers
T sensors
bus interface
refined modeling
radiation evaluation
low power variants
ramp generator
REU components

CRYO-2.5

REU sub-path demo

CRYO-3

refined CRYO-2
REU sub-paths
more digital
more sensors
actuation
RF blocks
more bus interfaces
RHBD evaluation
low power variants

CRYO-4

refined CRYO-3
REU-on-a-chip
library enhancements
RHBD enhancements
modeling enhancements
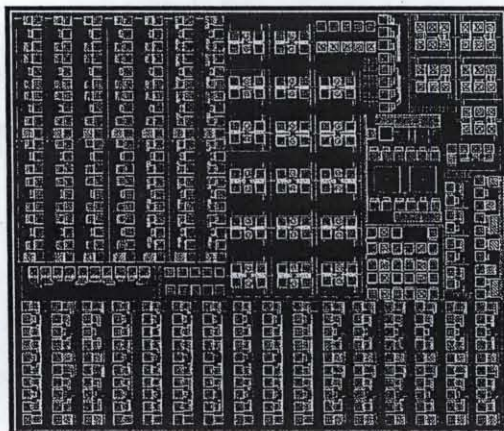low power variants

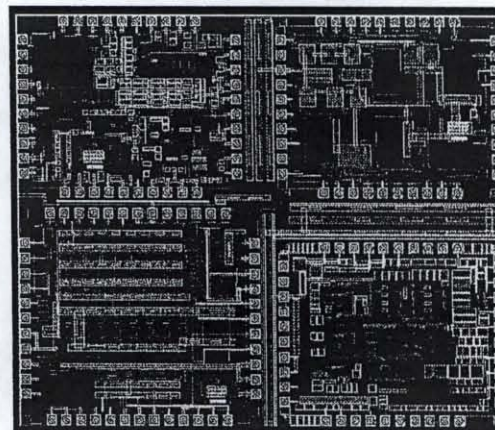## Develop Infrastructure for Extreme Environment Components / Systems

SiGe CRYO-2 Designs

Georgia Tech #1

Georgia Tech #2

Univ. of Tennessee

Univ. of Arkansas

Auburn Univ.

JPL / Boeing

SiGe CRYO-2 Hardware
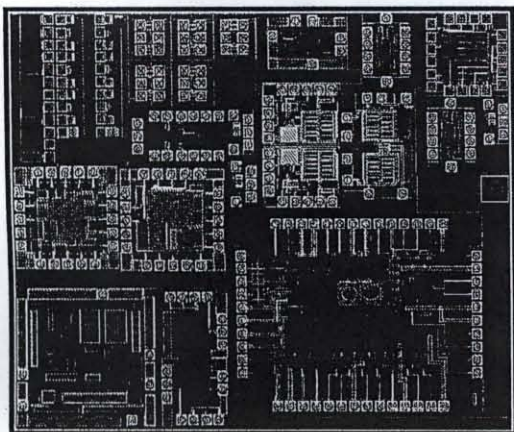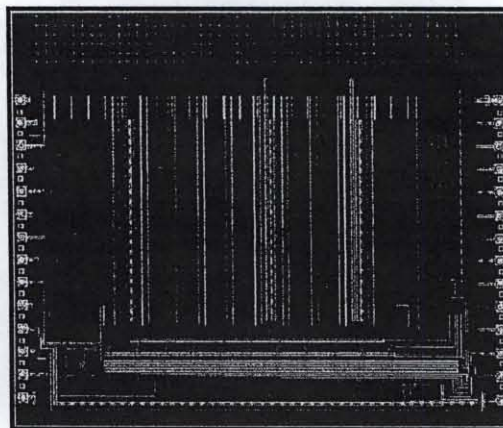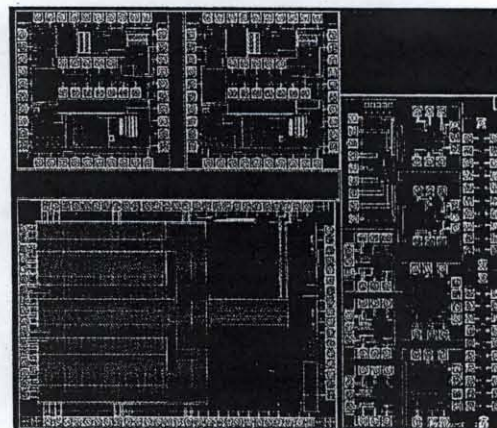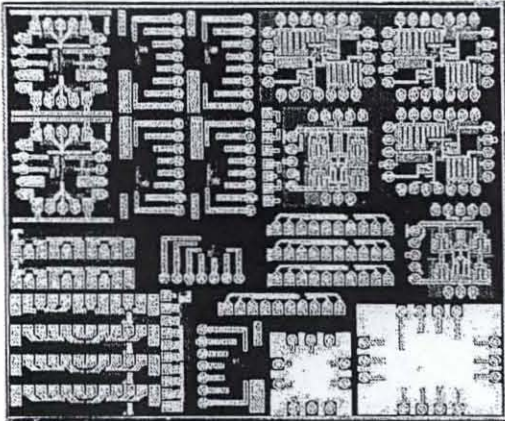

Georgia Tech #1
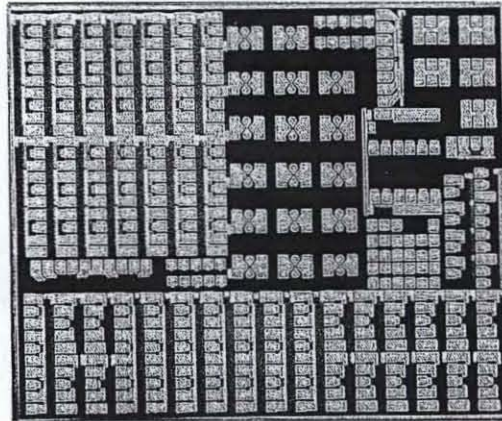
Georgia Tech #2
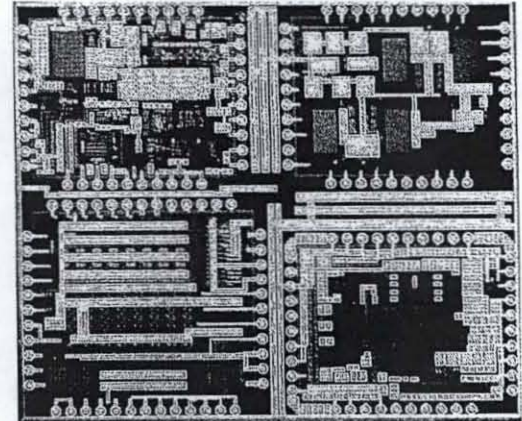
Univ. of Tennessee
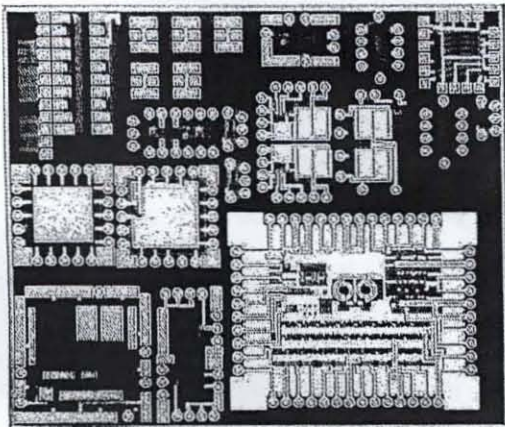
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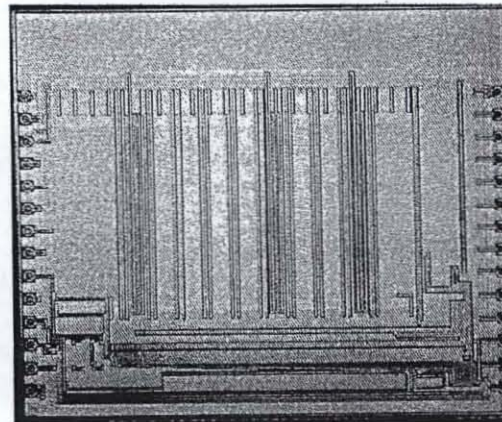
Auburn Univ.
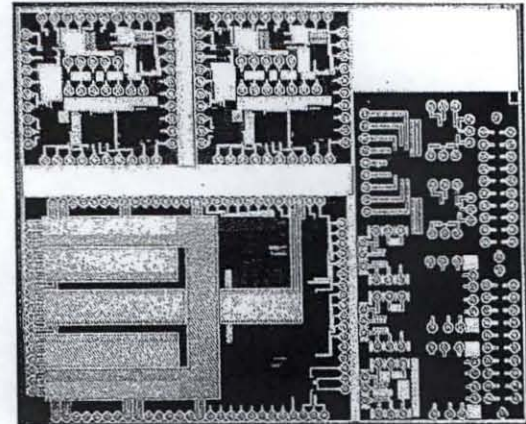
JPL / Boeing

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◆ **Work is needed to address the challenge of <u>surviving the thermal stresses</u> induced on electronic devices when they are exposed to the Lunar ambient environments (-230C in permanently shadowed areas and/or -180C to +120C diurnal temperatures).**

◆ **The need for extreme environment electronics, operating in Lunar ambient, comes from the necessity to <u>simplify the complexity and magnitude of the wires</u> connecting the key sensors and actuators to the centralized core computer system.**

◆ **Extreme environment electronics can be distributed to locations at the major appendages and integrated with the local sensors and actuators limiting needed connections to <u>power and data buses.</u>**

MER Baseline Design - State of the Art

- **Centralized Design:**

  - The standard electronics , mostly rated from –55C to +125C operation (Mil-Spec), is kept at a safe temperature (-40C to +40C) inside a Warm Electronics Box (WEB). Very little if any electronics outside
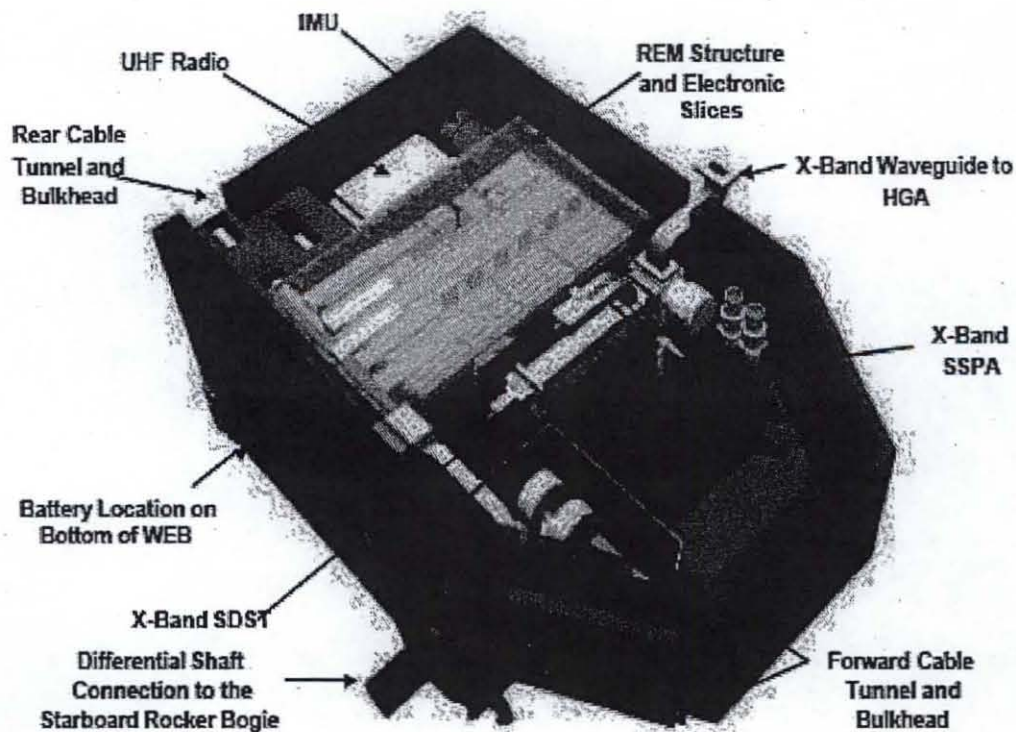
Issues with MER Baseline Centralized Design

- **Excessive Wire Length: <u>2,685 m per rover !</u>**
  - Mass and volume penalty, noise coupling, transmission line effects, resistive losses, lower reliability
- **Excessive Number of Wires: <u>1106 per rover !</u>**
  - Mass penalty, thermal loss to WEB (25% wires contribution) leading to higher required power
- **Complexity**
  - Costly and lengthy ATLO (Assembly, Test, and Launch Operations)
- **No Modularity**
  - No savings in recurring costs for next rover, no repair after launch
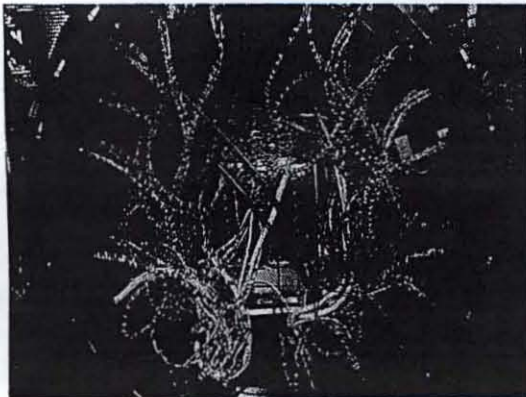
MER Rover Electronics in Thermal -Vac
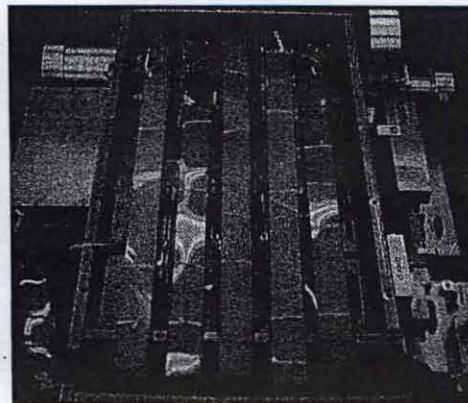
MER internal wiring
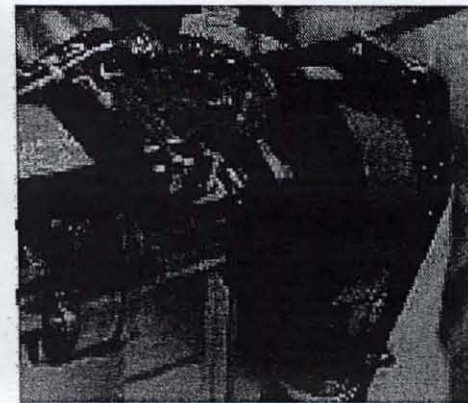
Wiring for a joint in robotic arm

MER Testing

Innovative SRE-EE technology

◆ Self-Reconfigurable *analog* Electronics for EE (SRE-EE) technology: *combination of survivability at cell level and flexibility at architectural level*

- o Survivability at analog Cell level:
  - – Designed with digitally-controlled, tunable compensation points
  - – Wide-temperature design, rad-hard by fabrication

- o Flexibility at architectural level
  - – Many functions - by same IC – via programmable interconnection between cells
  - – In-situ, on-line functional change by self (algorithmic) reconfiguration

SRE-EE Proposed Solution

Centralized Architecture   **Distributed Architecture**
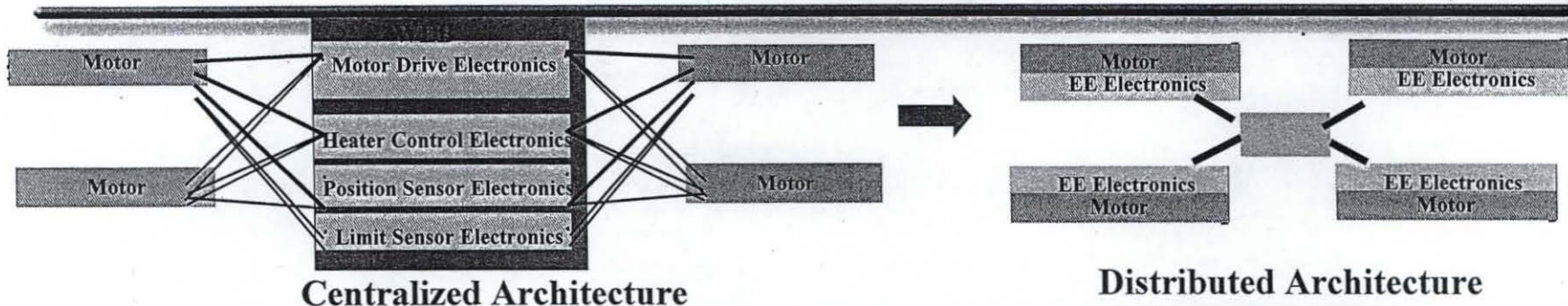
	Centralized Architecture (MER)	Distributed Architecture	Estimated Benefits of Distributed Architecture (EE Electronics)
Wire length	~2,500 m	~200 m	~90 % reduction
Number of wires	~1600	~350	~65 % reduction
Modularity	No	Yes	Easier redesign, fab, test, and assembly

◆ **Make electronics *self*-reconfigurable, adaptive to extreme environments.**

◆ SRE-EE designs and algorithms will
  - detect degradation in circuit performance due to faults or partial drifts caused by temperature and radiation
  - **compensate for these faults and drifts** by changing to another configuration (either pre-determined or computed in-situ) more appropriate for the operating conditions.

Self-Reconfigurable Analog Array

Reconfiguration Control (digital)

Reconfigurable Analog Array

In ⟶ ⟶ Out

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Radiation Modeling

- The Single Event Effect (SEE) prediction models currently in use were developed ~10 years ago.
  - They were written when feature sizes were >1 μm
  - Devices did not contain heavy metals
  - Microcircuits were not complex 3-D structures
  - These models are not reliable for modern devices
- Current radiation model available:

https://creme96.nrl.navy.mil/

Radiation Modeling Objectives

- ◆ Provide accurate evaluations radiation effects in space
  - o By understanding how specific device technologies respond to ionizing radiation,
  - o By providing the ability for designers to accurately predict a mean-time-between-failure for components and sub-systems, and
  - o By providing a computational tool to estimate mission-specific total dose and SEE rates.
- ◆ Improve External Radiation Environment Descriptions
  - o Galactic cosmic cays
  - o Solar energetic particles
  - o Anomalous cosmic rays
- ◆ Improve Radiation Transport though Spacecraft
  - o Full Monte Carlo radiation transport
- ◆ Provide a Physics-Based Simulation Tool of Single-Event Effects
  - o Correctly treat hole-electron plasma creation
  - o Charge collection
  - o Circuit response
- ◆ Make the computational tool available to designers through the internet.

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- Low Temperature Tolerant MicroElectroMechanical Systems (MEMS)
- Exploration Systems Mission Directorate's (ESMD's) Constellation Program Support
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High Performance Processor Motivation

- ◆ **Problem**: Exploration Systems Missions Directorate objectives and strategies are constrained computing capabilities and power efficiencies

  - o Autonomous vehicle operations
  - o Autonomous rendezvous and docking
  - o Vision systems
  - o Precision landing systems

  ...all predicted to require processor capabilities that **exceed the current RAD750's performance specifications**.

- ◆ CASE STUDY: LPRP Robotic lander Pre-Phase A design team selected the specified capabilities of the RAD750 processor as a target platform against which to do loading studies during descent and landing phase of the mission.

  - o Preliminary processing needs saturated RAD750 processor capabilities.
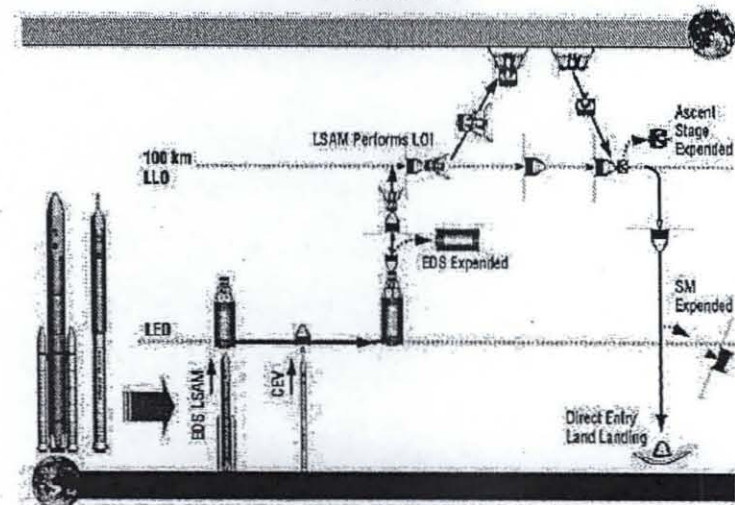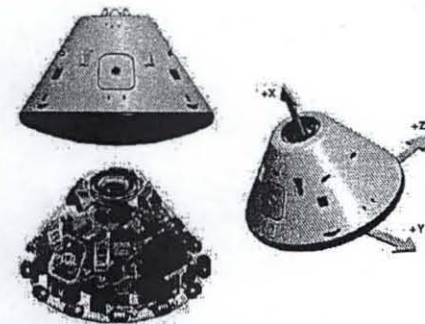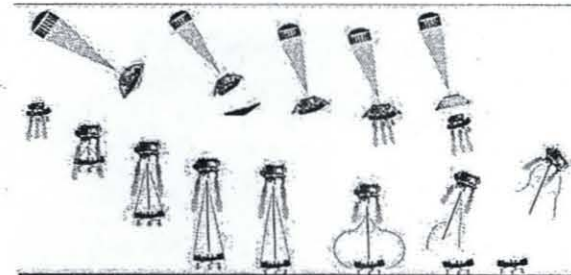
High Performance Processor Development

NASA

Driving Capabilities

Objectives- Evaluate suitability of DoD-funded DSP technologies for NASA numerically-intensive applications. Implement Phase I (hardened-by-microarchitecture) radiation mitigation strategies.

Will solicit IPP Seed funds

ELD, Hazard Avoidance, Surface Mobility, AR&D

GMAC/sec Digital Signal Processor Characterization DoD/DARPA/NASA

Functional, Performance, Radiation Characterization

Define, Implement, Evaluate ø1 Mitigation Strategies
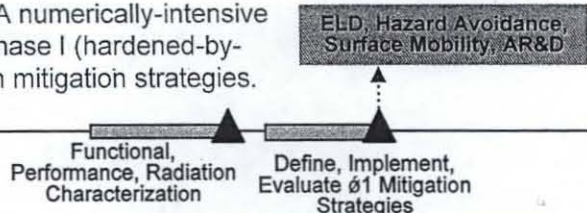
Objective- Develop radiation-tolerant state-of-the-art reconfigurable FPGAs

Rad-tolerant FPGA Fabric

Modular / Reconfigurable Systems

rFPGA/PPC440 Processor

ELD, Hazard Avoidance, Surface Mobility, AR&D

Majority of funds from DoD

DoD/NASA rFPGA Program

SIRF Virtex-5 LX delivery and eval (Fabric only)

NASA Virtex-5 FX delivery and eval (w/ embedded processors)
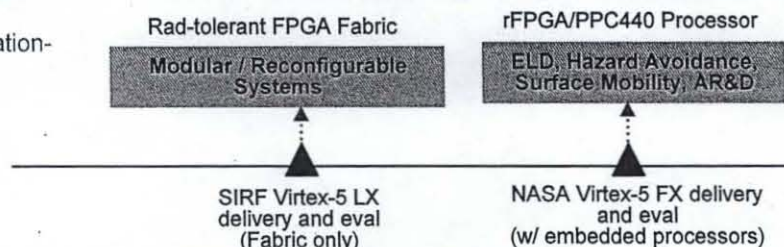
Objective- Develop high-performance near-state of the art processor by leveraging DoD investments in radiation-hardened-by-design technologies

LSAM, Lunar Habitat Systems

LSAM, Lunar Habitat Systems

>1000 MIP Embedded Processor Core

DoD/NASA 90nm RHBD IP Cores Collaboration

AFRL / ASU / NASA Kickoff

Functional, Performance, Radiation Characterization

RHBD Processor Core Delivery

>1000 MIP, 1W Embedded SoC

DoD 90nm RHBD Program

DoD RHBD Library/Tool Development

RHBD EDA Flow, Libraries Delivery

90nm SoC Cores Delivery

NASA/DoD 90nm SoC Delivery

NASA Investments
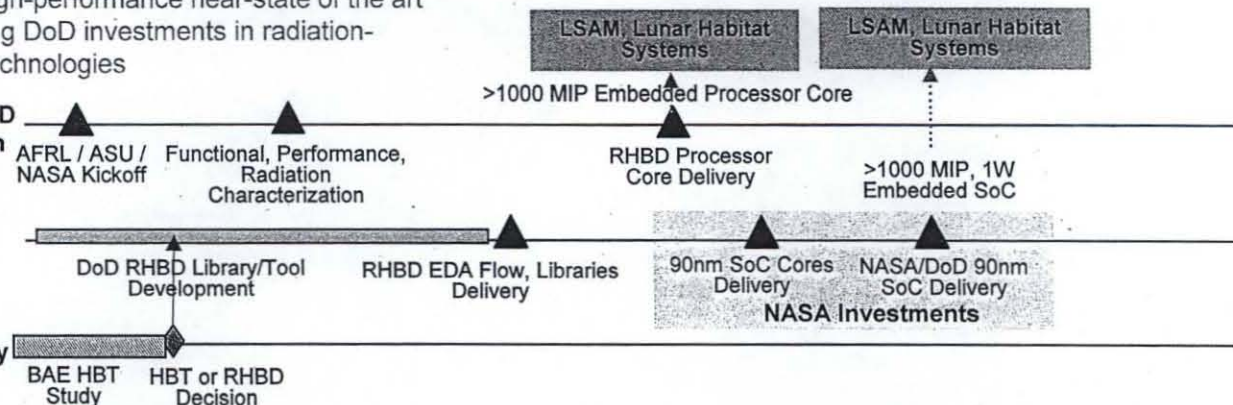
RHESE BAE Silicon Germanium HBT Study

BAE HBT Study

HBT or RHBD Decision

Objective- Infuse NASA legacy rad-tolerant ultra-low power general purpose processor into relevant ESMD applications

Lunar Habitat Systems, EVA Spacesuits

Rad Tolerant Ultra Low Power (RT ULP) Processor Development

32-bit RT ULP processor design

v0 RT ULP delivery

v1 RT ULP delivery

v2 RT ULP delivery
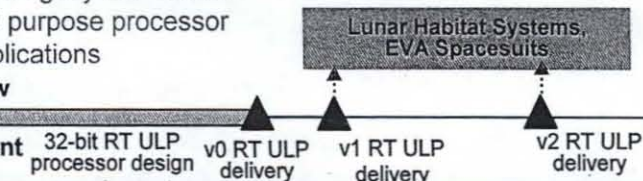
International P

CY   2007   2009   2012

Which Spaceflight Processor Design Approach is Superior- COTS-based or Radiation-Hardened?

It depends … The approach should be driven by system-level criteria-

| CRITERIA	COTS HARDENING BY ARCHITECTURE (e.g. Maxwell SCS750 single board computer)		RADIATION HARDENING BY DESIGN (RHBD) (e.g. BAE RAD750)	
Current Performance Level	COTS components and systems offer relatively high throughput (e.g. approximately 1300 MIPS for the Maxwell SCS750 single board computer).	G	Performance of available products lags commercial technologies by several fabrication process generations (e.g. < 200 MIPS for the RAD750 processor).	R
Radiation Susceptibility / System Impacts of Mitigation Strategies	Tolerance is derived from strategies such as processor voting or error correcting codes. Mitigation strategies can have "non-linear" system-level ramifications (e.g. state rollback or system reset) and adversely affect or disrupt throughput. Performance impacts depend on the system and on the type and severity of the error: ◉○ **Minimal** for systems amenable to transient impacts ◉ **Major** for systems intolerant of upsets	Y	Tolerance is derived from microarchitecture- and component-level strategies- e.g. device fabrication process modifications, and restructured, spatially distributed or voted logic cells. Radiation mitigation does not affect system behavior. Impact is reflected in the lower performance of devices incorporating radiation-hardened-by-design mitigation strategies.	G
Mitigation Strategy Complexity	Architecture-derived mitigation strategies increase processor-board or system complexity and component count.	R	Complexity is implemented at the device fabrication and micro-architecture levels. Board- or system-level architectures are not impacted.	G
Relevant Ongoing Technology Development Programs	Goal of ongoing programs (e.g. ST8) is to accommodate insertion of any COTS processor into hardening-by-architecture systems. Programs do not address system complexity or resource efficiency.	G	Significant DoD investment in RHBD cell libraries and development tools targeting "near state of the art" technology nodes is ongoing. Significant deliverables in 12-18 months. Technologies target throughput greater than 1000 MIPS for general purpose computing and greater than 10 GMACS/S for special purpose computing.	G
Power Efficiency	Significant inefficiencies result from the need to incorporate multiple processors, voting logic and a system monitor.	R	Deep submicron fabrication processes and micro-circuit design techniques promote power efficiency. Hardening strategies compromise power efficiency relative to non-hardened designs.	Y

General Purpose Commercial vs. Radiation-Hardened Processor Comparison

◆ Commercial devices, specifications, and capabilities are **driven by consumer market**, not NASA, DoD, DOE or Intelligence Agency requirements.

  o Preliminary data released 28 March on Intel Core 2 "Penryn" Processor family (release date in late 2007):
    – Produced by new Intel foundries in AZ (Fab 32) and Israel (Fab 28)
    – 45 nm High-k metal gate process technology
    – Core clock speeds > 3GHz
    – Power < 65W
    – Radiation Hardness = ???
      • Commercial suppliers often **intentionally avoid radiation characterization** of product to stay clear of ITAR restrictions.
      • Consumer electronics manufacturers may want to **prevent space environment validation** of parts.

◆ Radiation Hardened electronics, by comparison, are **domestically driven by US Government needs and requirements** and lag commercial development by **about 10 years**.

  o Current state-of-the-art rad-hard processor = BAE's RAD750 specifications.
    – Produced in BAE foundry (only two rad-hard foundry lines in US: BAE and Honeywell)
    – 250 nm CMOS processing technology
    – Processor speed 110 to 133 MHz
    – Capability = 200 MIPS
    – Power dissipation = 10 W
    – Temperature range = -55C to 125C
   – Radiation Hardness = TID of 200 krad, SEU of 1e-10 upsets/bit-day
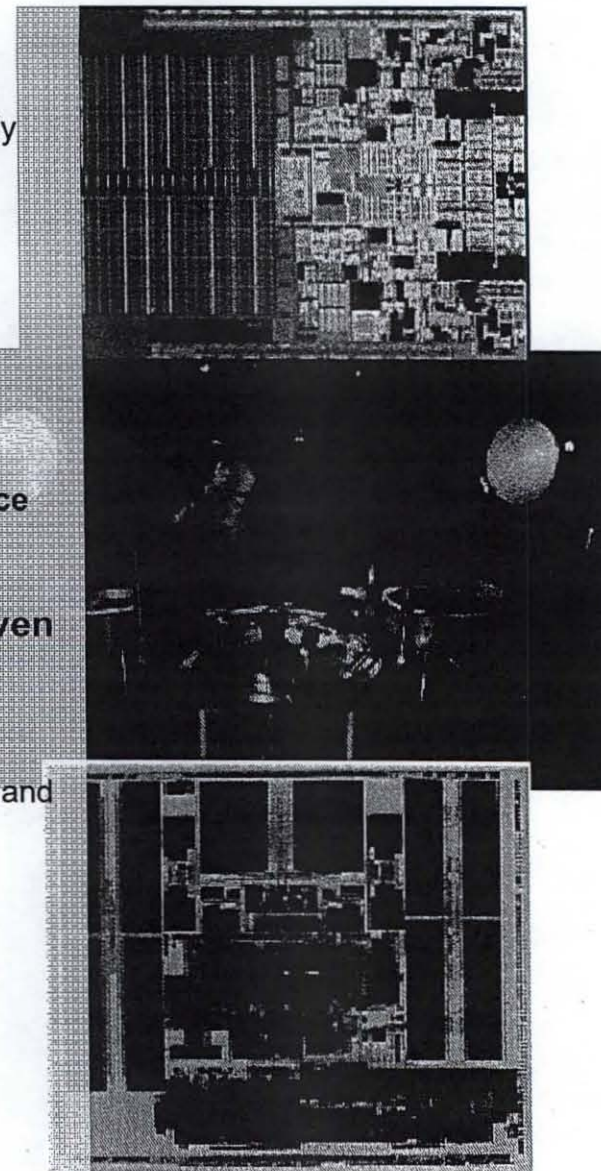
High-Performance Power-Efficient Processors
Multi-generation Performance Lag

◆ **Radiation-hardened processors lag commercial devices by several technology generations (approx. 10 years)**

o RHESE High Performance Processor project full-success metric conservatively keeps pace with historical trend (Moore's Law)
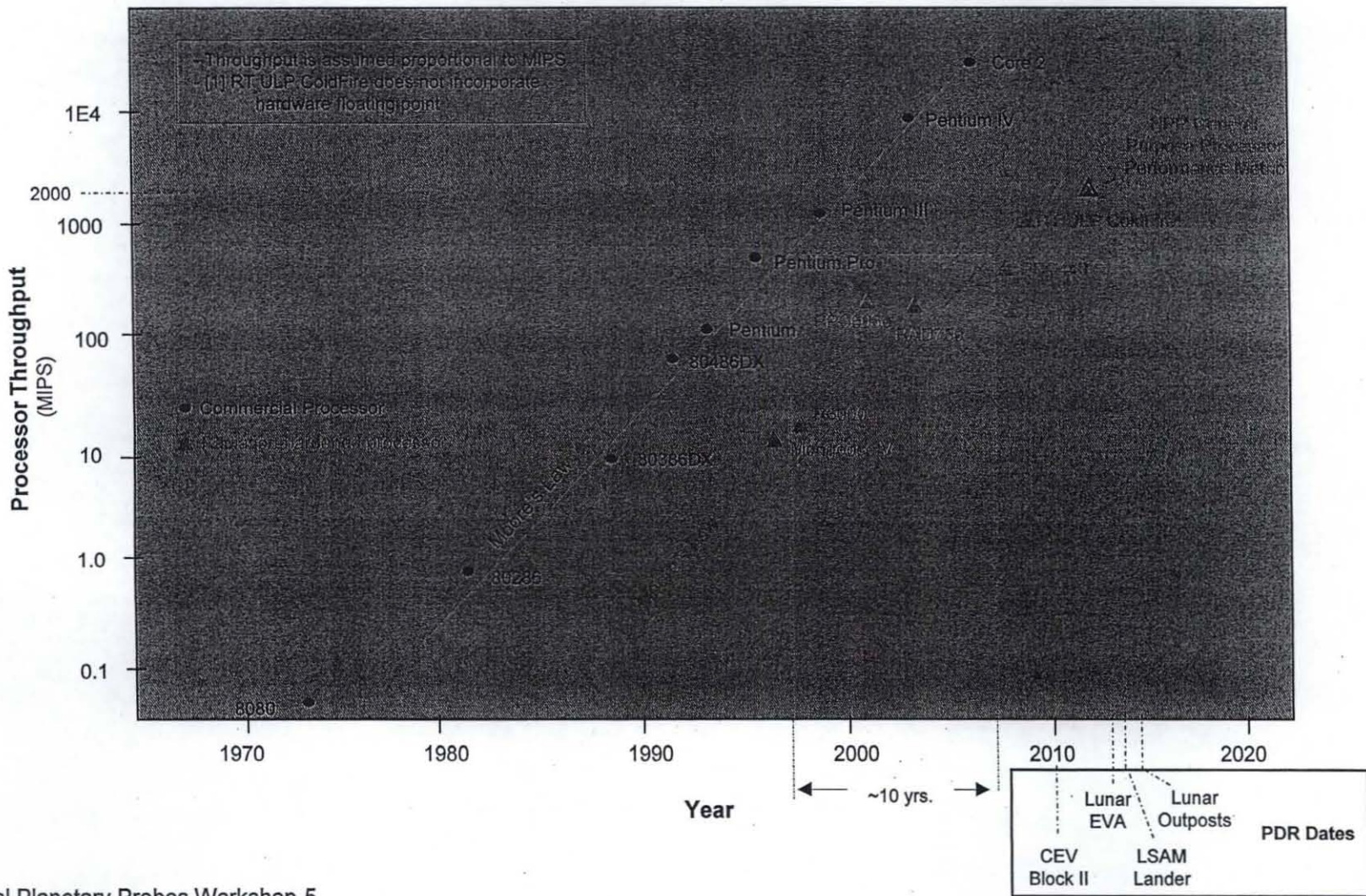
High Performance Processing
Autonomy

- Remote-control of spacecraft with delays is infeasible
  - *Even true with "only" lunar transit times*
  - Especially true of systems with strong dynamics (e.g. spacecraft landing/docking)
  - Orbital Maneuvering Systems (OMS) demonstration in the early 90's demonstrated 0.5 sec latency in low earth orbit was sufficient to **prevent reliable human remote control of spacecraft.**
- Critical autonomy areas:
  - *Reduced ground support costs* (Orion, LPRL, New Millennium, etc.)
  - Safe and accurate landing (e.g. LPRP)
  - Enhanced rover operations (e.g. LPRP)
  - Anytime/anywhere abort for human spacecraft
  - Unmanned spacecraft (e.g. quiescent Orion, New Millennium, etc.)
  - Spacecraft docking (e.g. Cx)
- Performance of existing spaceflight-capable processors directly affects Exploration systems capabilities
  - Imposes significant constraints on spacecraft autonomous operations, rover traverses, EDL performance
  - Processor power inefficiency further constrains implementation options and systems feasibility
- RHESE is addressing this challenge by collaborating with DoD to leverage relevant processor development programs
  - Technologies under consideration address processor performance and power efficiency metrics
    - Signal processing at greater than **10 GIPS** with less than **2 W** power dissipation
  - Metrics of candidate technologies meet or exceed performance requirements for Exploration systems
  - Power efficiency of candidate technologies facilitates systems implementation in severely power-constrained environments
- High Performance Processor technologies targeting NTL FY12 delivery

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◆ Silicon Germanium (SiGe) Integrated Electronics for Extreme Environments

◆ Self-Reconfigurable Electronics for Extreme Environments

◆ Radiation Effects Predictive Modeling

◆ Radiation Hardened High Performance Processors

◆ **Reconfigurable Computing**

◆ Single Event Effects (SEE)-Immune Reconfigurable Field Programmable Gate Array (FPGA) (SIRF)

◆ Radiation Hardened Memory

◆ Radiation Hardened by Software

◆ Low Temperature Tolerant MicroElectroMechanical Systems (MEMS)

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◆ Summary

Reconfigurable Computing

- ◆ **Flight-Qualified, Multi-String Redundant Hardware is Expensive**
  - o Development, Integration, IV&V, and Flight Qualification
  - o Space and Weight
  - o Power Consumption
  - o Dissimilar Spares
- ◆ **"From Scratch" Design of Computing Resources for Every New Flight System is Unnecessary and Wasteful**
- ◆ **Requirements for Flexibility are Increasing and Smart**
  - o Reconfigurable and Modular Capabilities
  - o Capacity to use one system to back up any number of others
  - o General Reusability
- ◆ **Current Options for Harsh/Flight Environment Systems are Limited**
  - o Custom Hardware, Firmware, and Software
  - o Dedicated and Inflexible
  - o Often Proprietary

Reconfigurable Computing Products
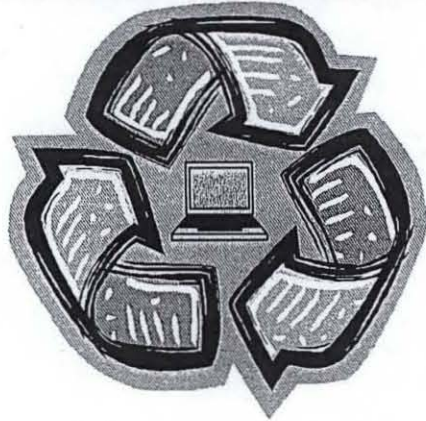
♦ Specific **products and applications** of this task will include:

o Reconfigurable processors supporting multiple architectures to enable single spares to fulfill multiple electronic functions.

o Reconfigurable processors supporting avionics redundancy by providing adaptable spares.

o Reconfigurable processors supporting recovery from component damage by radiation strikes and other events.

o Reconfigurable processors supporting multiple interfacing and interconnection options.

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Single Event Effects (SEE) Immune Reconfigurable Field Programmable Gate Array (FPGA) (SIRF)

- Target Device: 5th generation Virtex™ device
  - o 65 nm process
  - o 11 metal layers
  - o Up to 8M gates
- Columnar Architecture enables resource "dial-in" of
  - o Logic
  - o Block RAM
  - o I/O
  - o DSP Slices
  - o PowerPC Cores
- **FPGA design techniques developed that produce radiation-tolerant technologies capable of exhibiting**
  - o **radiation-tolerant reconfigurable interfaces**
  - o **digital interconnects.**

Fabrication process and device architecture yield a high speed, flexible component
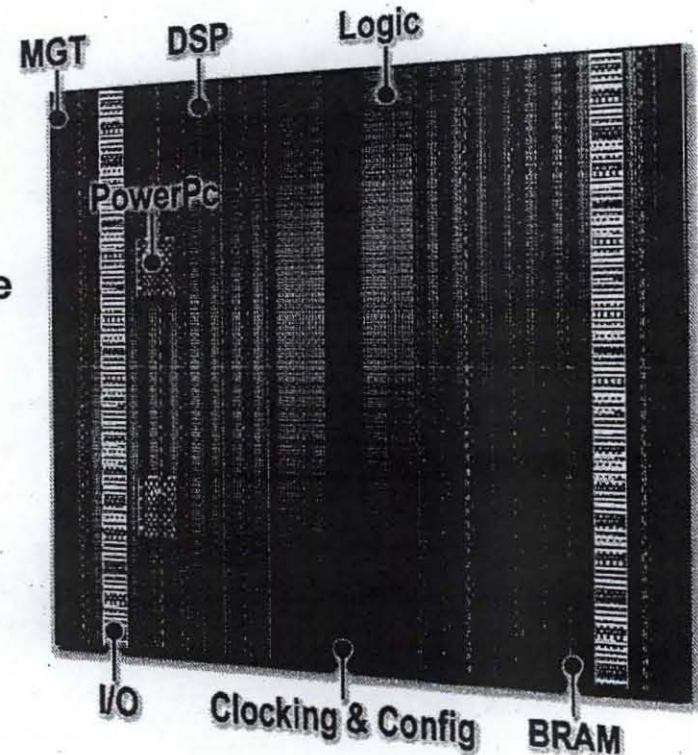
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Radiation Hardened Memory

- **Problems to solve:**
  - TMR (Triple Module Redundancy) - cost, power, complexity, weight
  - No high density Nonvolatile memory is available
  - FLASH or EEPROM nonvolatile memory has endurance problems (i.e. limited number of writes)
- **Virtues of Radiation Hardened Nonvolatile Memory (Ferroelectric(FRAM), Chalcogenide, Magneto-resistive (MRAM), Nano-tube)**
  - Advanced material based memory is emerging as a viable commercially available product - within the next few years
  - Inherently radiation tolerant
  - Allow single string use as opposed to TMR and still meet reliability requirements
  - Offer high-speed read and write - can be used in computer's main memory or cache
  - High endurance (# read/writes)
  - Dense
  - Low power
  - Eliminates refresh requirements
- **Collectively these novel memory technologies suggest near term and significant advancement in radiation-hardened memory devices**
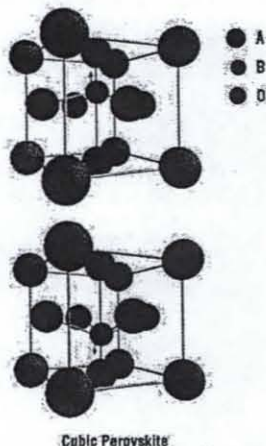
Freescale Semiconductor
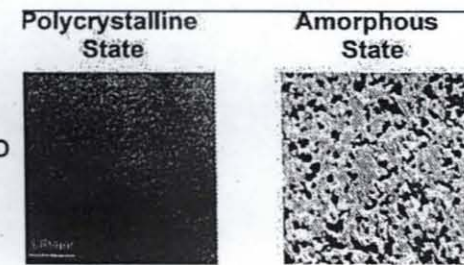*MRAM*
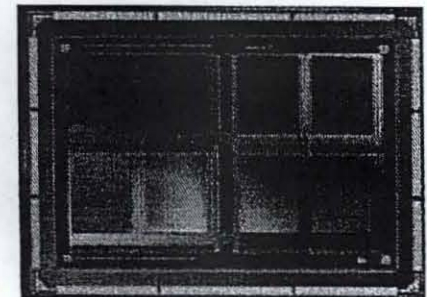
Radiation Hardened Memory

◆ Product Description: Ferroelectric Based Memory (FeRAM)

   o Uses ferroelectric material to store charge by moving a positively charged atom within the crystal lattice.

A
B
O

Cubic Perovskite

◆ Product Description: Chalcogenide Based Memory (C-RAM)

   o Chalcogenide materials store data by having two stable configurations that have different resistance.

Polycrystalline State   Amorphous State

◆ Product Description: Carbon Nanotube Based Memory (NRAM)

   o Carbon Nanotubes are suspended above an anode to which they can be connected with an electrical pulse.

nanotube

100nm
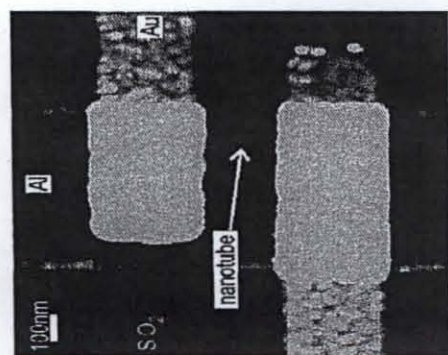
◆ Product Description: Magnetoresistive Random Access Memory (MRAM)

   o MRAM use magne polarization to chai the resistance of a memory cell to sto data.

MagRAM Architecture

Reading a bit

Bit Line
Word Line

Writing "1"
Writing "0"

Word Line
Bit Line
Bit Line
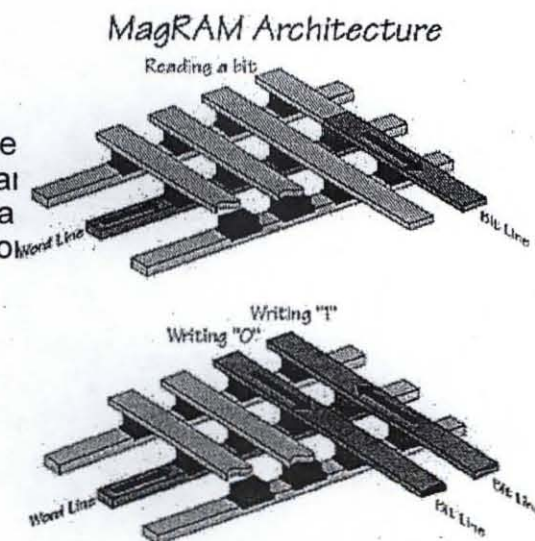
MTJ MagRAM promises
- density of DRAM
- speed of SRAM
- non-volatility

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Radiation Hardened by Software (RHS)

◆ Product will be such an SEE mitigation toolkit, primarily targeting COTS Xilinx FPGAs (e.g. Virtex II or II Pro).

◆ Two approaches:
   o Approach 1: Optimizing Standard Techniques
   o Approach 2: Evolutionary Sub-Circuit Design

◆ Several product components:
   o Radiation-optimized digital sub-circuit library
   o Evolutionary design toolbox that hardens a class of circuits with the ability to recover from a single fault, and
   o Evolutionary design toolbox that hardens a class of circuits with the ability to recover from multiple faults.
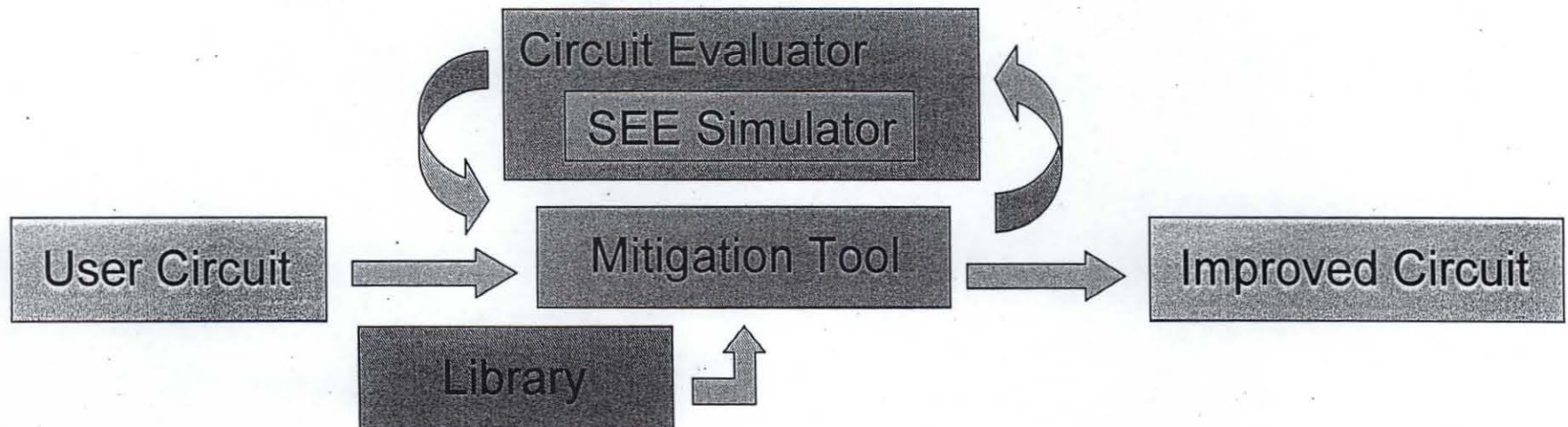
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Technical Justification for Low Temp MEMS

- ◆ Low Temperature Design Challenges
    - ○ behavior of materials at extreme low temperatures not completely understood
        - – brittleness and fatigue
        - – intensified effect of vibration and shock
        - – thermal contraction
            - • delamination concerns
    - ○ parametric characteristics altered
        - – e.g. charge buildup increases pull-in voltages at low temperature in MEMS switches
        - – e.g. resonator, gyroscope drive and sense frequencies sensitive to temperature
- ◆ 'Low Temperature By Design' Benefits
    - ○ increased accuracy and reliability
        - – design specifically for performance at low temperatures
            - • potentially exploit temperature environment as part of the design
        - – direct exposure to environment (e.g. sensors)
    - ○ reduce size, weight, and complexity of protective & environmental packaging
    - ○ also 'temperature harden' existing designs
- ◆ Most COTS MEMS designs were not developed to operate in extreme temperature environments

MEMS Technical Approach: Description

- Optimization using Evolutionary Programming...
  - o Based after neo-Darwinian model (breeding + selection)
    - – 'program instructions' for constructing design, not just parameter optimization
  - o Allows for multi-objective searches and non-symmetrical, non-intuitive designs
  - o Is parallelized and designed to run over an expandable network, and can easily leverage third-party domain-specific simulators
  - o Can compensate for variation in simulated vs. actual performance by incorporating 'noise' and empirical correlations into the evaluation process
  - o Is a 'proven' design approach, utilized for the ST5 antenna
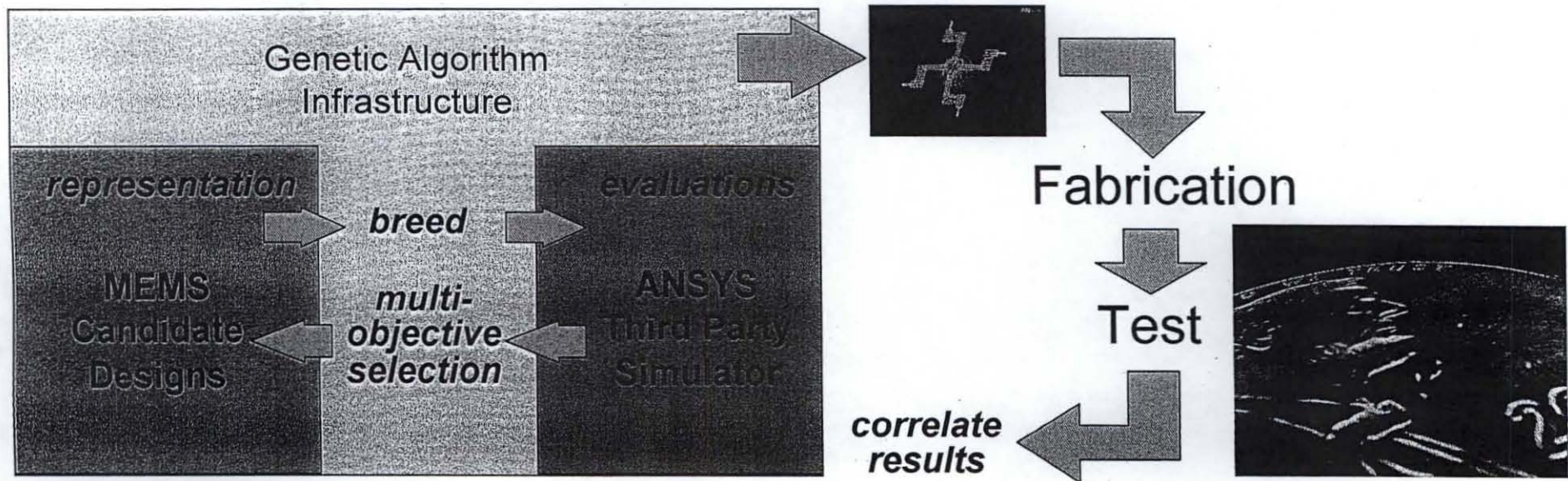
Low-Temperature MEMS Products

◆Specific <u>products</u> provided by this task include:

- o Design rules and algorithms for computer-assisted design of low-temperature MEMS design.
- o A tool for designing multiple classes of temperature-hardened MEMS devices
- o Computer cluster modeling software for MEMS design and simulation.
- o System for automatically evaluating instances of a class of MEMS designs
- o Retooled MEMS design software to include low-temperature capabilities

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Meeting Orion Objectives

◆ **Radiation Hardened Electronics for Space Environments (RHESE)**

◆ Meets **Orion Objectives** through…

- o **High Performance Processors** capable of performing calculation-intensive, time-critical tasks (**cross-technology application to AR&D on Orion**) **within all encountered natural environments** through the development of radiation hardened, low-power, high performance processors.

- o **Reconfigurable Computing** providing the capability for a single electronic board or subsystem to serve multiple applications…
  - – …through a *standardized* interface allowing active and spare boards to be *swapped out* across all architecture elements (**interface modularity** between Orion, multiple individual Lunar Landers, and Lunar Outpost elements).
  - – …through the ability of the board or subsystem to reconfigure dependent on the service needed (**spares modularity** - e.g. DSP, microcontroller, microprocessor). .
  - – …through the ability to **reconfigure** in response to error and failure detections.

- o **Radiation Effects Modeling** providing reliable predictions of radiation effects in electronics in the space environment…
  - – …by modeling the new ways that radiation is found to affect modern electronic components, ways that dominate single event effect rates. These include nucleus-nucleus reactions, simultaneous errors in multiple transistors or in successive clock cycles and device structures that strongly distort charge collection.
  - – …through the update of predictive models of the radiation environment.

◆ **Radiation Hardened Electronics for Space Environments (RHESE)**

◆ Meets **Cargo Launch Project (Ares V) Objectives** through…

o **Radiation Effects Modeling** providing reliable predictions of radiation effects in electronics in the space environment…

  – …by modeling the new ways that radiation is found to affect modern electronic components, ways that dominate single event effect rates. These include nucleus-nucleus reactions, simultaneous errors in multiple transistors or in successive clock cycles and device structures that strongly distort charge collection.

  – …through the update of predictive models of the radiation environment

Meeting Lunar Lander Objectives

◆ **Radiation Hardened Electronics for Space Environments (RHESE)**

◆ **Meets Lunar Lander Objectives** through…

o **High Performance Processors** capable of performing calculation-intensive, time-critical tasks (cross-technology application to **Automated Precision Landing and Hazard Avoidance, Optical Terrain-Relative Navigation and Hazard Avoidance**) **within all encountered natural environments** through the development of radiation hardened, low-power, high performance processors.

o **Reconfigurable Computing** providing the capability for a single electronic board or subsystem to serve multiple applications…

  – …through a *standardized* interface allowing active and spare boards to be *swapped out* across all architecture elements (**interface modularity** between Orion, multiple individual Lunar Landers, and Lunar Outpost elements).

  – …through the ability of the board or subsystem to reconfigure dependent on the service needed (**spares modularity** - e.g. DSP, microcontroller, microprocessor).

  – …through the ability to **reconfigure** in response to error and failure detections.

o **SiGe Materials** (cross-technology application to **Lander Heath Monitoring**) that enable and support externally-distributed, environmentally-exposed electronic units (such as **remote Data Acquisition Units (DAUs), miniaturized sensor nodes,** and **remote control electronics for actuators**) capable of operations in natural environments.

  – Benefits include:

    • Positioned to implement **high-speed wireless (RF)** component/sensor networking, reducing cabling

      » Leverages AFRL investments in SiGe-enabled RF systems.

    • Positioned to implement **low-temperature operations**.

    • Positioned to implement **low-power operations**.

    • **Reduction of cabling** connecting environmentally-protected control electronics to sensors/effectors/drives on lander system extremities.

o **Radiation Effects Modeling** providing reliable predictions of radiation effects in electronics in the space environment…

  – …by modeling the new ways that radiation is found to affect modern electronic components, ways that dominate single event effect rates. These include nucleus-nucleus reactions, simultaneous errors in multiple transistors or in successive clock cycles and device structures that strongly distort charge collection.

  – …through the update of predictive models of the radiation environment.

Meeting Lunar Outpost Objectives

◆ **Radiation Hardened Electronics for Space Environments (RHESE)**

◆ Meets **Lunar Outpost Objectives** through...

o **High Performance Processors** capable of performing calculation-intensive, time-critical tasks (cross-technology application to **Lunar Outpost Autonomous Systems**) **within all encountered natural environments** through the development of radiation hardened, low-power, high performance processors.

o **Reconfigurable Computing** providing the capability for a single electronic board or subsystem to serve multiple applications...

  – ...through a *standardized* interface allowing active and spare boards to be *swapped out* across all architecture elements (**interface modularity** between Orion, multiple individual Lunar Landers, and Lunar Outpost elements).

  – ...through the ability of the board or subsystem to reconfigure dependent on the service needed (**spares modularity** - e.g. DSP, microcontroller, microprocessor).

  – ...through the ability to **reconfigure** in response to error and failure detections.

o **SiGe Materials** (cross-technology application to **Lunar Outpost** and **Lunar Surface Systems Avionics and Health Monitoring**) that enable and support externally-distributed, environmentally-exposed electronic units (such as **remote Data Acquisition Units (DAUs), miniaturized sensor nodes,** and **remote control electronics for actuators**) capable of operations in natural environments.

  – Benefits include:

    • Positioned to implement **high-speed wireless (RF)** component/sensor networking, reducing cabling.

      » leverages AFRL investments in SiGe-enabled RF systems.

    • Positioned to implement **low-power operations**.

    • Positioned to implement **low-temperature operations**.

    • **Reduction of cabling** connecting environmentally-protected control electronics to sensors/effectors/drives on system extremities.

o **Radiation Effects Modeling** providing reliable predictions of radiation effects in electronics in the space environment...

  – ...by modeling the new ways that radiation is found to affect modern electronic components, ways that dominate single event effect rates. These include nucleus-nucleus reactions, simultaneous errors in multiple transistors or in successive clock cycles and device structures that strongly distort charge collection.

  – ...through the update of predictive models of the radiation environment

Meeting EVA Objectives

◆ **Radiation Hardened Electronics for Space Environments (RHESE)**

◆ Meets **EVA Objectives** through...

- o **SiGe Materials** (cross-technology application to **PLSS Heath Monitoring, Power, and Sensor capabilities)** that enable and support externally-distributed, environmentally-exposed electronic units (such as **remote Data Acquisition Units (DAUs)** and **miniaturized sensor nodes**) capable of operations in natural environments.
    - – Benefits include:
        - • Positioned to implement **high-speed wireless (RF)** component/sensor networking, reducing cabling
            - » Leverages AFRL investments in SiGe-enabled RF systems.
            - » Potential to leverage existing suit RF infrastructure.
        - • Positioned to implement **low-power operations**.
        - • **Reduction of cabling** connecting environmentally-protected control electronics to sensors/effectors/drives on suit extremities.
- o **Radiation Effects Modeling** providing reliable predictions of radiation effects in electronics in the space environment...
    - – ...by modeling the new ways that radiation is found to affect modern electronic components, ways that dominate single event effect rates. These include nucleus-nucleus reactions, simultaneous errors in multiple transistors or in successive clock cycles and device structures that strongly distort charge collection.
    - – ...through the update of predictive models of the radiation environment

Presentation Order

- Establishment of the Space Radiation Environment
- Radiation Hardened Electronics for Space Environments (RHESE) Project Overview
- Silicon Germanium (SiGe) Integrated Electronics for Extreme Environments
- Self-Reconfigurable Electronics for Extreme Environments
- Radiation Effects Predictive Modeling
- Radiation Hardened High Performance Processors
- Reconfigurable Computing
- Single Event Effects (SEE)-Immune Reconfigurable Field Programmable Gate Array (FPGA) (SIRF)
- Radiation Hardened Memory
- Radiation Hardened by Software
- Low Temperature Tolerant MicroElectroMechanical Systems (MEMS)
- Exploration Systems Mission Directorate's (ESMD's) Constellation Program Support
- **Summary**

RHESE Summary

- **Space Radiation affects all spacecraft.**
  - o Space electronics have a history of power resets, safing, and system failures due to
    - – Long duration exposures
    - – Unpredictable solar proton activity
    - – Ambient galactic cosmic ray environment
- **All RHESE tasks are "requirements-pulled"** by specific CARD requirements, LAT technology needs, and surface systems' defined environments.
  - o RHESE currently **IS NOT** identified as a need on the Technology Prioritization Panel's listing.
  - o RHESE currently **IS** identified on the LAT enabling and enhancing technology listings.
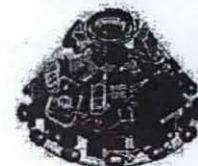- **Radiation and low-temperature environments influence spacecraft system architectures.**
 - o **Centralized systems** to keep electronics warm are costly, weighty and use excessive cable length
  - o Mitigation can be achieved by active **SiGe electronics**.
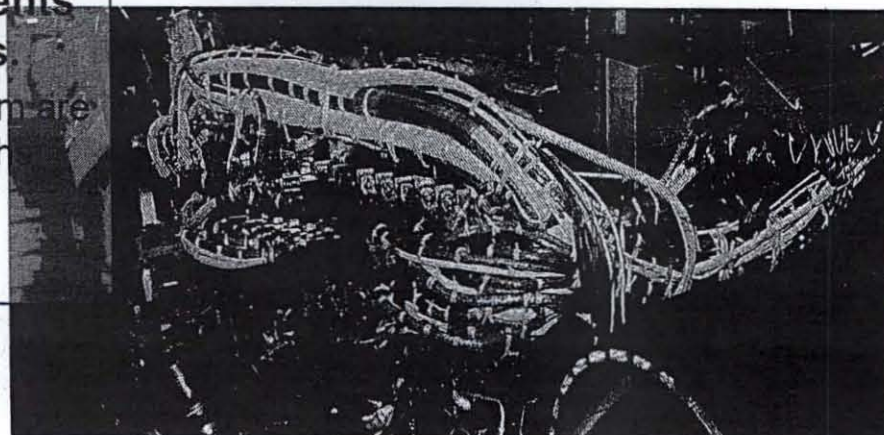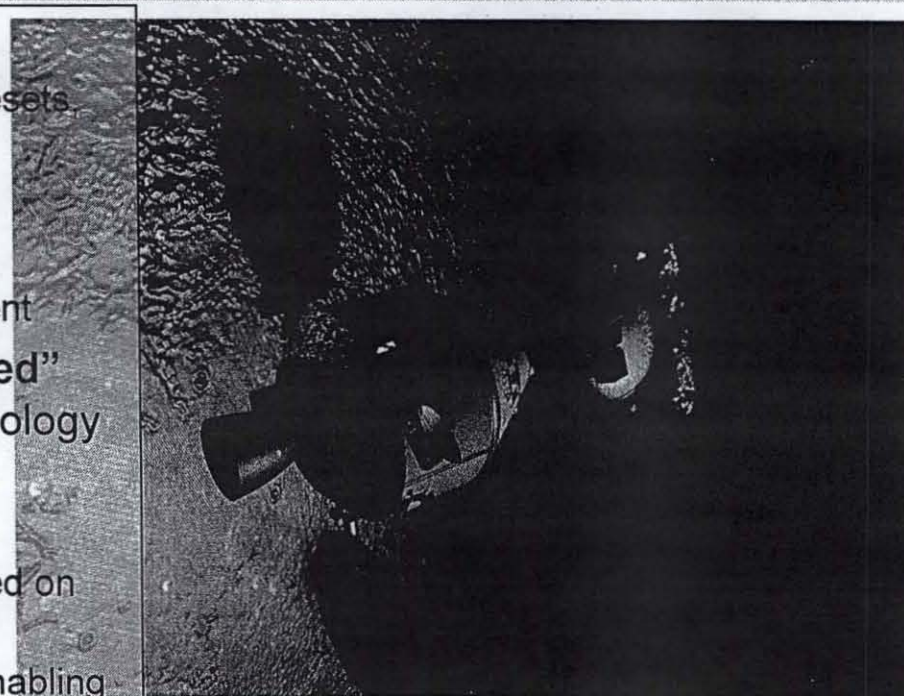
RHESE Summary

- ◆ **An application-dependent trade space is enabled by:**
  - o Radiation Hardening by Architecture using COTS processors, and
  - o Radiation Hardening By Design using Rad-Hard processors.
  - o Considerations include performance requirements, power efficiency, design complexity, radiation hardness.

- ◆ **Radiation Environmental Modeling is crucial** to proper predictive modeling and electronic response to the radiation environment.
  - o When compared to on-orbit data, CREME96 has been shown to be inaccurate in predicting the radiation environment.
  - o The NEDD bases much of its radiation environment data on CREME96 output.

- ◆ **Close coordination and partnership with DoD radiation-hardened efforts** will result in leveraged - not duplicated or independently developed - technology capabilities of:
  - o Radiation-hardened, reconfigurable FPGA-based electronics,
  - o High Performance Processors (NOT duplication or independent development).
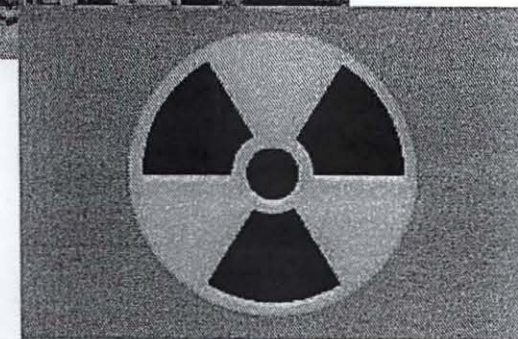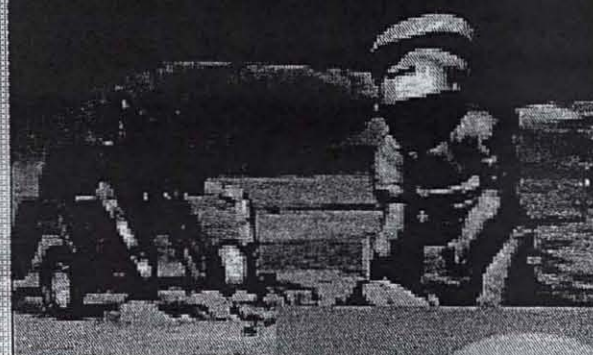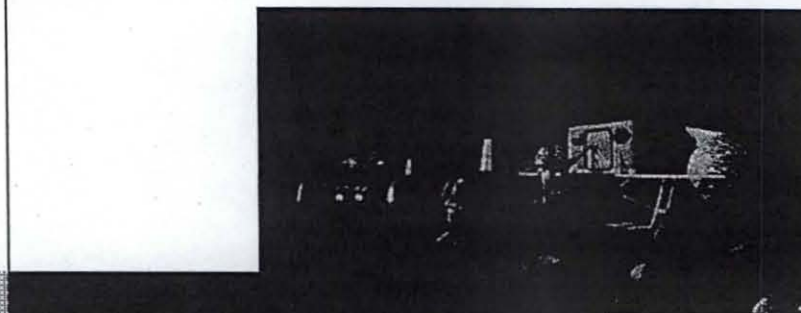
RHESE Provides Solutions to...

◆ ...low-temperature electronic operation in lunar surface environments...
  o ...through the development of SiGe materials tested to temperature extremes of -180C and cycled through temperature extremes.
  o ...through the development of self-reconfigurable electronic circuits that operate in the extreme environment and adapt to the sensed radiation and temperature.

◆ ...the understanding of electronic performance in the radiation environment...
  o ...through the update of predictive models of the radiation environment
  o ...through the ability to model the complex physical architectures of modern electronic components and packaging and their performance in the radiation environment.

◆ ...the need for a single electronic board or subsystem to serve multiple applications...
  o ...through the ability of the board or subsystem to reconfigure dependent on the service needed.
  o ...through the modular packaging interface that is standardized across the onboard avionics.
  o ...through joint participation with AFRL and other DoD agencies in the development and qualification of Field Programmable Gate Array devices capable of emulating electronic subsystems.

◆ ...the need for processors capable of performing calculation-intensive, time-critical tasks (autonomous rendezvous and docking or autonomous hazard avoidance) ...
  o ...through the development of radiation hardened, low-power, high performance processors capable of 2000 MIPS and beyond.
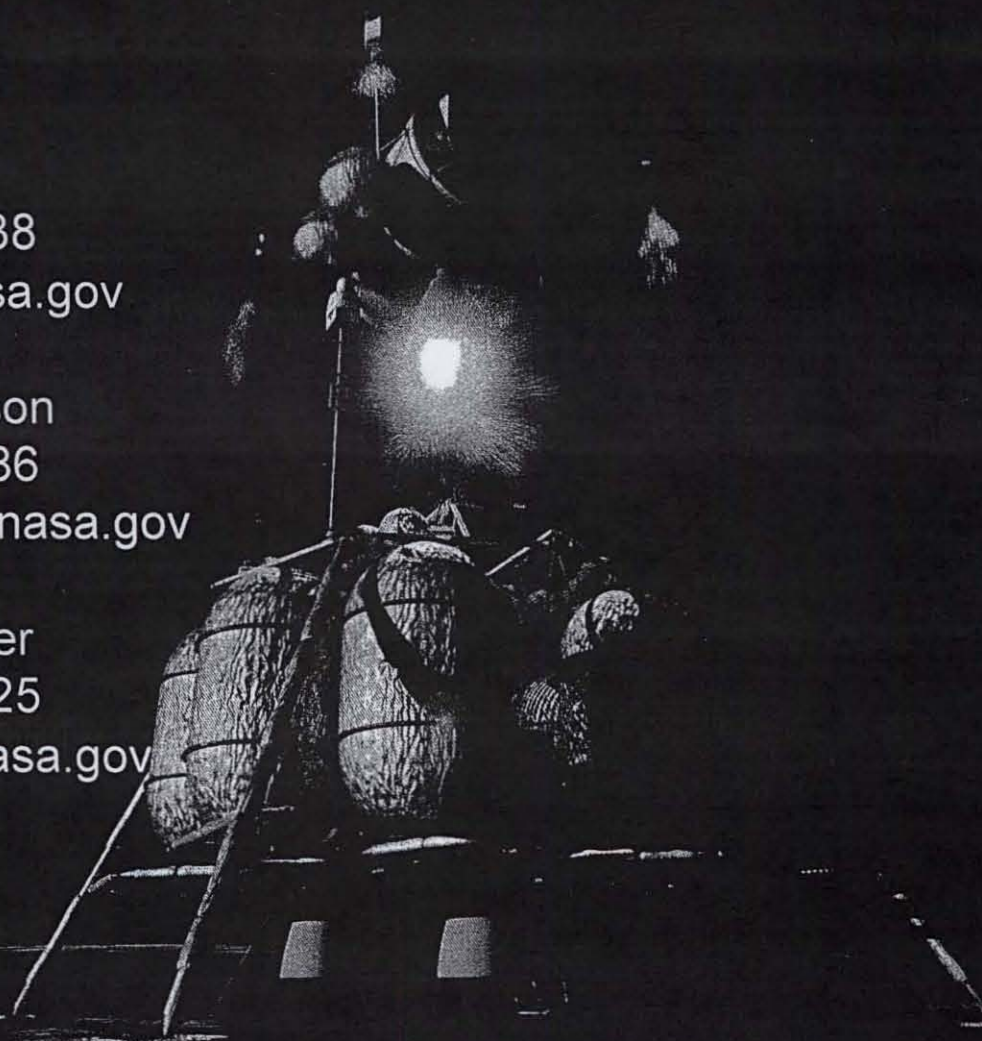
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