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PERFORMANCE MEASUREMENT OF A MULTI-LEVEL/ANALOG FERROELECTRIC MEMORY DEVICE DESIGN

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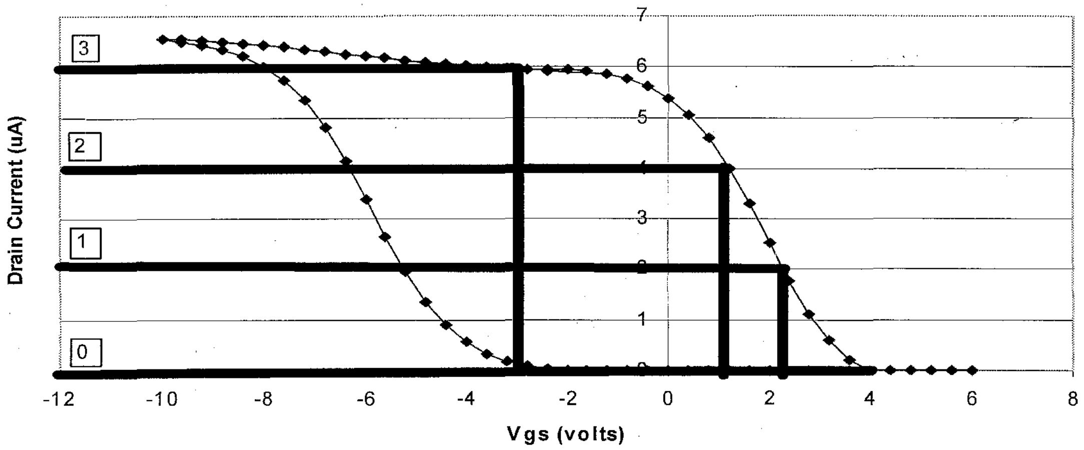
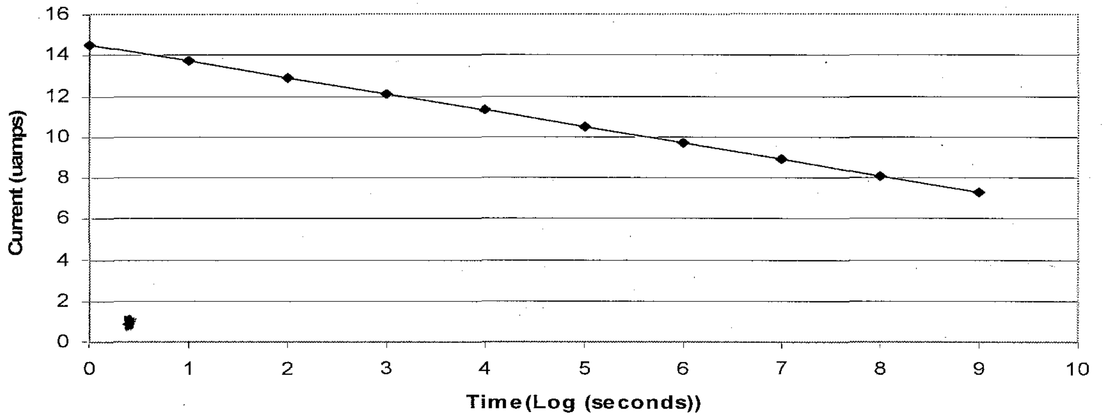
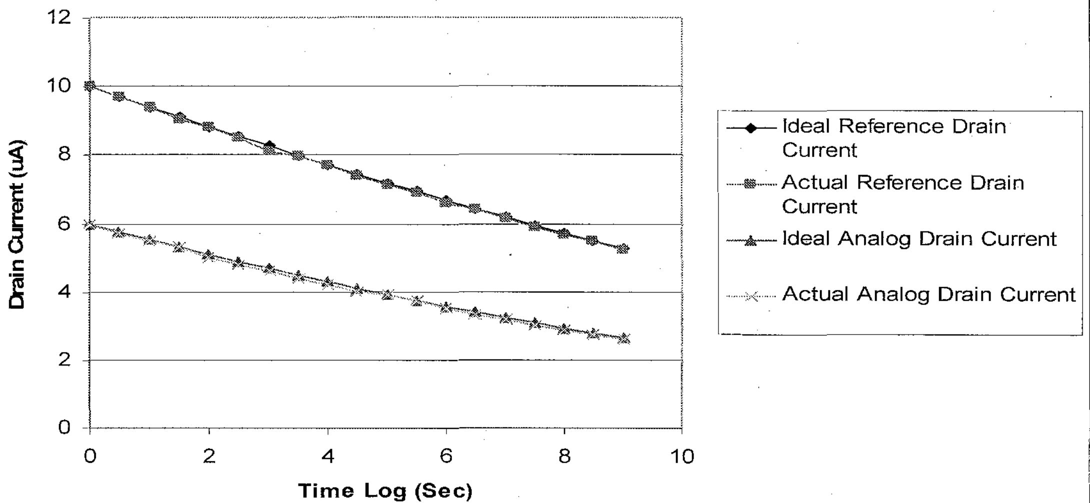
Increasing the memory density and utilizing the unique characteristics of ferroelectric devices is important in making ferroelectric memory devices more desirable to the consumer. This paper describes the characterization of a design that allows multiple levels to be stored in a ferroelectric based memory cell. It can be used to store multiple bits or analog values in a high speed nonvolatile memory. The design utilizes the hysteresis characteristic of ferroelectric transistors to store an analog value in the memory cell. The design also compensates for the decay of the polarization of the ferroelectric material over time. This is done by utilizing a pair of ferroelectric transistors to store the data. One transistor is used a reference to determine the amount of decay that has occurred since the pair was programmed. The second transistor stores the analog value as a polarization value between zero and saturated. The design allows digital data to be stored as multiple bits in each memory cell. The number of bits per cell that can be stored will vary with the decay rate of the ferroelectric transistors and the repeatability of polarization between transistors. This paper presents measurements of an actual prototype memory cell. This prototype is not a complete implementation of a device, but instead, a prototype of the storage and retrieval portion of an actual device. The performance of this prototype is presented with the projected performance of the overall device. This memory design will be useful because it allows higher memory density, compensates for the environmental and ferroelectric aging processes, allows analog values to be directly stored in memory, compensates for the thermal and radiation environments associated with space operations, and relies only on existing technologies.



Model Remnant Drain Current
Drain Current (uA)
Vgs (volts)
3
2
1
0
7
6
5
3
1
-12
-10
-8
-6
-4
-2
0
2
4
6
8



Drain Current vs. Time for a typical FFET
Current (uamps)
Time(Log (seconds))
16
14
12
10
8
6
4
2
0
0
1
2
3
4
5
6
7
8
9
10



Projected Data Measurement of Analog Memory Cell
Drain Current (uA)
Time Log (Sec)
12
10
8
6
4
2
0
0
2
4
6
8
10
Ideal Reference Drain Current
Actual Reference Drain Current
Ideal Analog Drain Current
Actual Analog Drain Current