

National Aeronautics and Space Administration

# Radiation-Hardened Electronics for the Space Environment

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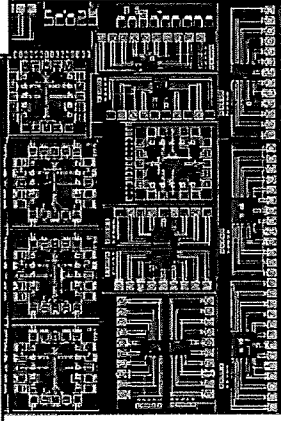
# RHESE Project Overview



## RHESE Project Description:

- The Radiation Hardened Electronics for Space Environments (RHESE) project seeks to advance the current state-of-the-art in **environmentally hardened electronic components** for use in Exploration (Constellation, LPRP) and Science mission applications.
- RHESE investigates a full spectrum of approaches to harden space electronics against **extreme radiation environments**, including:
  - Assessment of new materials,
  - Modeling of the radiation environment and its effects,
  - Hardware self-reconfigurability techniques, and
  - Software design techniques that improve radiation tolerance.
- RHESE additionally investigates rad-hard methods and devices facilitating operation in **low temperature environments** (down to -180C), including:
  - SiGe materials,
  - reconfiguration to counter low-temperature effects, and
  - design approaches to improve low temperature operation.
- **Analog, digital and mixed-mode** electronic systems all benefit from RHESE investments.

CRYO-I Circuit Design from GA Tech

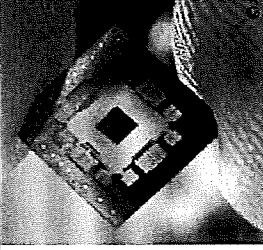


Low Temp Micro-Electromechanical Systems (MEMS)

CRYO-T Center-of-Excellence at GA Tech



Radiation Modeling

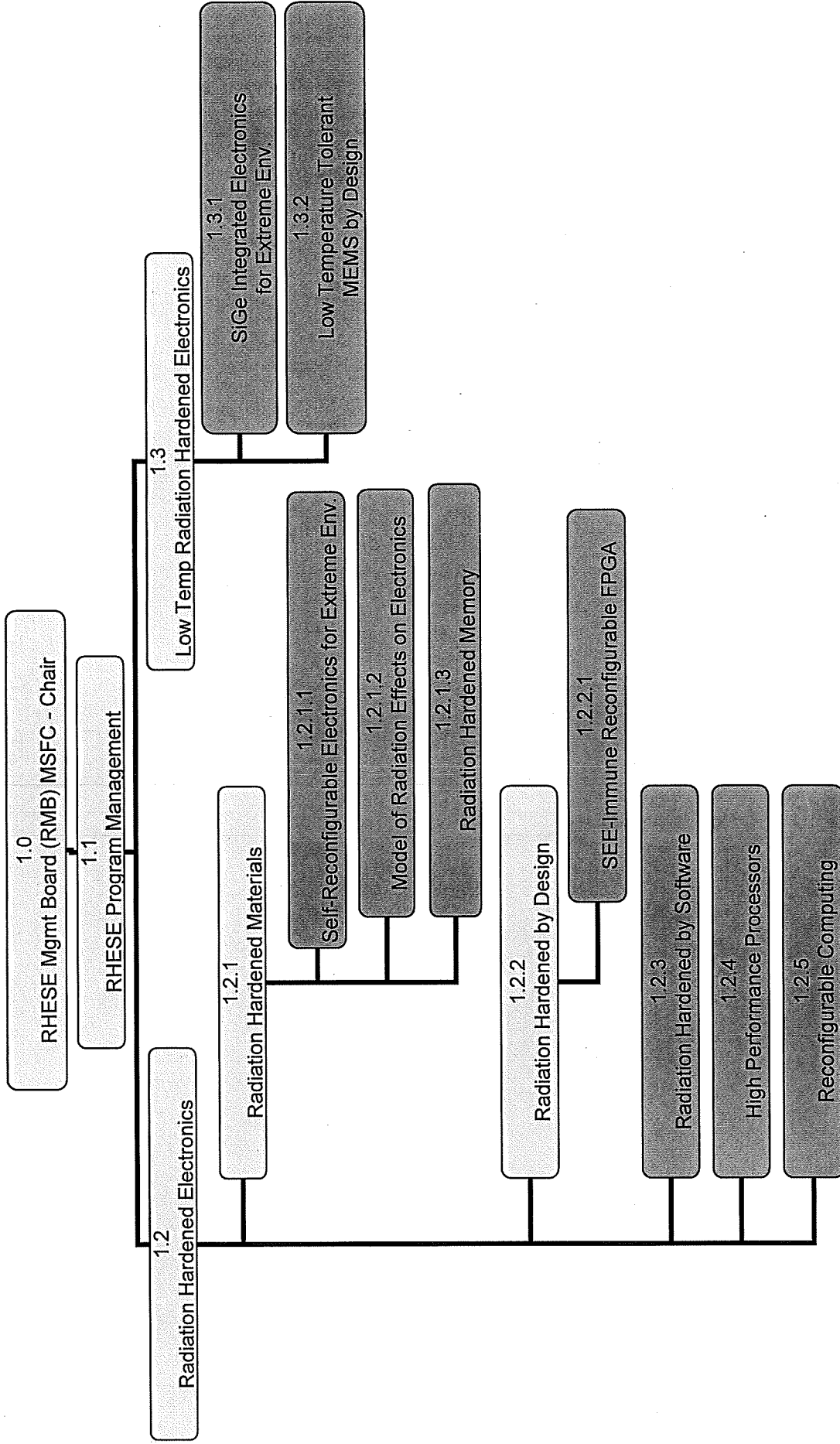


## RHESE Project Tasks:

(Managing NASA Center and Task Implementers)

- (1.2.1.1) **Self Reconfigurable Electronics for Extreme Environments**  
JPL, US Navy SPAWAR, LaRC, Arizona State University
- (1.2.1.2) **Radiation Effects Predictive Modeling**  
MSFC, Vanderbilt University
- (1.2.1.3) **Radiation Hardened Memory**  
MSFC
- (1.2.2.1) **Single Event Effects (SEE) Immune Reconfigurable Field Programmable Gate Array (FPGA) (SIRF)**  
GSFC, AFRL, SNL, University of Idaho, MDA
- (1.2.3) **Radiation Hardened by Software**  
ARC
- (1.2.4) **Radiation Hardened High Performance Processors (HPP)**  
GSFC, JPL, LaRC, MSFC
- (1.2.5) **Reconfigurable Computing**  
MSFC, LaRC
- (1.3.2) **Low Temperature Tolerant MEMS by Design**  
ARC
- (1.3.1) **Silicon-Germanium (SiGe) Integrated Electronics for Extreme Environments**  
LaRC, Georgia Institute of Technology, JPL, Auburn University, BAE Systems, Boeing, IBM, Lynquent Corporation, University of Arkansas, University of Maryland, University of Tennessee, Vanderbilt University

# RHESE Work Breakdown Structure (WBS)





# RHESE Project Content

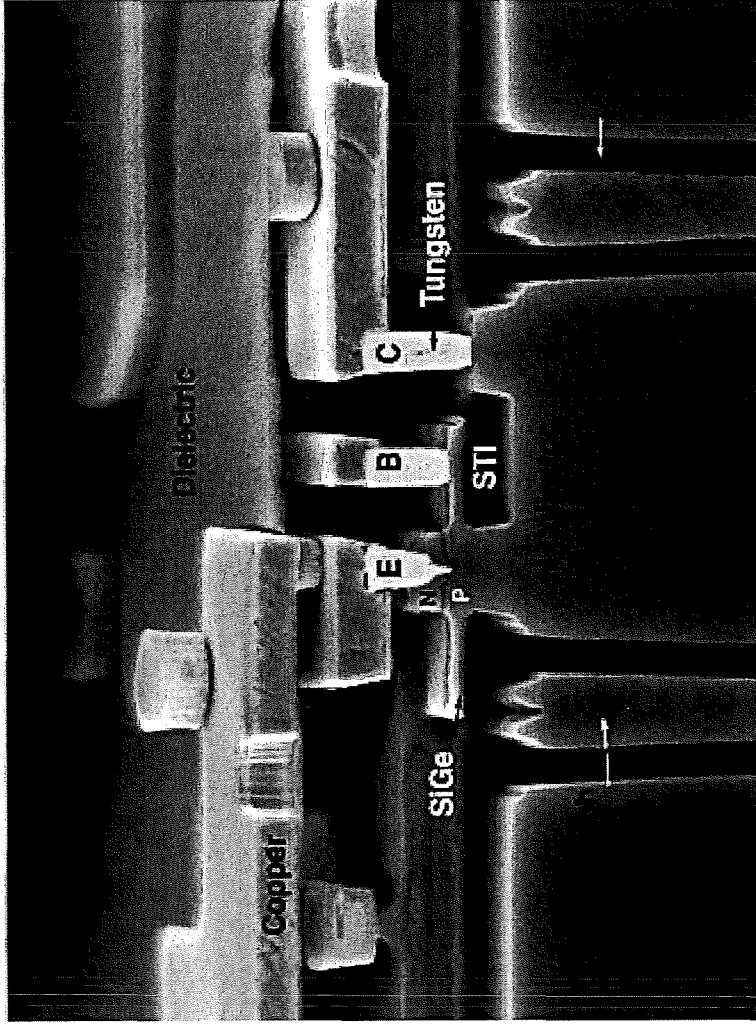
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- **Silicon-Germanium (SiGe) Integrated Electronics for Extreme Environments**
  - Georgia Institute of Technology, JPL, Auburn University, BAE Systems, Boeing, IBM, Lynquent Corporation, University of Arkansas, University of Maryland, University of Tennessee, Vanderbilt University
- **Self Reconfigurable Electronics for Extreme Environments**
  - JPL, US Navy SPAWAR, LaRC, Arizona State University
- **Single Event Effects (SEE) Immune Reconfigurable Field Programmable Gate Array (FPGA) (SIRF)**
  - AFRL, SNL, University of Idaho, MDA
- **Radiation Hardened High Performance Processors (HPP)**
  - GSFC, JPL, LaRC, MSFC
- **Radiation Hardened Memory**
  - MSFC
- **Radiation Hardened by Software**
  - ARC
- **Radiation Effects Predictive Modeling**
  - MSFC, Vanderbilt University
- **Reconfigurable Computing**
  - MSFC, LaRC
- **Low Temperature Tolerant MEMS by Design**
  - ARC



# SiGe Integrated Electronics

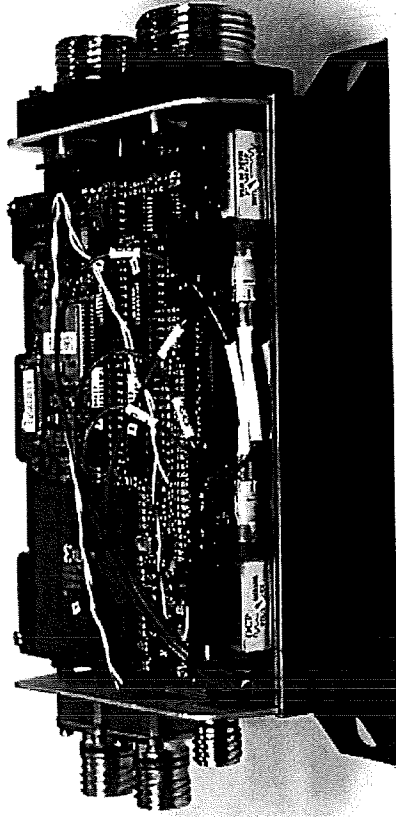
- **OBJECTIVES:** Develop and Demonstrate Extreme Environment Electronic Components Required for Distributed Architecture Lunar / Martian Robotic / Vehicular Systems Using SiGe HBT BiCMOS Technology
- **Extreme Environment Requirements:**
  - +120C (day) to -180C (night) + cycling (main focus)
  - radiation (TID + SEU tolerant)
- **Major Project Goals / Approach:**
  - prove SiGe BiCMOS technology for +120C to -180C applications
  - develop mixed-signal electronics with proven extreme T + rad capability
  - develop best-practice extreme T range circuit design approaches
  - deliver compact modeling tools for circuit design (design suite)
  - deliver requisite mixed-signal circuit components (component library)
  - deliver robust packaging for these circuits (integrated multi-chip module)
  - demonstrate device + circuit + package reliability per NASA specs
  - develop a robust maturation path for NASA mission insertion (TRL-6)
- **Goal: Be Ready for NASA Insertion in 2009**





# SiGe Integrated Electronics

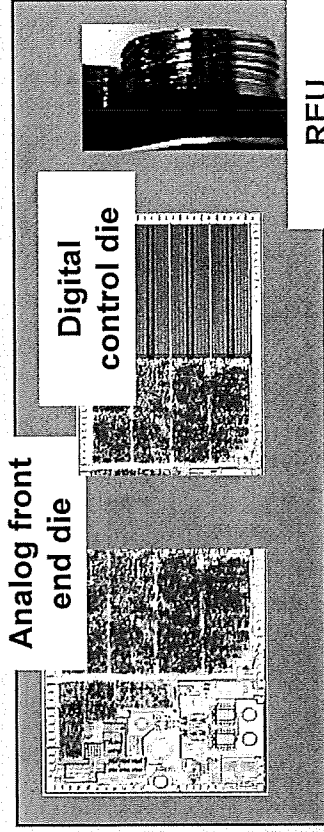
The X-33 Remote Health Unit (circa 1998)



## X-33 Remote Health Unit SPECIFICATIONS:

- 5" wide by 3" high by 6.75" long = 101 in<sup>3</sup>
- 11 kg
- 17.2 Watts dissipated
- -55oC to +125oC

Remote Electronics Unit (circa 2009)

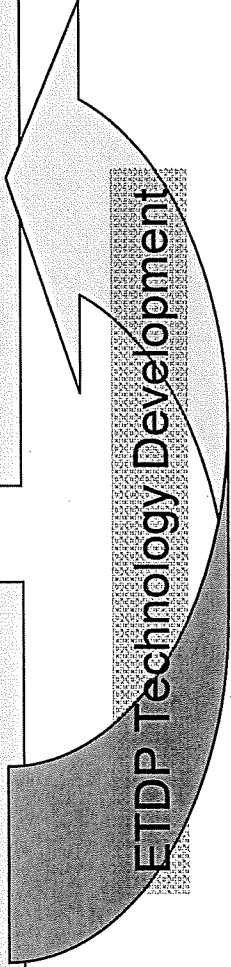


Conceptual integrated REU system-on-chip SiGe BiCMOS die

## SiGe Application

### GOALS:

- 1.5" high by 1.5" wide by 0.5" long = 1.1 in<sup>3</sup>
- < 1 kg
- < 2-3 Watts dissipated
- -180°C to +125°C, radiation tolerant



ETDP Technology Development

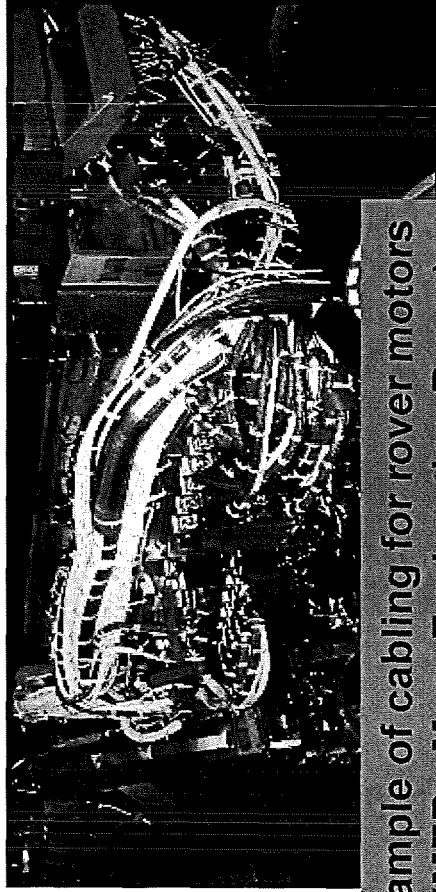


# Self-Reconfigurable Electronics for Extreme Environments

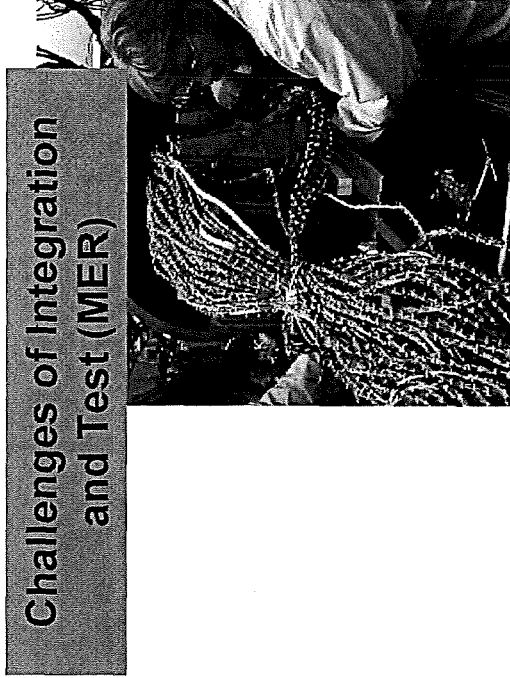
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## PROBLEM STATEMENT:

- **Centralized architectures require all electronics inside a Warm Electronic Box (WEB)**
  - WEB maintains an Earth-like environment (-40 °C to +40 °C) inside
  - Cables required form a jungle of wiring harness
  - Complicated ATLO (Assembly, Test, and Launch Operations)
- **No electronics at extremities (e.g. motors, arms, etc)**



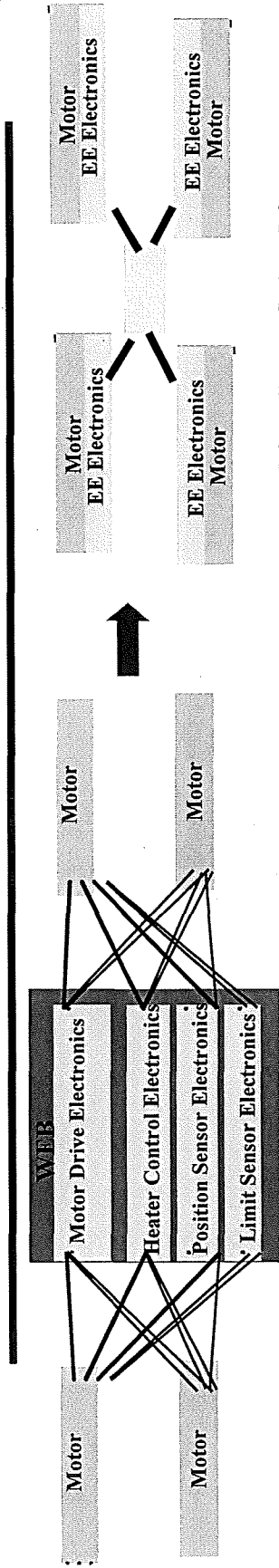
Example of cabling for rover motors  
(MER - Mars Exploration Rover)



Challenges of Integration  
and Test (MER)



# SRE-EE Proposed Solution



**Centralized Architecture**

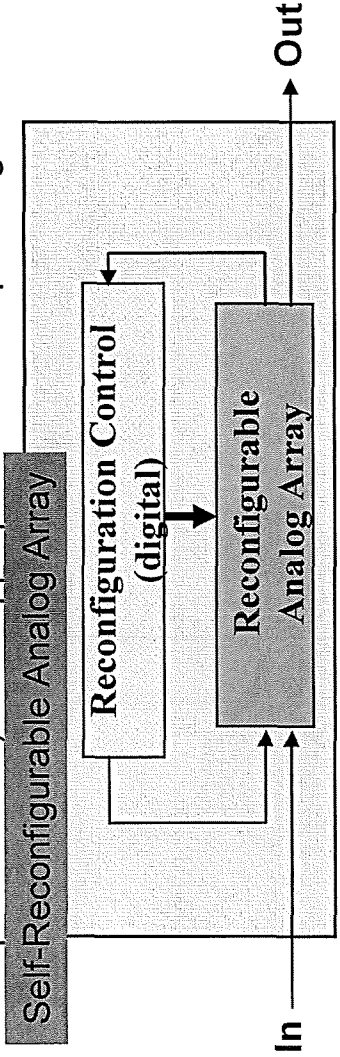
**Distributed Architecture**

	Centralized Architecture (MER)	Distributed Architecture	Estimated Benefits of Distributed Architecture (EE Electronics)
Wire length	~2,500 m	~200 m	~90 % reduction
Number of wires	~1600	~350	~65 % reduction
Modularity	No	Yes	Easier redesign, fab, test, and assembly

- Make electronics self-reconfigurable, adaptive to extreme environments.

- **SRE-EE designs and algorithms will**

- detect degradation in circuit performance due to faults or partial drifts caused by temperature and radiation
- compensate for these faults and drifts by changing to another configuration (either pre-determined or computed in-situ) more appropriate for the operating conditions.





# Single Event Effects (SEE) Immune Reconfigurable Field Programmable Gate Array (FPGA) (SIRF)



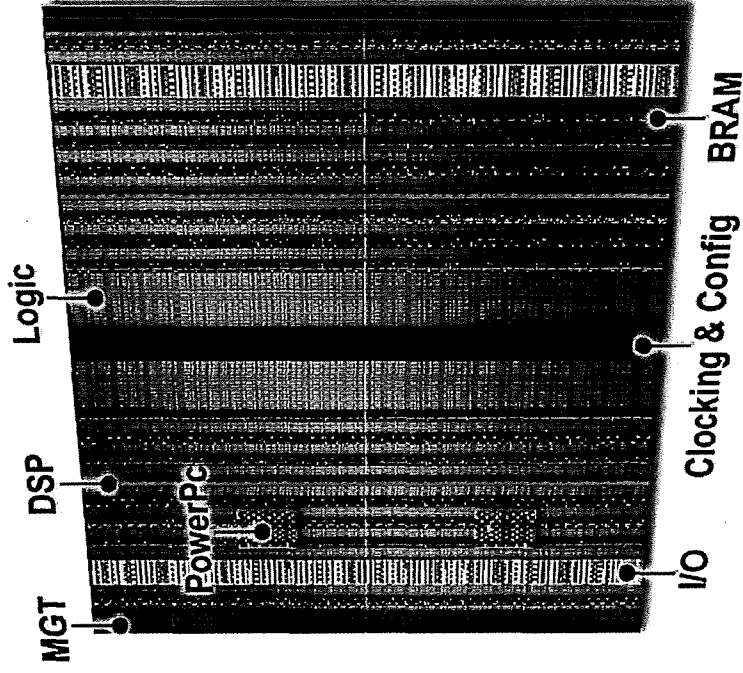
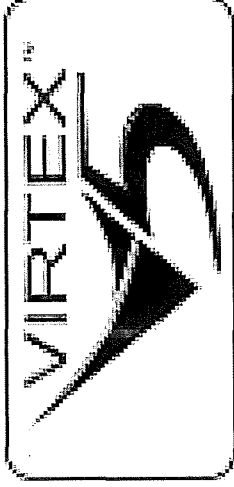
- **Target Device: 5th generation Virtex™ device**

- 65 nm process
- 11 metal layers
- Up to 8M gates

- **Columnar Architecture enables resource “dial-in” of**

- Logic
- Block RAM
- I/O
- DSP Slices
- PowerPC Cores

- **FPGA design techniques developed that produce radiation-tolerant technologies capable of exhibiting**
  - **radiation-tolerant reconfigurable interfaces**
  - **digital interconnects.**

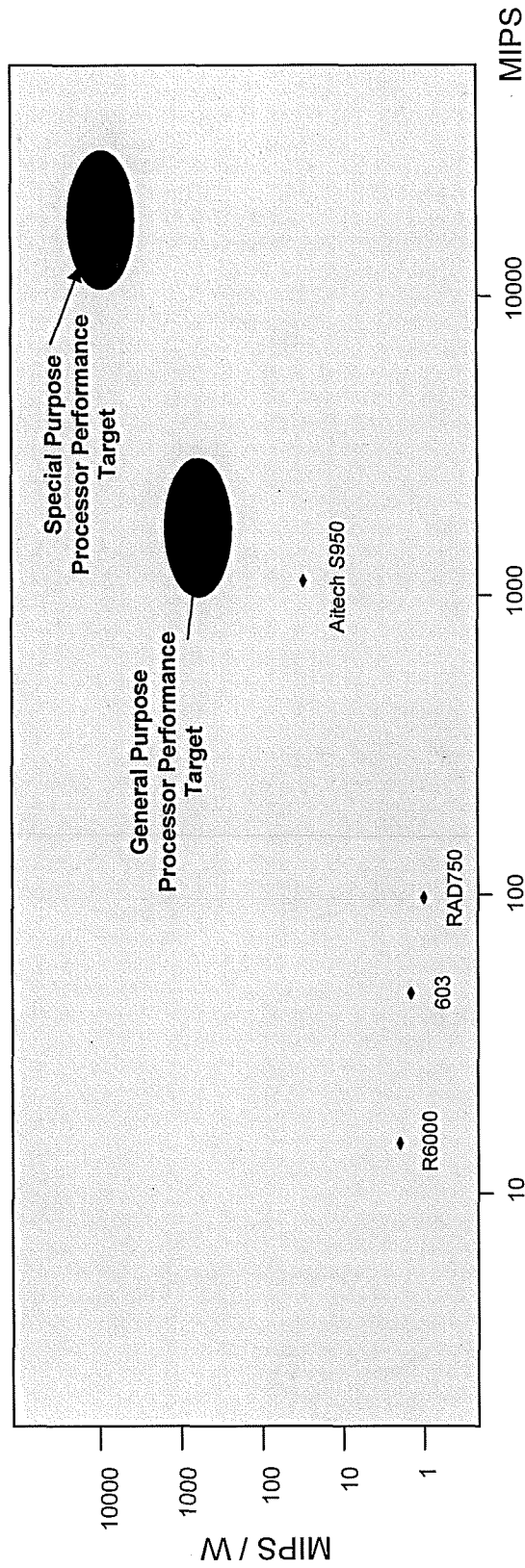


Fabrication process and device architecture yield a high speed, flexible component



# High Performance Processing

- **State of Practice - BAE RAD750 is the “state of the art” radiation-tolerant spacecraft processor**
  - Exhibits ~100 MIPS sustained throughput (compare to >6000 MIPS for Intel Centrino (or recently announced research-grade teraflop, 80-core processor))
  - Radiation tolerant COTS-based boards offer increased performance (~1000 MIPS) at expense of reduced power efficiency
- **Assessment - Processing capability and power efficiency directly affects spacecraft systems performance and implementation options**
  - Autonomous rovers, Entry, Descent and Landing systems, autonomous systems



Performance and Power Efficiency of Current and Targeted Processor Technologies



## High Performance Processing Assessments

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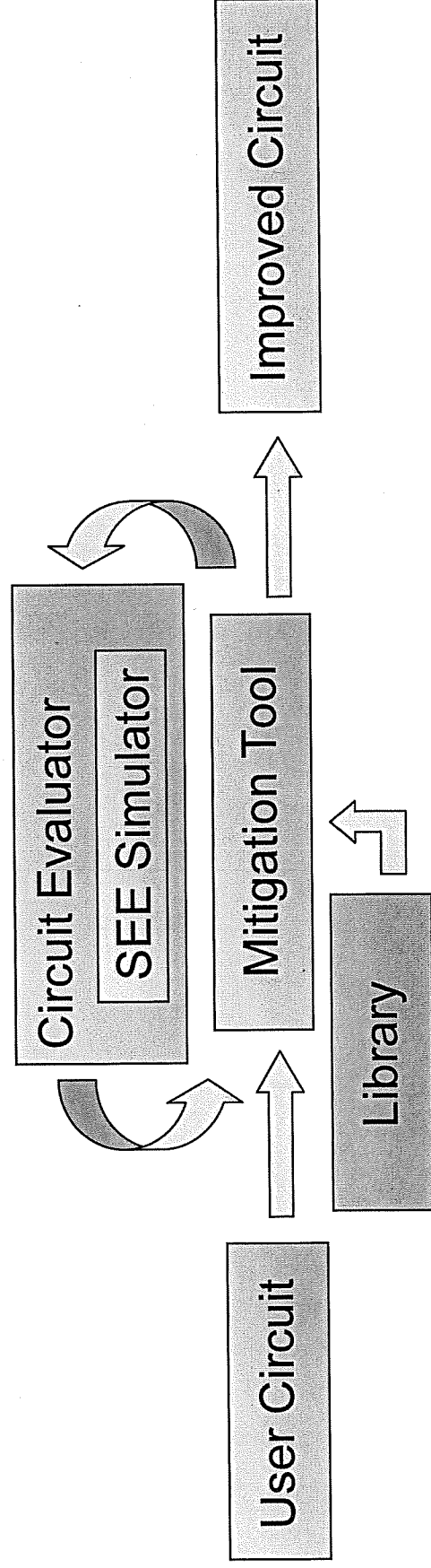
- **Performance of existing spaceflight-capable processors directly affects Exploration systems capabilities**
  - Imposes significant constraints on spacecraft autonomous operations, rover traverses, EDL performance
  - Processor power inefficiency further constrains implementation options and systems feasibility
- **RHESE is addressing this challenge by collaborating with DoD to leverage relevant processor development programs**
  - Technologies under consideration address processor performance and power efficiency metrics
    - Signal processing at greater than **10 GIPS** with less than **2 W** power dissipation
  - Metrics of candidate technologies meet or exceed performance requirements for Exploration systems
  - Power efficiency of candidate technologies facilitates systems implementation in severely power-constrained environments
- **Specific products for this task:**
  - High-performance (2000 MIPS, 500 MIPS/W) radiation hardened processors for space application.
- **High Performance Processor technologies targeting system-level**



## Radiation Hardened by Software (RHS)

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- Product will be such an SEE mitigation toolkit, primarily targeting COTS Xilinx FPGAs (e.g. Virtex II or II Pro ).
- Two approaches:
  - Approach 1: Optimizing Standard Techniques
  - Approach 2: Evolutionary Sub-Circuit Design
- Several product components:
  - Radiation-optimized digital sub-circuit library
  - Evolutionary design toolbox that hardens a class of circuits with the ability to recover from a single fault, and
  - Evolutionary design toolbox that hardens a class of circuits with the ability to recover from multiple faults.





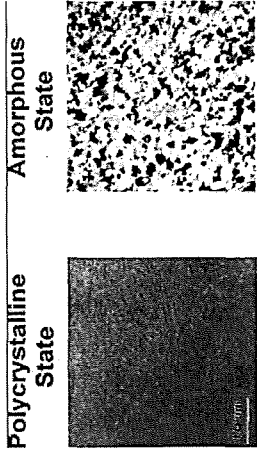


# Radiation Hardened Memory

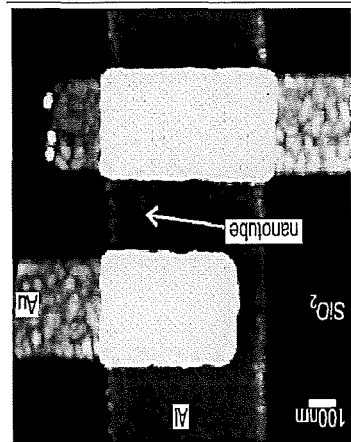
- Product Description: Ferroelectric Based Memory (FeRAM)**
  - Uses ferroelectric material to store charge by moving a positively charged atom within the crystal lattice.

Cubic Perovskite

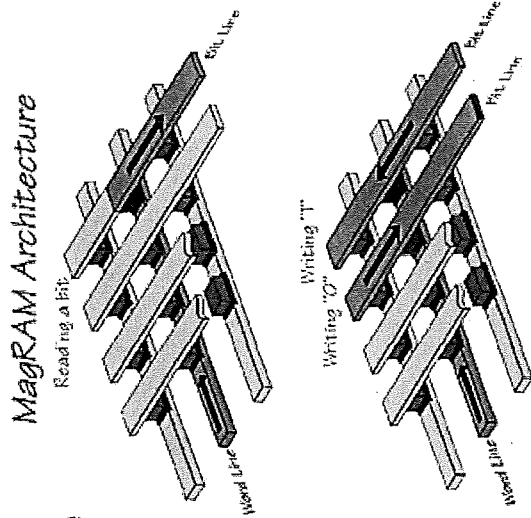
- Product Description: Chalcogenide Based Memory (C-RAM)**
  - Chalcogenide materials store data by having two stable configurations that have different resistance.



- Product Description: Carbon Nanotube Based Memory (NRAM)**
  - Carbon Nanotubes are suspended above an anode to which they can be connected with an electrical pulse.



- Product Description: Magnetoresistive Random Access Memory (MRAM)**
  - MRAM use magnetic polarization to change the resistance of a memory cell to store data.



MTJ MagRAM promises

- density of DRAM
- speed of SRAM
- non-volatility

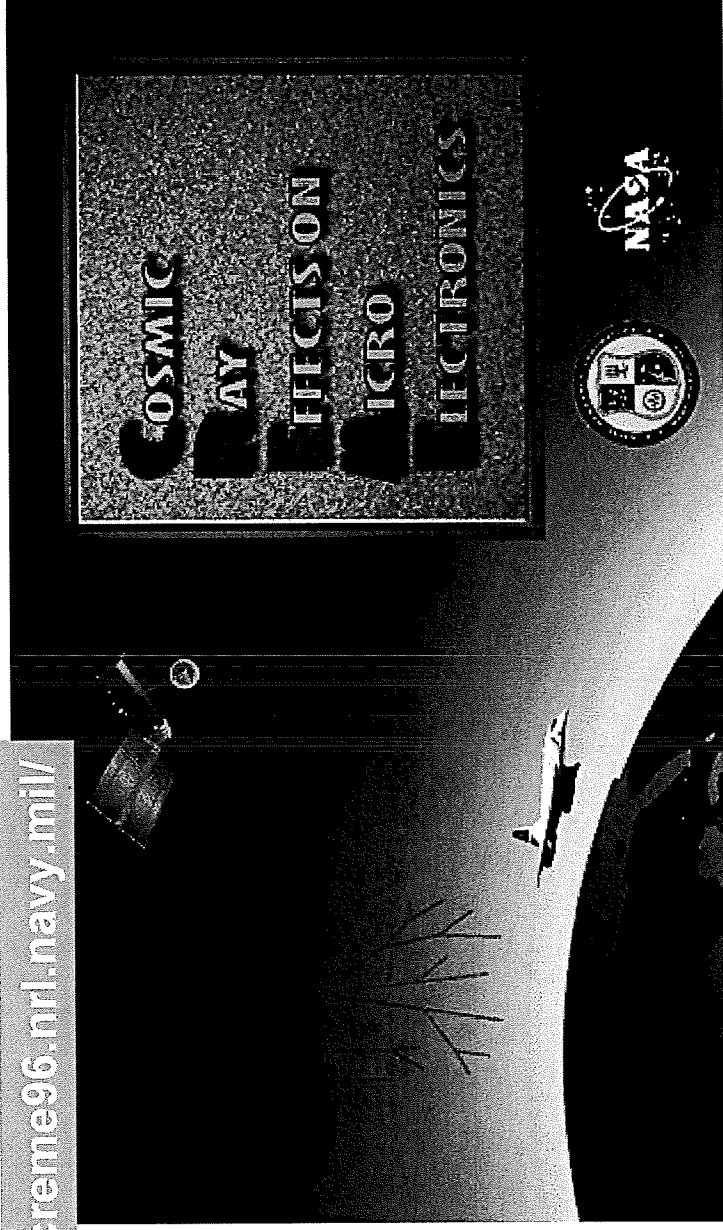


## Radiation Modeling

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- **The Single Event Effect (SEE) prediction models currently in use were developed ~10 years ago.**
  - They were written when feature sizes were  $>1 \mu\text{m}$
  - Devices did not contain heavy metals
  - Microcircuits were not complex 3-D structures
  - These models are not reliable for modern devices
- **Current radiation model available:**

<https://creme96.nrl.navy.mil/>





## **Radiation Modeling Objectives**

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- **Provide accurate evaluations radiation effects in space**
  - By understanding how specific device technologies respond to ionizing radiation,
  - By providing the ability for designers to accurately predict a mean-time-between-failure for components and sub-systems, and
  - By providing a computational tool to estimate mission-specific total dose and SEE rates.
- **Improve External Radiation Environment Descriptions**
  - Galactic cosmic rays
  - Solar energetic particles
  - Anomalous cosmic rays
- **Improve Radiation Transport through Spacecraft**
  - Full Monte Carlo radiation transport
- **Provide a Physics-Based Simulation Tool of Single-Event Effects**
  - Correctly treat hole-electron plasma creation
  - Charge collection
  - Circuit response
- **Make the computational tool available to designers through the internet.**



## **Reconfigurable Computing**

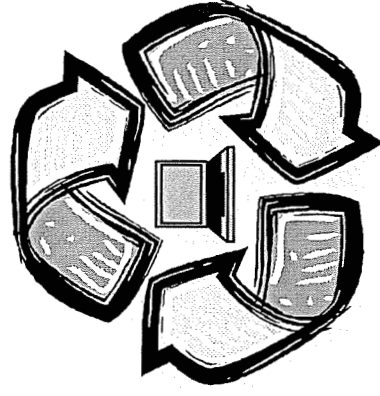
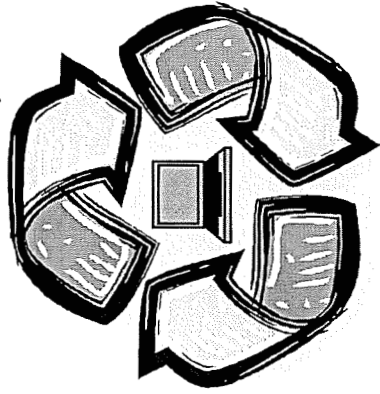
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- **Flight-Qualified, Multi-String Redundant Hardware is Expensive**
  - Development, Integration, IV&V, and Flight Qualification
  - Space and Weight
  - Power Consumption
  - Dissimilar Spares
- **“From Scratch” Design of Computing Resources for Every New Flight System is Unnecessary and Wasteful**
- **Requirements for Flexibility are Increasing and Smart**
  - Reconfigurable and Modular Capabilities
  - Capacity to use one system to back up any number of others
  - General Reusability
- **Current Options for Harsh/Flight Environment Systems are Limited**
  - Custom Hardware, Firmware, and Software
  - Dedicated and Inflexible
  - Often Proprietary



# Reconfigurable Computing Products

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- **Specific products and applications of this task will include:**
  - Reconfigurable processors supporting multiple architectures to enable single spares to fulfill multiple electronic functions.
  - Reconfigurable processors supporting avionics redundancy by providing adaptable spares.
  - Reconfigurable processors supporting recovery from component damage by radiation strikes and other events.
  - Reconfigurable processors supporting multiple interfacing and interconnection options.



## Technical Justification for Low Temp MEMS

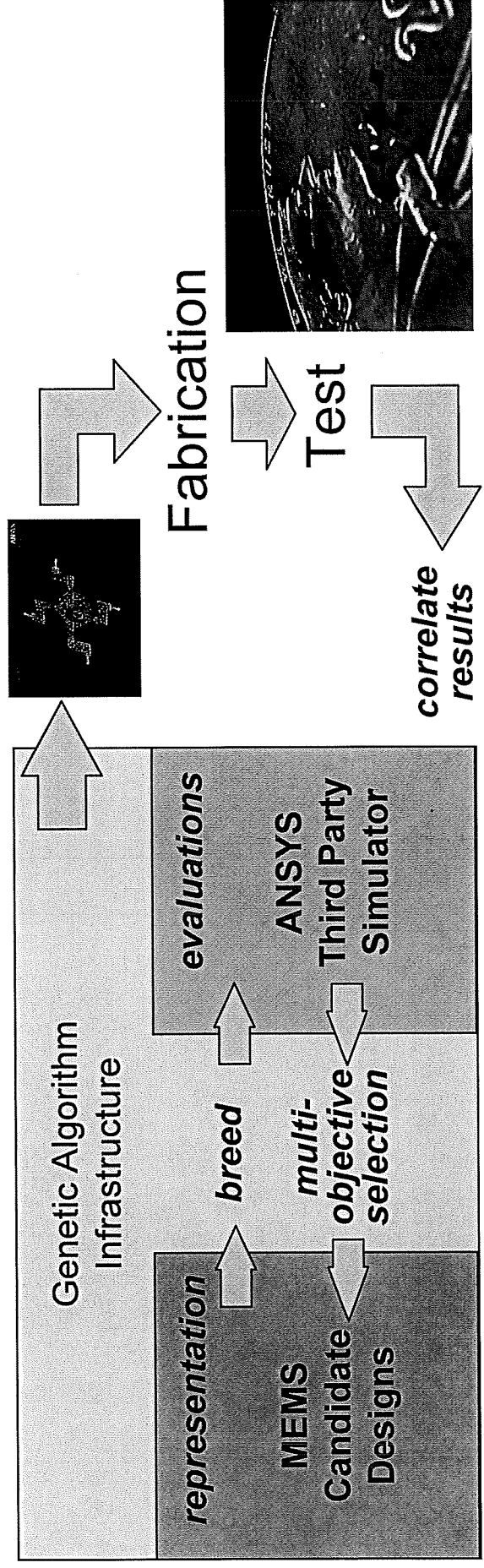
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- **Low Temperature Design Challenges**
  - behavior of materials at extreme low temperatures not completely understood
    - brittleness and fatigue
    - intensified effect of vibration and shock
    - thermal contraction
      - delamination concerns
    - parametric characteristics altered
    - e.g. charge buildup increases pull-in voltages at low temperature in MEMS switches
    - e.g. resonator, gyroscope drive and sense frequencies sensitive to temperature
- **'Low Temperature By Design' Benefits**
  - increased accuracy and reliability
    - design specifically for performance at low temperatures
      - potentially exploit temperature environment as part of the design
    - direct exposure to environment (e.g. sensors)
  - reduce size, weight, and complexity of protective & environmental packaging
    - also 'temperature harden' existing designs
- **Most COTS MEMS designs were not developed to operate in extreme temperature environments**



## MEMS Technical Approach: Description

- **Optimization using Evolutionary Programming...**
  - Based after neo-Darwinian model (breeding + selection)
    - 'program instructions' for constructing design, not just parameter optimization
  - Allows for multi-objective searches and non-symmetrical, non-intuitive designs
  - Is parallelized and designed to run over an expandable network, and can easily leverage third-party domain-specific simulators
  - Can compensate for variation in simulated vs. actual performance by incorporating 'noise' and empirical correlations into the evaluation process
  - Is a 'proven' design approach, utilized for the ST5 antenna





## **Low-Temperature MEMS Products**

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- **Specific products provided by this task include:**
  - Design rules and algorithms for computer-assisted design of low-temperature MEMS design.
  - A tool for designing multiple classes of temperature-hardened MEMS devices
  - Computer cluster modeling software for MEMS design and simulation.
  - System for automatically evaluating instances of a class of MEMS designs
  - Retooled MEMS design software to include low-temperature capabilities





## RHESE Summary

- **RHESE covers a broad range of technology areas and products.**
  - Radiation Hardened Electronics
  - High Performance Processing
  - Reconfigurable Computing
  - Radiation Environmental Effects Modeling
  - Low Temperature Radiation Hardened Electronics
- **RHESE has aligned with currently defined customer needs.**
- **RHESE is leveraging/advancing SOA space electronics, not duplicating.**
  - Awareness of radiation-related activities through out government and industry allow advancement rather than duplication of capabilities.

- Current Leveraging Efforts
  - NASA Electronics Parts Program (NEPP)
    - SiGe Integrated Electronics
    - Radiation Effects Predictive Modeling
  - Defense Threat Reduction Agency (DTRA)
    - High Performance Processing
    - Radiation Environment Effects Modeling
    - SiGe Integrated Electronics
  - Defense Advanced Research Programs Agency (DARPA)
    - High Performance Processors
    - Mixed Signal Analog Devices
  - Department of Energy
    - High Performance Processing
    - Radiation Hardened FPGA
  - Air Force Research Laboratory (AFRL)
    - Reconfigurable Computing
    - Radiation Hardened FPGA
  - Naval Research Laboratory (NRL)
    - High Performance Processing
  - IBM
    - Low Temperature Electronics
  - BAE Systems
    - Low Temperature Electronics
  - Honeywell
    - Radiation Hardened Electronics
  - Vanderbilt University
    - Radiation Environment Effects Modeling
  - Brigham Young University
    - FPGA Design Software
  - Arizona State University
    - Power Efficient FPGA Design
  - University of Idaho
    - High Performance Processing

## Contact Information

For additional information on the Radiation-Hardened Electronics for Space Environments (RHESE) project, please contact:

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