

# Design of Low Power CMOS Read-Out with TDI Function for Infrared Linear Photodiode Array Detectors

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**Abstract**— A new low voltage CMOS infrared readout circuit using the buffer-direct injection method is presented. It uses a single supply voltage of 1.8 volts and a bias current of 1 $\mu$ A. The time-delay integration technique is used to increase the signal to noise ratio. A current memory circuit with faulty diode detection is used to remove dark current for background compensation and to disable a photodiode in a cell if detected as faulty. Simulations are shown that verify the circuit that is currently in fabrication in 0.5 $\mu$ m CMOS technology.

## I. INTRODUCTION

Readout circuits for infrared imagers have many commercial, scientific and military applications which are continually expanding [1]-[5]. The main function of an infrared readout circuit is to transform a very small (nAs) diode incremental current, generated by infrared radiation, into a relatively large measurable output voltage. This is commonly done by integrating the photocurrent in a small capacitor during a fixed period of time. The capacitor's voltage at the end of the integration period should be proportional to the current and as such to the incident infrared radiation at a pixel corresponding to the location of the infrared diode photo sensor. Infrared imagers consist of linear or two dimensional arrays including a very large number of infrared photo sensors. These arrays are denoted linear or focal plane arrays (FPAs). Given that in the most general case each pixel of an image requires an individual readout circuit, the electronics associated to an infrared imager consists of a very large number (thousands) of readout circuits. The basic readout circuit is denoted "unit cell". Readout electronics is implemented as very large scale custom integrated circuits or ASICs in CMOS technology. Due to the fact that infrared imagers can have several thousand unit cells, the unit cell is required to be very compact, to have very low power dissipation and at the same time to have high performance characteristics. A versatile buffer direct injection (BDI) circuit has been conceived with several innovative features: 1) low single supply voltage

( $V_{DD}=1.8V$ ) and uses an amplifier with a very low quiescent current (1 $\mu$ A); 2) low input resistance ( $<1k\Omega$ ) this in spite of the very small input currents achieved by the injection amplifier which has a high GB; 3) incorporates a compact current memory cell for background compensation; 4) utilizes a shared buffer amplifier to minimize area for the purposes of time-delay integration (TDI). The TDI technique integrates the current from each pixel over several periods. This allows the integration to take place over a longer time giving a more reliable output. The TDI technique reduces the noise by a factor  $\sqrt{N}$  where N is the number of integration periods per pixel [6]. The current memory cell is used for background compensation. This is required to prevent the dark current from being integrated along with the photocurrent signal. This allows the utilization of a smaller integrating capacitor and improves dynamic range.

## II. PROPOSED CIRCUIT

### A. Buffered Direct Injection Circuit Design

The scheme of a buffered direct injection readout unit cell is shown in Figure 1. The IR diode is modeled as a current source in parallel with a shunt resistance  $R_0$  and a shunt capacitance  $C_0$ . Transistor M1 is used as a current buffer to pass the diode photocurrent to the integrating capacitor. In order to achieve high current efficiency from the diode it is required that the input impedance,  $R_x$ , be much less than  $R_0$ . A practical problem in direct injection readout circuits is that with extremely small input currents, the input resistance of M1 in the common gate configuration (given by  $R_{in} = 1/g_m$ ) can take very high values ( $R_{in} \sim 10M\Omega$ ). This can lead to very poor current efficiency and low dynamic range. Amplifier A is used to accurately set the voltage  $V_x$  used as the photodiode bias voltage. With very little fluctuations in  $V_x$ , amplifier A establishes a virtual ground in which the photodiode can efficiently inject current. Buffer  $B_A$  serves all the amplifiers in a large array of unit cells. Other approaches attempt to generate a low impedance

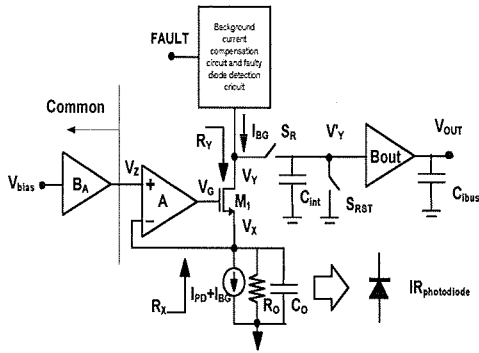


Figure 1. Unit cell readout using Buffered Direct Injection scheme

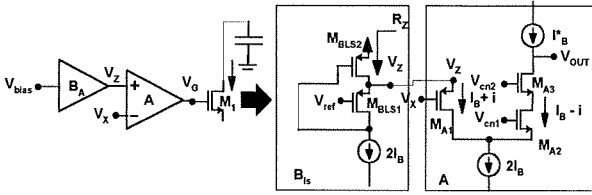


Figure 2. CMOS implementation of buffer BA and amplifier A.

common source node using a conventional voltage follower. This is highly inefficient since the voltage follower requires very high bias current and large transistor sizes in order to generate a very low impedance node with impedance  $R_z = 1/g_m$ . This problem is solved by the inclusion of the compact and low power buffer BA which offers two orders of magnitude lower output impedance than a conventional voltage follower:  $R_z = 1/(g_m(g_m r_o))$ . The shared buffer conserves area by sharing BA with all the amplifiers A in a readout array, and reducing the hardware requirements for amplifier A. Figure 2 shows the configuration of buffer BA and amplifier A.

### B. Implementation of Buffer BA and Amplifier A

The buffer BA is implemented using a flipped voltage follower and is used as the shared element as it serves all the amplifiers A in a readout array. This buffer has an output node with a constant voltage  $V_Z = V_{bias} + V_{SG}$ . Amplifier A is used in the BDI scheme to boost the input conductance (and the output impedance) at the source of M1 by the gain A. Amplifier A is implemented using a single ended folded double cascoded amplifier with the source terminal of the input transistor MA1 connected to the low impedance node VZ serving as virtual ground for the source of MA1. Due to the double cascoding the open loop gain A has a very high value,  $A = (g_m r_o)^3 \approx 10^4 - 10^5$ . This high gain is needed due to the very high input impedance ( $\sim 10M\Omega$ ) of M1. By using the buffered injection scheme the input impedance of M1 is reduced to a value  $R_x \approx R_{in}/A \approx 500\Omega$ .

### C. Line Output Buffer

The line output buffer, Bout, is required to transfer the voltage signal from the small integration capacitor Cint to an output bus that has a large parasitic capacitance. It will

prevent errors in the readout signal due to charge redistribution. The output buffer should have the following characteristics:

- Very low static power dissipation
- Very compact circuit
- Very high slew rate so that it is capable of providing high dynamic currents to charge the large capacitance of the output bus
- If possible, there should be no DC level shift between the input and output buffer terminals.

One of the two line buffers reported in [8]-[9] is used as the line buffer because of the characteristics needed by this application.

### D. Current Memory Cell with Faulty Diode Detection

Figure 3 shows the memory cell circuit with faulty diode detection. The current memory cell is used for background compensation. The most important problems for background compensation are the possibly large errors due to charge injection when storing very small currents [10]-[11]. This is due to the fact that with these small currents, transistor M1 operates either in weak or moderate inversion. This causes the drain current to be exponentially dependent on VGS. Small changes in VGS introduced by charge injection of switch S2 can lead to very large changes in the current generated by M1 during the readout phase. In order to improve accuracy and make the memory cell less sensitive to charge injection errors, the circuits in Figure 4 store an amplified version of the background current, IBK, in a relatively small transistor M3. Due to its small W/L and larger stored current, KI BK, this transistor operates in saturation with a relatively large VGS. For this reason it is less sensitive to charge injection errors. Operation of the current amplified cells is as follows: During the sampling phase the current is mirrored with gain K from M1 to the branch with M2 and M3 and stored in the form of a voltage VGS at CMEM. During the readout phase the direction of the mirror reverses. The current generated by M3 is now mirrored from M2 to M1 with gain 1/K and subtracted from the

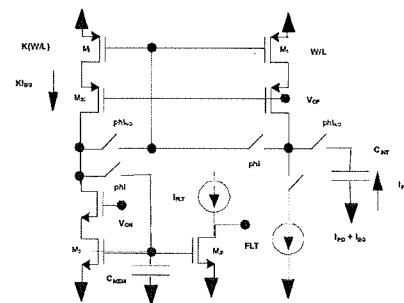


Figure 3. Amplified storage cell using gain K mirror.

diode current  $ID_{MI}=I_{BK}+I_{PD}$ . The cell also incorporates circuitry for faulty diode detection. A high is generated at terminal FLT in case  $I_{BG}>I_{FLT}$ . This indicates that the photodiode has an abnormal high background current (or low impedance) and it is for this reason considered a faulty diode. If a high is detected signal FLT can be used to disable the diode from the array.

### III. SIMULATION RESULTS

Simulations have been done using the integrated circuit design environment “Cadence.” The design was done using  $0.5\mu\text{m}$  CMOS (AMI-MOSIS) technology. All PMOS transistors were sized at 13/1 and all NMOS transistors were sized at 5/1 except for the switches, which have minimum feature sizes. Figure 4 shows the voltage across the integrating capacitor with an input photodiode current of 10 nA. The linearity of the current to voltage conversion is shown in Figure 5. Figure 6 shows the layout of the circuit which has four main sections representing four cells in the BDI scheme.

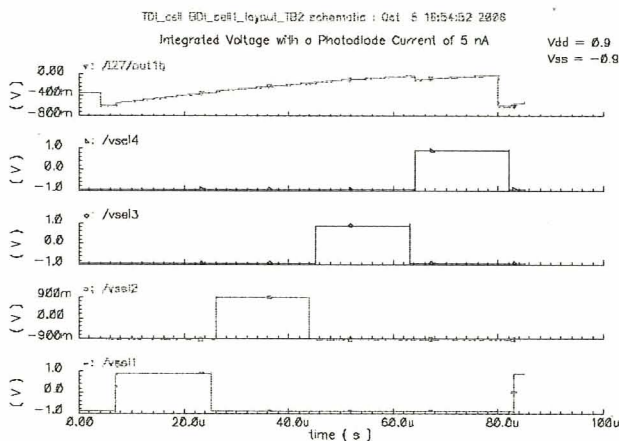


Figure 4. Integrated Voltage of one cell over four clock periods.

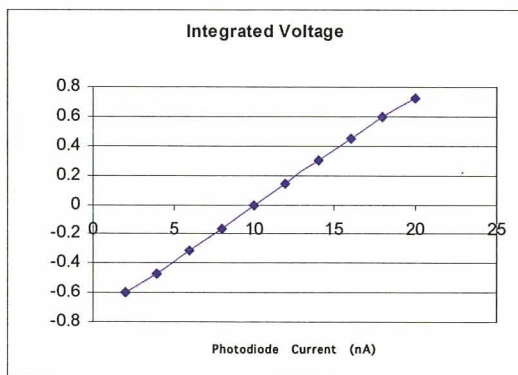


Figure 5. Integrated Voltage as a function of Photodiode current.

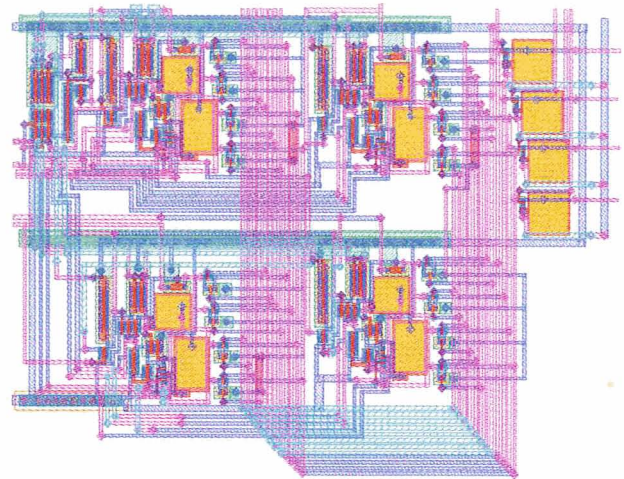


Figure 6. Layout of BDI implementation.

### IV. CONCLUSIONS

The focus of the project is on developing low voltage, compact and high performance circuits for the BDI approach. Some innovative features were proposed: utilization of a new a very high gain amplifier with high GB, current memory cells that are less sensitive to charge injection errors, and compact class AB line buffers with high slew rate and very low static power dissipation. The simulations performed show a very good linear relationship between the photodiode current and the integrated voltage. This circuit was done with low power requirements (1.8V supply and  $1\mu\text{A}$  bias current). The circuit is currently under fabrication with the  $0.5\mu\text{m}$  CMOS (AMI-MOSIS) technology.

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