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Ferroelectric Material Application: Modeling Ferroelectric Field Effect Transistor Characteristics from Micro to Nano

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Abstract - All present ferroelectric transistors have been made on the micrometer scale. Existing models of these devices do not take into account effects of nanoscale ferroelectric transistors. Understanding the characteristics of these nanoscale devices is important in developing a strategy for building and using future devices. This paper takes an existing microscale ferroelectric field effect transistor (FFET) model and adds effects that become important at a nanoscale level, including electron velocity saturation and direct tunneling. The new model analyzed FFETs ranging in length from 40,000 nanometers to 4 nanometers and ferroelectric thickness from 200 nanometers to 1 nanometer. The results show that FFETs can operate on the nanoscale but have some undesirable characteristics at very small dimensions.

I. INTRODUCTION

The purpose of this paper is to develop a model that can accurately predict the characteristics of ferroelectric field effect transistors (FFET) for a range of sizes of channel lengths from tens of microns to a few nanometers. Models exist [1] that can accurately characterize FFETs in the micron scale size. These can be verified to be accurate by comparison with data from actual FFETs. Recent research [2] [3] has developed equations and models of very small transistors (non-ferroelectric). This paper takes an existing FFET model and incorporates effects from having a very short channel length and very thin ferroelectric films over the channel. The model simulates only classical FET layout design of a transistor and does not attempt to simulate single molecule or vortex layouts. The basis for the empirical data is a PZT FFET [4] with a channel length of approximately 40 microns. The model was run for channel lengths of 40,000 nm, 4000 nm, 400 nm, 40 nm, and 4 nm. To reduce complexity all W/L ratios were 1. The ferroelectric film thicknesses ranged from 200 nm to 3 nm. For thicknesses of less than 3 nm, the model did not produce good results. This may be due to instability in the model or actual physical problems due to the short distances and high electric

fields. Ferroelectric films of less than 2 nm would be difficult to produce and the perovoskite crystal structure has physical size limitation in this range.

II. Basis of the Model

A. *Partitioned Ferroelectric Model*

The major difference between the Ferroelectric Field Effect Transistor and the normal MOSFET is the replacement of the oxide layer with a ferroelectric layer above the channel of the transistor. This layer develops charge much differently than the oxide layer due to polarization of the material. These charges affect the surface potential within the channel and change the threshold voltage of the transistor. Several researchers have studied these effects and have developed models of how they work. Wu [5] developed a mathematical model that accounts for the additional charges from the ferroelectric material at the semiconductor-ferroelectric interface. Since the threshold voltage for a MOSFET is a function of the total charge at the semiconductor-insulator interface, the threshold voltage is:

$$V_T = 2\phi_F + \phi_{FS} - \frac{Q_{SS}}{C_D} \pm \frac{P_S \cdot A_F}{C_F} + \frac{\sqrt{4q\varepsilon N_A \phi_F}}{C_D} \qquad (1)$$

Where P_S is the ferroelectric polarization, A_F is the ferroelectric material area, and C_D is the insulator capacitance (or ferroelectric capacitance, C_F). This new C_D is calculated using the following equation.

$$C_D = \frac{C_{ox} C_F}{C_{ox} + C_F} \qquad (2)$$

Where, C_{ox} is the capacitance of the oxide layer.
When there is only a ferroelectric insulator and no oxide, $C_D = C_F$.

Chen [6] developed a MFSFET model that included the field effect parameter A. This model was only derived for a saturated hysteresis curve. These models are helpful in understanding the theoretical process for the operation of an FFET but do not produce data that is consistent with real world FFETs actual measurements. To improve on this Bailey and Ho [1] developed a model that partitions the ferroelectric layer into segments. The motivation for breaking the ferroelectric layer into segments comes from the fact that each section of the layer is under different conditions. For example, if the gate-source voltage is greater the flatband voltage and the drain-source voltage is greater than zero, the gate to channel voltage would be constant for the entire length of the channel but the semiconductor surface potential would very from Ψ_{S0} at the source to Ψ_{SL} at the drain. This causes the electric field applied to the ferroelectric material to vary from $V_{GS} - \frac{\Psi_{S0}}{d_F}$ (3) at the source to $V_{GS} - \frac{\Psi_{SL}}{d_F}$ (4) at the drain, where d_F is the ferroelectric thickness. This shows that each segment of the ferroelectric material sees a different electric field. This indicates that the polarization for each segment of the ferroelectric material varies with position. Complicating the model is the fact that the

polarization depends not only on the present conditions but also on past conditions. This approach was presented by Tsividis [4] with respect to ferroelectric polarization.
The standard Threshold voltage equation must be modified to account for the charges due to polarization of the ferroelectric material. It is given by

$$V_T = V_{FB} + \phi_B + \gamma\sqrt{\phi_B + V_{SB}} - \frac{Q'_F}{C'_F} \qquad (5)$$

Where V_T is the transistor threshold voltage, V_{FB} is the flatband voltage, $\Phi_B = 2\Phi_F + 6\,\Phi_t$, where Φ_B is the voltage drop across the depletion region, Φ_F is the Fermi voltage and Φ_t is the thermal voltage, γ is the Body effect coefficient, V_{SB} is the source to body voltage, Q'_F is the ferroelectric polarization per unit area, and C'_F is the ferroelectric capacitance per unit area. The difficult part of this equation is determining the overall ferroelectric polarization of the ferroelectric material. The model used in this paper divides the length of the channel up in to partitions and calculates the polarization numerically given the previous polarization, material characteristics, and the voltages present at the transistor terminals.
Figure 1 shows the layout of the model under operating conditions. The ferroelectric material is divided into segments. For this paper, the number of segments used was 100. Increasing the number of partitions did not significantly change the model's output.

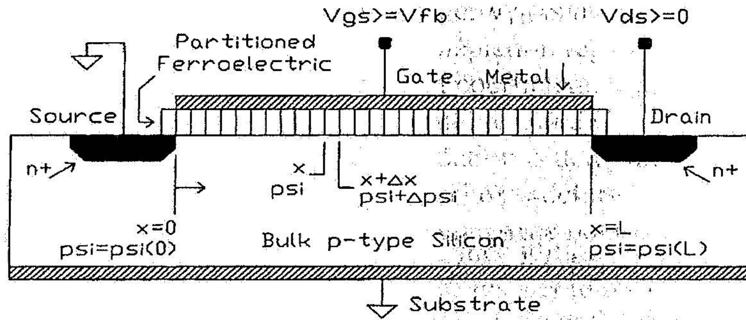

Fig. 1. Partitioned MFSFET under operation conditions.

To obtain the FFET threshold voltage the total amount of charge at the channel interface must be determined. This is determined by finding the polarization for each segment using

$$E_i = \frac{V_{GS} - \left(\frac{\Psi_i + \Psi_{i+1}}{2}\right)}{d_F} \qquad (6)$$

then summing all of the partitions. The key parameter to solve this equation is the surface potential at each partition. The relationship between the channel position and the surface potential is given by

$$\frac{x}{L} = \frac{f[\Psi_S(x)] - f(\Psi_{S0})}{f(\Psi_{SL}) - f(\Psi_{S0})} \qquad (7)$$

Where x is the channel position, L is the length of the channel and f is a function given by

$$f(\Psi_S) = \mu C'_F\left[(V_{GS} - V_{FB} + \phi_t)\Psi_S - \tfrac{1}{2}\Psi_S^2 - \tfrac{2}{3}\gamma\Psi_S^{\frac{3}{2}} + \phi_t\Psi_S^{\frac{1}{2}}\right] \qquad (8)$$

Since $f(\Psi_S)$ is nonlinear in Ψ_S, the solution is obtained by a numerical root solving method of the following equation

$$0=V_{GS}-V_{FB}-\Psi_S+\zeta\gamma\sqrt{\phi_t e^{\frac{-\Psi_S}{\phi_t}}+\Psi_S-\phi_t+e^{\frac{-2\phi_F}{\phi_t}}\left(\phi_t e^{\frac{(\Psi_S-V_{CB})}{\phi_t}}-\Psi_S-\phi_t e^{\frac{-V_{CB}}{\phi_t}}\right)} \quad (9)$$

Once the threshold voltage is determined for the particular FFET conditions the drain current is calculated by

$$V'_{DS} = \frac{V_{GS} - V_T}{1 + \delta} \quad (10)$$

For $V_{DS} \le V'_{DS}$

$$I_{DS} = k\frac{W}{L}\mu C'_F\left[(V_{GS} - V_T)\cdot V_{DS} - \frac{1}{2}(1 + \delta)\cdot V_{DS}^2\right] \quad (11)$$

For $V_{DS} > V'_{DS}$

$$I_{DS} = k\frac{W}{L}\mu C'_F\frac{(V_{GS} - V_T)}{2(1 + \delta)} \quad (12)$$

Where,
V'_{DS} is the modified drain to source voltage, V_{GS} is the gate to source voltage, V_T is the transistor threshold voltage, k is an empirical scaling constant, and μ is the electron mobility.

B. *Velocity Saturation Model*

The effect of velocity saturation has a very significant affect when the dimension of the transistor becomes small. Both the channel length and the oxide thickness have an effect. The model uses equations developed by Hodges [2]. The first effect is that of varying the effective electron mobility. For high electric fields across the channel oxide a large number of carriers are induced in the inversion layer changing the effective mobility. The equation for the effective mobility is given by

$$\mu_e = \frac{\mu_0}{1 + \left(\frac{V_{GS} - V_T}{\Theta \bullet t_{ox}}\right)^{\eta}} \quad (13)$$

Where
Θ and η are empirical values (3.6×10^6 and 1.85 where used).

The drain current for the linear region is given by

$$I_{DS} = \frac{W}{L}\frac{\mu_e C_{ox}}{\left(1+\frac{V_{DS}}{E_c L}\right)}\left(V_{GS} - V_T - \frac{V_{DS}}{2}\right)\cdot V_{DS} \quad (14)$$

Where
E_c is the electric field across the channel and L is the channel length.

The drain current for the saturation region is given by

$$I_{DS} = W v_{sat} C_{ox} \frac{(V_{GS} - V_T)^2}{(V_{GS} - V_T) + E_c L} \qquad (15)$$

Where
V_{sat} is the saturation velocity.

Another effect that becomes important when transistor dimensions become very small is the direct tunneling as described by Wong [3]. When the oxide becomes very thin then the reduced barrier and increase electric field cause an increase in electrons directly tunneling from the gate to the channel. This reduces the desirable characteristics of the transistor. The tunneling current density is given by

$$J = \frac{q^3}{8\pi h \phi_b \varepsilon_{ox}} C \cdot \exp\left\{ -\frac{8\pi\sqrt{2 m_{ox} \phi_b^3}}{3hq|E_{ox}|} \left[1 - \left(1 - \frac{V_{ox} q}{\phi_b} \right)^{3/2} \right] \right\} \qquad (16)$$

Where,

$$C = \exp\left[\frac{20}{\phi_b} \left(\frac{|V_{ox}| - \phi_b}{\phi_{b0}} + 1 \right)^{\alpha} \left(1 - \frac{|V_{ox}|}{\phi_b} \right) \right] \frac{V_g}{t_{ox}} N \qquad (17)$$

$$N = \frac{\varepsilon_{ox}}{t_{ox}} \left\{ S \ln\left[1 + \exp\left(\frac{V_{ge} - V_T}{S} \right) \right] + v_t \ln\left[1 + \exp\left(\frac{V_{fb} - V_g}{v_t} \right) \right] \right\} \qquad (18)$$

Where S is the sub-threshold swing, v_t is the thermal voltage, V_T is the threshold voltage, φ_b and φ_{b0} are 3.1, m_{ox} is 0.4, and α is 0.6. These parameters are for SiO_2 and not for PZT. It is assume the PZT parameters would be similar enough to produce similar results.

IV. Results

A. *Verification of model with measured data*

The first result that must be verified is that the new model accurately characterizes an actual measured FFET. Measurements from a PZT FFET were compared to the model's predictions. The FFET had a channel length approximately 40 microns long and a ferroelectric thickness of about 200 nanometers. The operating gate voltage was +/- 8 volts. These parameters were input into the model and the resulting output was generated in figure 2 for the active mode (Gate voltage ON).

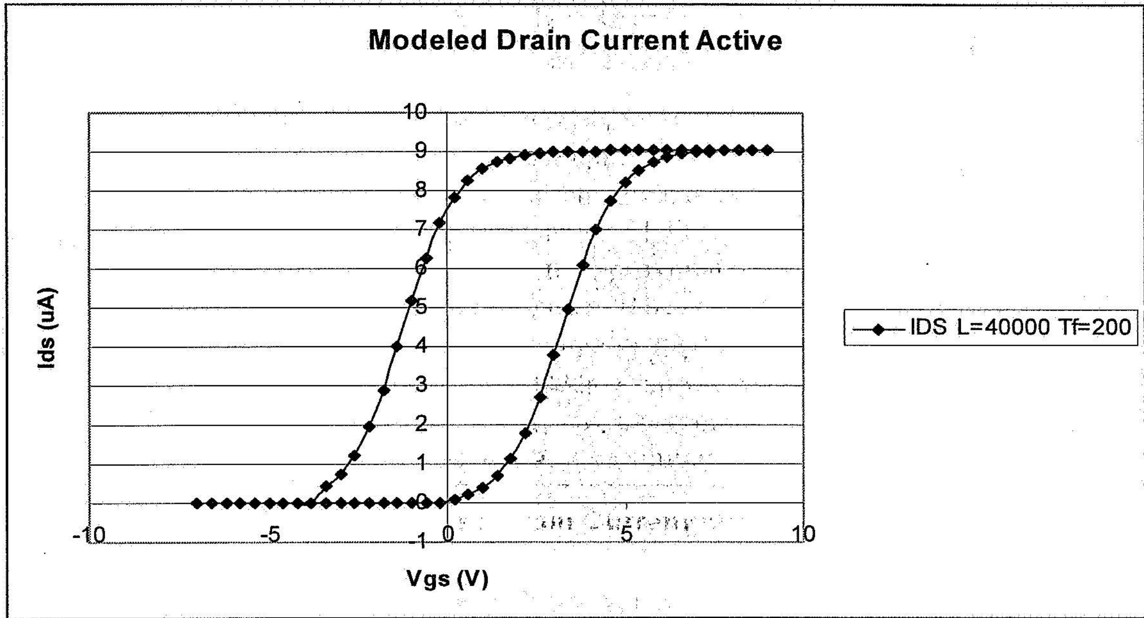

Fig 2. Model results for drain current for an FFET in Active mode with L=40,000 nm and Tf=200 nm.

This prediction compares quite well to the measured data from the FFET in figure 3.

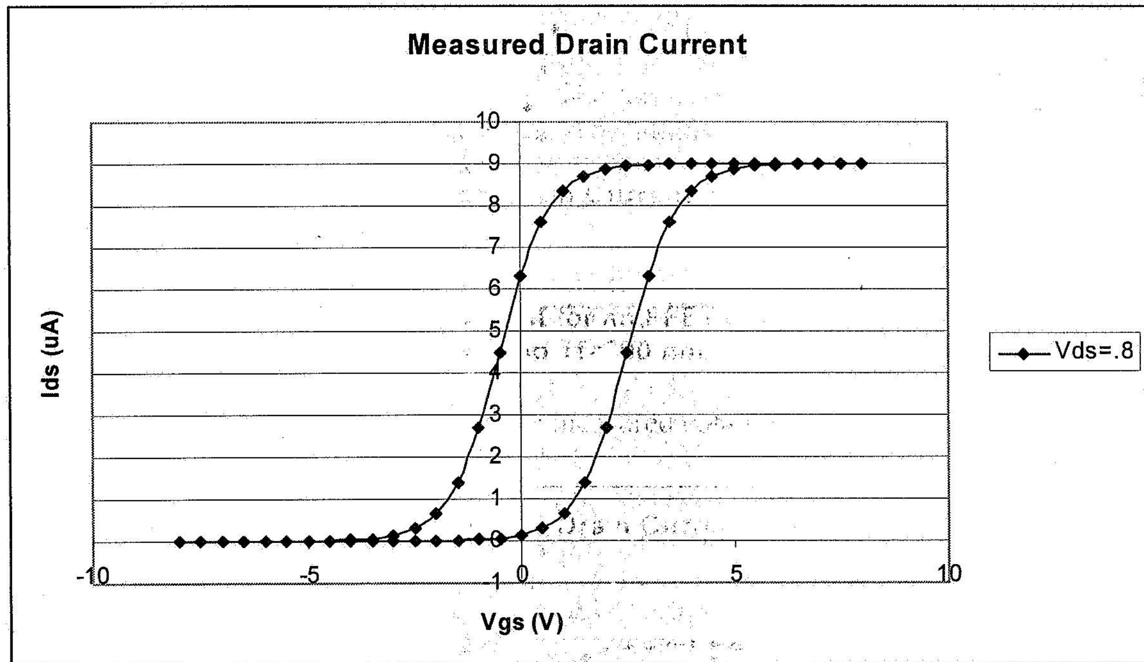

Fig. 3. Measured Drain current of actual FFET in Active mode with l~40,000 nm and Tf~200 nm.

The model also generates data for the remnant mode (Gate voltage OFF after applying the gate voltage shown on the X axis). This data is shown in figure 4.

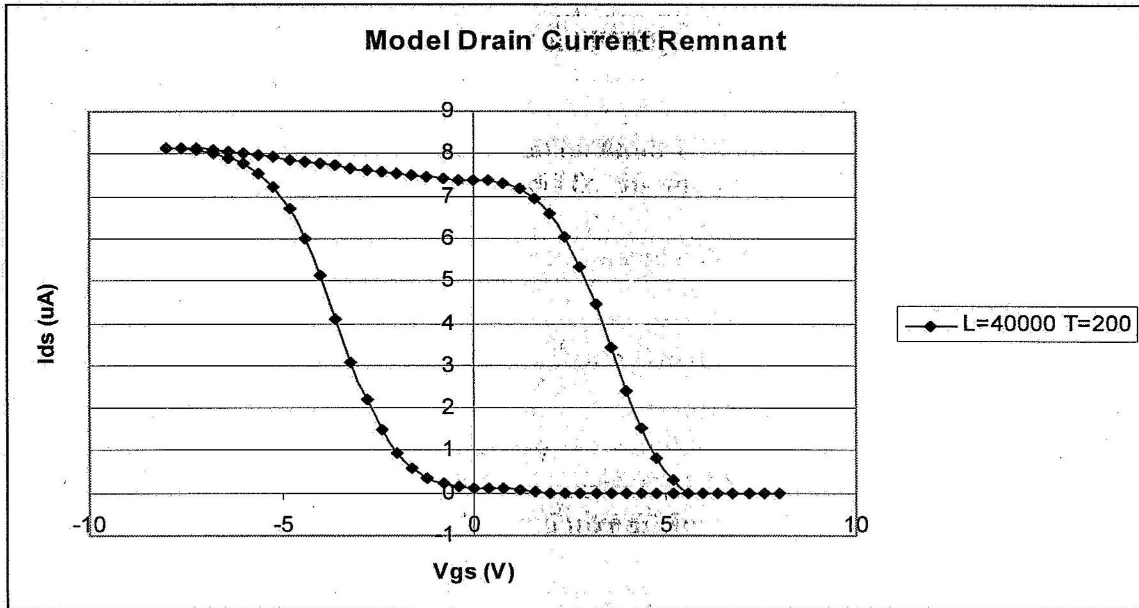

Fig. 4. Model results for drain current for an FFET in Remnant mode with L=40,000 nm and Tf=200 nm.

This again compares favorably to the measured data in figure 5. The remnant measured data is affected by the decay of the polarization of the ferroelectric material during the time it took to make the measurements. The model does not have any decay time modeled between gate pulses. This is why the upper portion of the measured data seems to be lower that the model predicts.

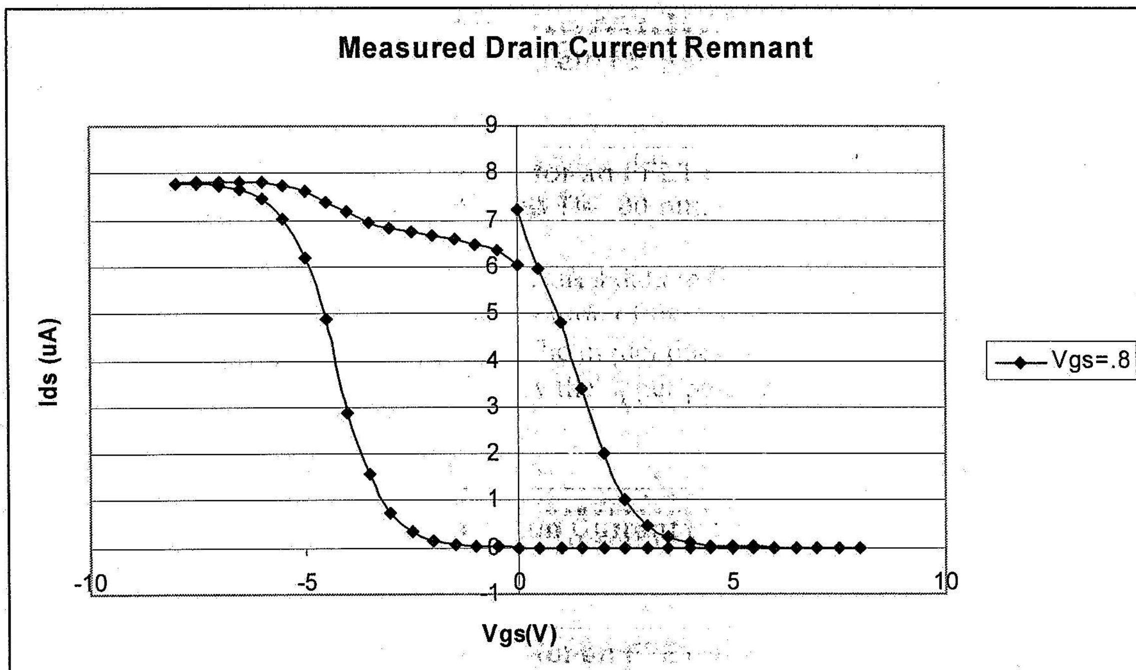

Fig. 5 Measured Drain current of actual FFET in Remnant mode with l~40,000 nm and Tf~200 nm.

B. *Combined Model Results*

The model was run in both the active and remnant modes for several combinations of channel length and ferroelectric film thicknesses. The simulation starts at 40,000 nanometer channel length because that is the length of the measured FFET. Each subsequent simulation has the 1/10th the previous channel length. Channel lengths of less than 4 nanometers produced no current in the model. Similarly the ferroelectric film thickness varied between 200 nanometers and 3 nanometers. At thicknesses less than 3 nanometers, the model became unstable and produced unreliable results. Figure 6 shows the active mode drain current predicted by the model for a variety of combinations channel length and film thicknesses.

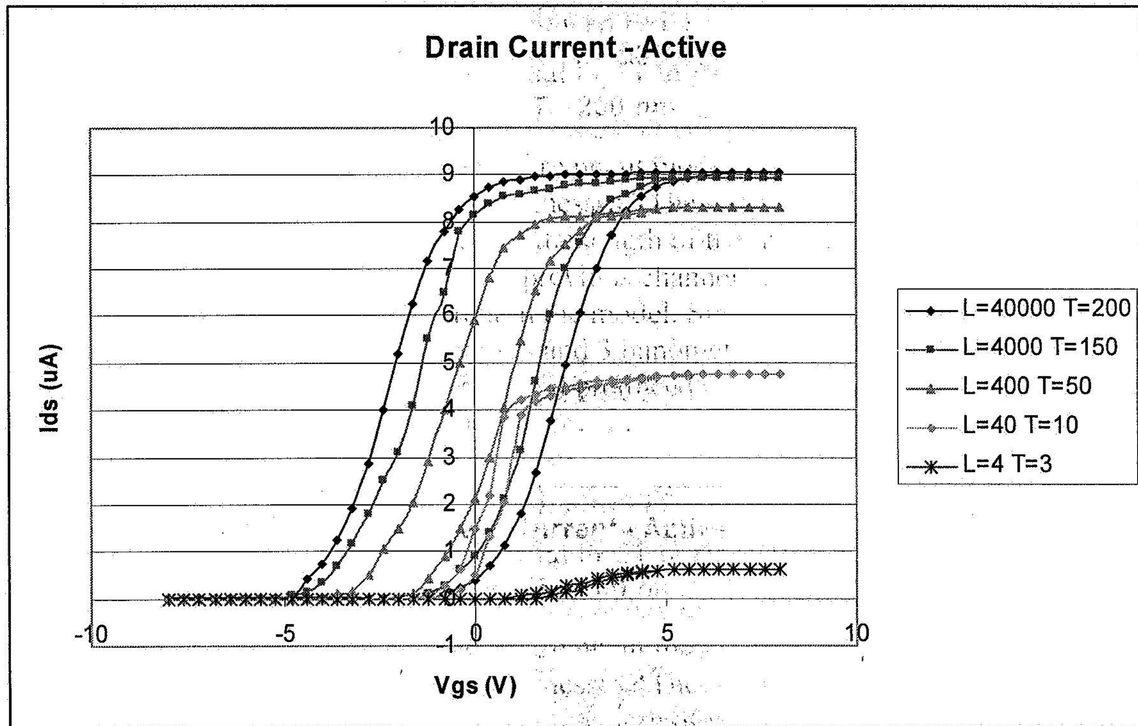

Fig. 6. Simulated drain current for Active mode (Gate voltage = +/- 8V).

Similarly, figure 7 shows the remnant mode drain currents predicted by the model for the same combinations.

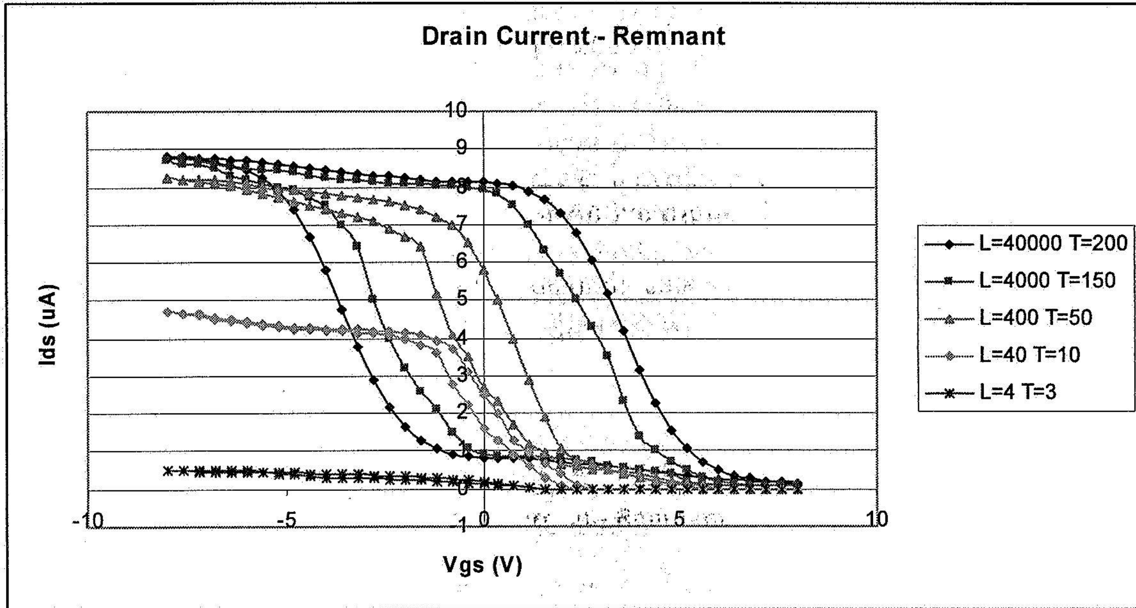

Fig. 7. Simulated drain current for Remnant mode (Gate voltage = +/- 8V).

Because the empirical data was taken from a large PZT FFET the model uses gate voltages of +/- 8 volts. For future nanoscale transistor different materials and lower voltages will be appropriate. Therefore, the simulation was also run with gate voltages of +/- 3 volts. Because the PZT does not fully polarize at these voltages, the shapes of the drain current versus gate voltage plots have a different shape. These results are shown in figures 8 and 9.

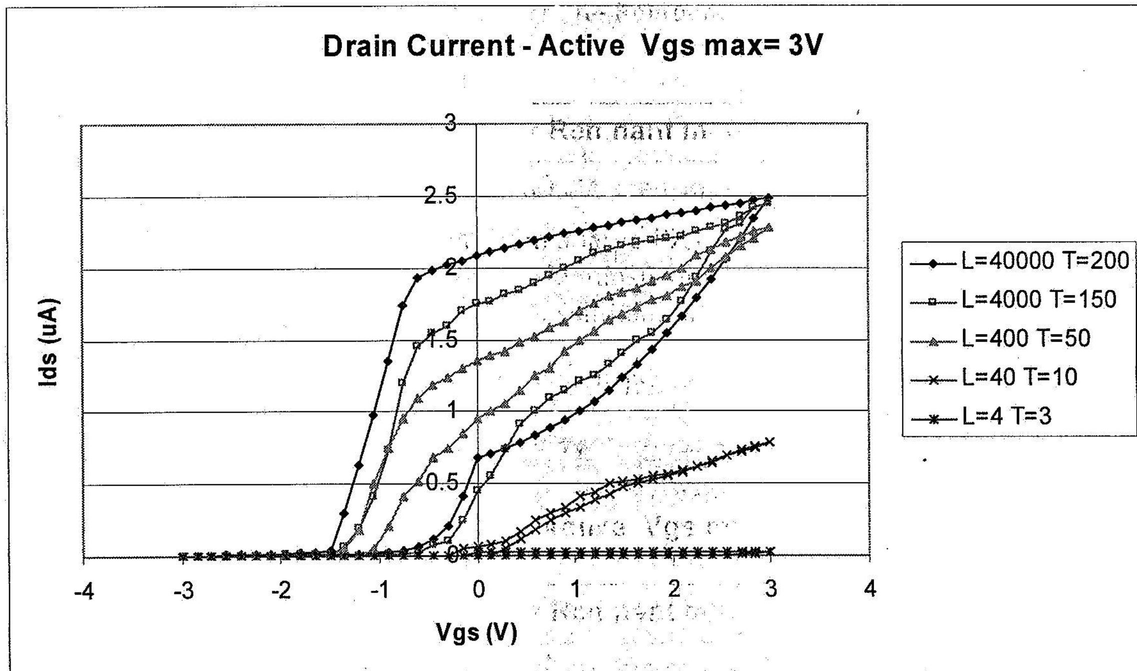

Fig. 8. Simulated drain current for Active mode (Gate voltage = +/- 3V).

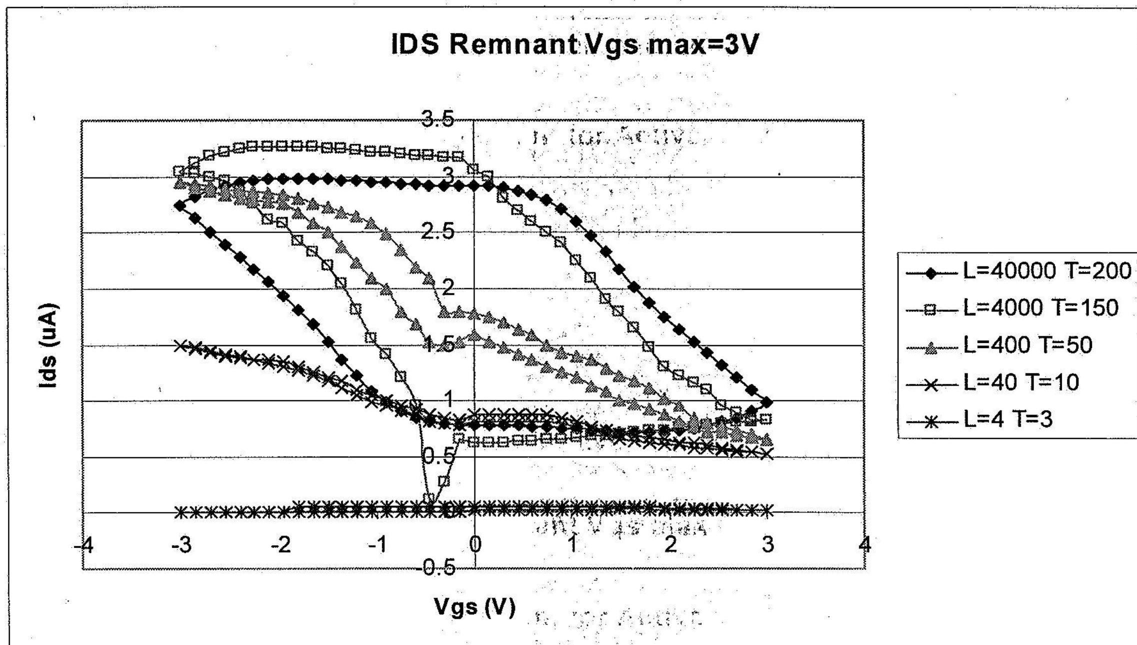

Fig. 9. Simulated drain current for Remnant mode (Gate voltage = +/- 3V).

C. *Direct Tunneling Current*

When the ferroelectric thickness gets very small the lower barrier and the high electric fields cause the direct tunneling current to rise to a level that could interfere with the normal operation of the transistor.

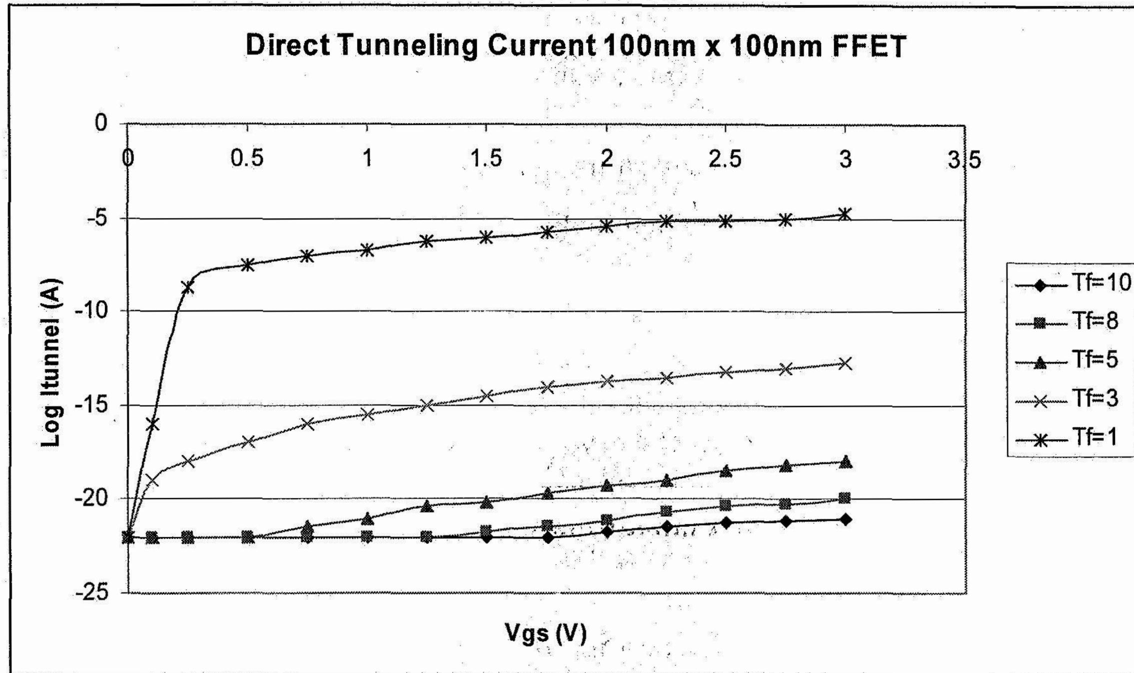

Fig. 10. **Direct tunneling predicted for a 100nm x 100nm FFET**

V. CONCLUSION

Model simulation suggests that very small ferroelectric transistors are possible. At some point the transistors become inoperable due to gate current tunneling into the channel and drain current reduction due to reduction in charge of the ferroelectric film, velocity saturation and carrier mobility reduction. The point at which these effects become overwhelming is about 4 nanometer channel length and 3 nanometer ferroelectric film thicknesses. These two parameters are independent but the model becomes unstable if either parameter goes below these thresholds. The authors of this paper tried to include all major effects on nano-ferroelectric transistors, but because no characterizations of actual nano-ferroelectric transistors have been made, there may be other effects that render the transistor inoperable that are not modeled in this simulation. Future simulations need to take more effects into consideration to produce more accurate results.

VI. REFERENCES

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