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Static and Turn-on Switching Characteristics of 4H-Silicon Carbide SITs to 200 °C

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Test results are presented for normally-off 4H-SiC Static Induction Transistors (SITs) intended for power switching and are among the first normally-off such devices realized in SiC. At zero gate bias, the gate p-n junction depletion layers extend far enough into the conduction channel to cut off the channel. Application of forward gate bias narrows the depletion regions, opening up the channel to conduction by majority carriers. In the present devices, narrow vertical channels get pinched by depletion regions from opposite sides. Since the material is SiC, the devices are usable at temperatures above 150 °C. Static curve and pulse mode switching observations were done at selected temperatures up to 200 °C on a device with average static characteristics from a batch of similar devices. Gate and drain currents were limited to about 400 mA and 3.5 A, respectively. The drain voltage was limited to roughly 300 V, which is conservative for this 600 V rated device. At 23 °C, 1 kW, or even more, could be pulse mode switched in 65 ns (10% to 90%) into a 100 Ω load. But at 200 °C, the switching capability is greatly reduced in large part by the excessive gate current required. Severe collapse of the saturated drain-to-source current was observed at 200 °C. The relation of this property to channel mobility is reviewed.

I. Introduction

The Static Induction Transistors (SITs), also referred to as vertical, short-channel, junction field-effect transistors (VJFETs), tested here are among the first normally-off such power devices realized in 4H-SiC. SITs commercially produced years ago in Si have all been normally-on devices, with characteristics resembling those of a triode vacuum tube and have accordingly found application as amplifiers in transmitters. The present SiC prototypes are more suitable for power switching, due to their normally-off property. This is achieved by having a built-in p-n junction depletion layer at zero bias extend far enough into the conduction channel to choke off current flow in the channel. As forward (positive) bias is applied to this gating p^+-n junction, the depletion regions narrow, opening up the n-doped channel to conduction by majority carriers. Hence the present SiC SITs can be viewed as gate voltage controlled, but with the flow of sometimes significant forward bias gate junction current. In the tested devices, depletion regions from opposite sides pinch narrow vertical channels. Since the material is SiC and there is no gate oxide layer, the devices exhibit favorable stability and are usable at temperatures above 150 °C. Moreover, recent efforts[1–4] have produced higher voltage, trenched and implanted devices that are easier to fabricate.

Static I-V curve and pulse mode switching observations were done at several temperatures up to 200 °C on two average performing devices, selected on the basis of static characteristics from 7 similar devices developed by United Silicon Carbide, Inc. on NASA SBIR contract NAS3-03036. These two devices were quite alike and hence only one (labeled "N-4") is presented here. Gate and drain currents were limited to about 400 mA and 3.5 A, respectively. The drain voltage was limited to roughly 300 V, which is conservative for this 600 V, 3 A rated device.

At 23 °C, 1 kW, or even more, could be switched in 65 ns (10 to 90%) into a 100 Ω load. But at 200 °C, serious problems arose due to collapsing gate-to-drain transconductance.

II. Static Drain-to-Source Curves

Static I_D-V_{DS} curves for the N-4 SIT at selected temperatures to 200 °C are presented in Figure 1. These curves were captured by a Tektronix model 370B programmable curve tracer, using a 0.5 V gate step (pulsed) up to 10 steps. The magnitude of the gate current is also indicated for the highest step as only a rough value, since this current depends somewhat on the V_{DS}. The corresponding gate current was estimated by comparison to a set of I_D-V_{DS} curves taken in the pulsed gate current step mode.

Figure 1 carries the manifest message that this particular SIT is not suitable for high temperature (~200 °C) operation as a power switch, unless its current rating is greatly reduced from the room temperature value. The killer property is the monotonically collapsing saturated drain-to-source current (I_{DSS}) with increasing temperature, for a given gate-to-source voltage. And there is obviously a limit to the allowable gate current, which increases with both gate voltage and temperature, according to the physics of a forward biased p-n junction. A fixed level of gate drive rapidly becomes inadequate to achieve saturated switching with rising temperature, resulting in an increasing voltage drop across the SIT and eventually thermal runaway.

According to abrupt junction, long-channel JFET[5] physics, the transconductance and I_{DSS} are proportional to the number of ionized donors and carrier mobility in the n-doped channel. Due to the relatively deep (compared to silicon) donor dopant ionization energy, dopant ionization in SiC may be only 60% at 20 °C, depending on particulars, but it increases with temperature. Electron mobility in SiC is usually taken to vary as approximately inverse square of the temperature. Various workers[6, 7] have observed the collapse of I_{DSS} in certain SiC-based JFETs with increasing temperature at least as early as 1992. They have attributed this collapse to the overriding effect of reduced carrier mobility. This long-channel model seems to predict qualitatively the behavior observed for these devices.

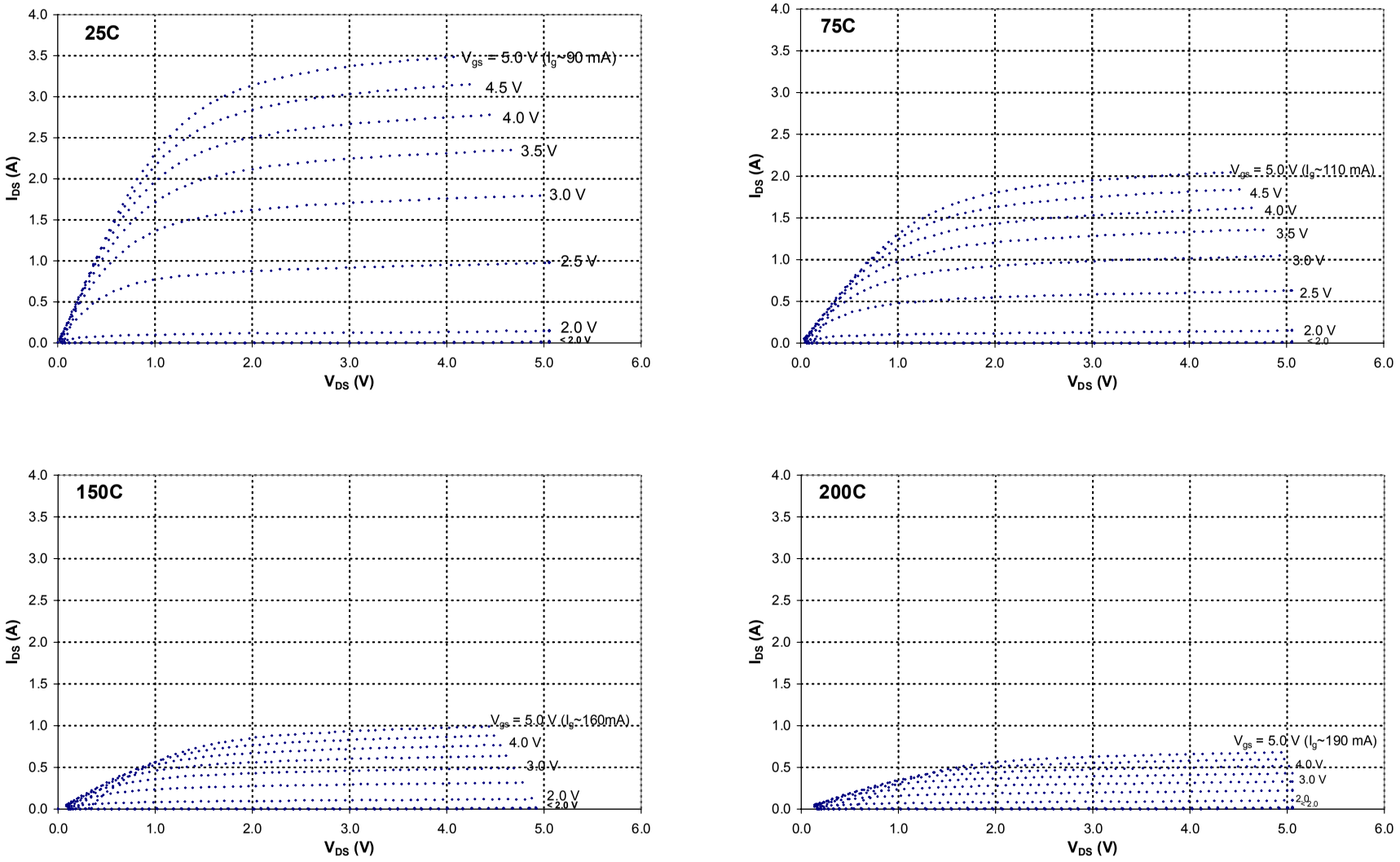

Figure 1.—Drain-to-source characteristics of the 4H-Silicon Carbide SIT "N-4" at the indicated selected temperatures to 200 °C. The gate current I_G indicated for the gate voltage V_{GS} = 5.0 V is only a rough value, as it also depends on the drain-to-source voltage V_{DS}. Although not shown above, the device successfully blocked current at V_{GS} = 0 for all drain biases to V_{DS} = 300 V at these temperatures.

III. Turn-On Testing Circuits

A constant voltage source V_0 feeding a resistive load R_D in the drain circuit was chosen to make up the power side of the circuit. A nearby charged capacitor served well to decouple from the actual V_0 supply, since operation was with sub-microsecond pulses at no more than 0.1% duty cycle. The SIT itself was mounted to a temperature-controlled plate, with a thermocouple attached directly to the SIT. Various modes of gate drive, such as constant current and constant voltage steps, were then applied. A general circuit diagram is provided in Figure 2.

Although the gate drive was implemented in both constant voltage and constant current modes, data was taken primarily using the constant current drive, shown in Figure 3. A constant voltage drive was investigated, but was avoided for two reasons. First, the constant voltage drive mode would produce an overly large inrush current spike into the gate capacitance, especially when setting the steady-state gate current above 300 mA. Second, it was more difficult to accurately set the steady-state gate current using this drive, as the gate current is exponentially sensitive to the gate voltage and also the device temperature. The gate damage danger limits of such inrush spikes are unknown for the present devices, but in some future applications a higher inrush current may help to decrease the drain current rise-time.

The drive circuit in Figure 3 is of course "constant current" only to the extent that its output impedance is much higher than the impedance of the SIT's gate. Due to the spurious impedances involving the SIT and connections, such a description becomes inaccurate on time scales below say 10 ns. Also, the effective gate impedance of the SIT is highly variable, due to capacitive and possibly other feedback from the drain circuit. A commercially available, high voltage (850 V into 50 Ω), fast rise (~6 ns) DEI model HV1000 pulser was adapted as the gate driver. In this way, very fast gate signal rise-times could be achieved. Indeed, the load current (I_D) rise-time was usually much longer than the gate-drive rise-time.

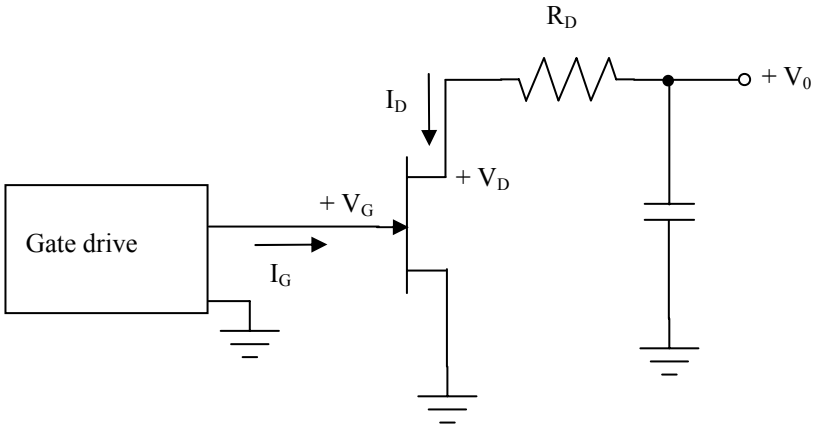

Figure 2.—Basic resistive load turn-on switching test circuit. Currents I_G and I_D are sensed by high-speed current transformers (Tektronix CT1 and CT2). Potential V_G is sensed by a 1 kΩ input impedance, fast-rise probe and potential V_D by a Tektronix 10X probe. R_D is a carbon composition resistor (e.g., the 100 and 300 Ω values in Table I).

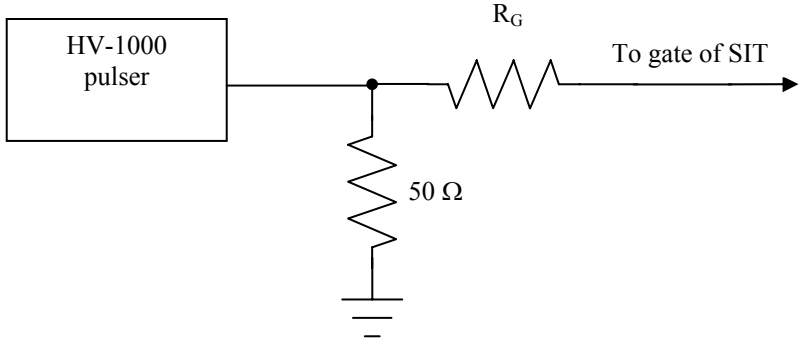

Figure 3.—Constant current gate drive circuit. R_G values of 300 Ω to 1 kΩ were used.

IV. High Temperature Switching Data Overview

The data presented in Table 1 is a subset of all data taken, showing the amount of gate drive needed to achieve acceptable switching at selected temperatures and load currents. The values of currents indicated are their steady state values, using a constant current gate drive. The gate drive difficulties and load current limitations as the temperature increases become apparent from this table. The Table 1 data is taken from dynamic scope traces, such as reproduced in Figure 4.

The switching dynamics in Figure 4 shows that at 200 °C and with a 100 Ω load, a 1 A drain current rises in less than 100 ns when switched by a 400 mA gate current step. The gate voltage and current rise within 10 ns, seemingly independent of the much slower rise of the drain current. For the "400 mA, 100 Ω, 1 A" condition, Table 1 shows a steady increase of the turn-on time with increasing temperature. Switching times are seen to roughly triple when going from 23 to 200 °C. Thus the switching time goes from 25 ns at 23 °C to 71 ns at 200 °C when switching 1 A into a 100 Ω load (400 mA gate drive).

The rise of the on-state V_{DS} with temperature for a given gate drive level is a more serious problem. Table 1 shows that at room temperature, just 100 mA of gate drive is sufficient to adequately switch at least 2 A, but drain current risetimes (10 to 90%) substantially less than 100 ns require at least 300 mA of gate drive current. At 150 °C, 1 A of load current seems to present no problems, but with 1.5 A of load current, a voltage drop of some 6 V (V_{DS} resolution in the table is no better than about 2 V) appears across the device, even with 400 mA of gate drive. At 2 A of load current, a 26 V drop appears across the device, even with 400 mA of gate drive and thus the switching is poor. This situation gets worse as the temperature increases, until at 200 °C it is not possible to acceptably switch load currents above 1 A, with the gate being limited to 400 mA. Basically, this behavior is predicted by the static characteristic curves for this SIT in Figure 1.

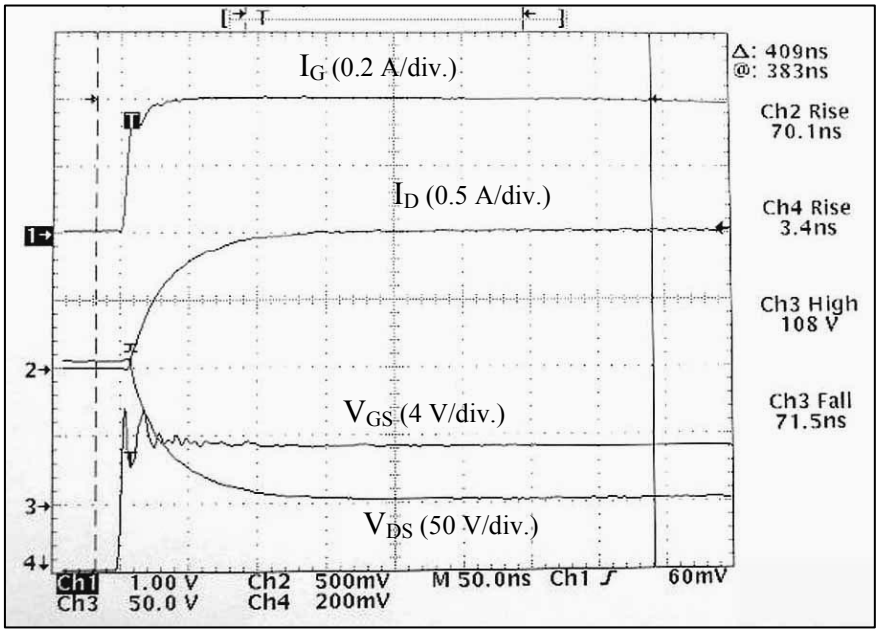

Figure 4.—Turn-on dynamics of the N-4 SIT at 200 °C, with a 400 mA gate current step and a 100 Ω load resistor.

Table 1.—Observed Switching Transition Times

Data at 23 °C:

I_G (mA)	R_D (Ω)	I_D (A)	V_{DS} (V)	V_0 (V)	τ_{ID} (ns)
400	100	3.5	2	352	73
300	"	"	0	350	93
200	"	"	2	352	127
100	"	"	6	356	209
400	"	2.0	0	200	42
300	"	"	0	200	56
200	"	"	0	200	79
100	"	"	0	200	133
400	"	1.0	0	100	25
300	"	"	0	100	31
200	"	"	0	100	43
100	"	"	0	100	83

Data at 150 °C:

I_G (mA)	R_D (Ω)	I_D (A)	V_{DS} (V)	V_0 (V)	τ_{ID} (ns)
400	100	2.0	26	226	98
300	"	"	44	244	108
400	"	1.5	6	156	78
300	"	"	6	156	100
400	"	1.0	4	104	47
300	"	"	3	103	63
300	300	"	2	302	92
200	"	"	2	302	127
100	"	"	-2	298	204

Data at 175 °C:

I_G (mA)	R_D (Ω)	I_D (A)	V_{DS} (V)	V_0 (V)	τ_{ID} (ns)
400	300	1.5	10	460	123
400	100	"	16	166	90
300	"	"	32	182	105
400	"	1.0	5	105	58
300	"	"	5	105	81
"	300	"	2	302	112
200	"	"	6	306	147
100	"	"	16	316	212

Data at 200 °C:

I_G (mA)	R_D (Ω)	I_D (A)	V_{DS} (V)	V_0 (V)	τ_{ID} (ns)
400	300	1.5	38	488	128
400	300	1.0	6	306	97
300	"	"	6	306	120
200	"	"	18	318	156
400	100	1.5	51	201	87
300	"	"	77	227	95
400	"	1.0	8	108	71
300	"	"	8	108	91

Notes: τ_{ID}: 10 to 90% time, I_G: steady state gate current, R_D: load resistor, I_D: drain current, V_0: supply voltage, V_{DS}: drain-to- source voltage. The V_{DS} resolution is no better than 2 V.

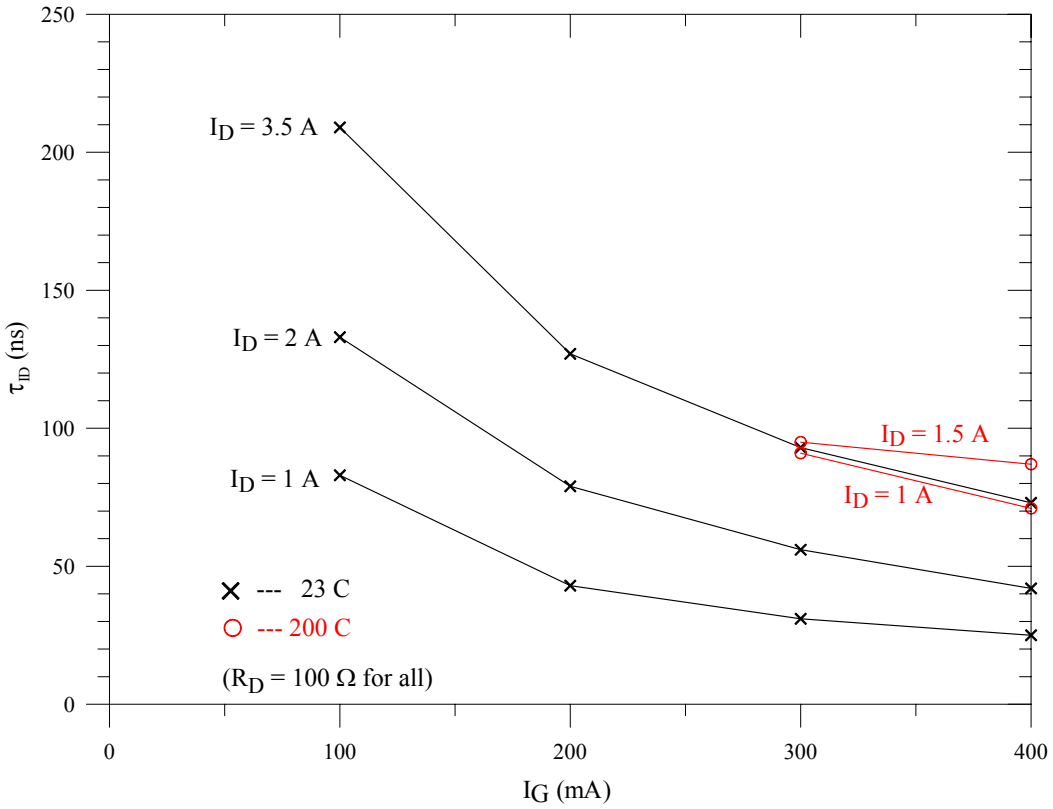

Figure 5.—Risetime of the drain current versus gate drive current for selected values of the drain current in the steady state. Data are taken at 23 and 200 °C from Table 1. V_{DS} is large at the 200 °C, I_D = 1.5 A data points (see Table 1).

The switching time clearly depends on the steady state gate and drain currents, as well as the temperature. Some aspects of this are illustrated in Figure 5, based on Table 1. The 23 °C curves show good switching, as the V_{DS} remains low over the indicated range of gate current I_G. The two 200 °C points for I_D = 1 A represent marginally acceptable switching, as the V_{DS} is somewhat high at 8 V, out of the 108 V supply. Hence these points seem to represent switching slowdown due just to increased temperature, as compared to switching the 1 A at 23 °C, where $V_{DS} \approx 0$ V. The two 200 °C, I_D = 1.5 A points do not admit to such a simple interpretation, because the V_{DS} remains very high (77 V at I_G = 300 mA and 51 V at I_G = 400 mA) compared to the supply voltage (227 V and 201 V) and the device is not fully turning on.

As expected, higher load resistances do slow down the switching, although not proportionally. And larger currents take longer to switch. Thus there seem to be various contributions, assuming that the switching time constant is basically of the RC type. An example of such variation of switching speed for two different load resistances, I_G = 200 mA and a test temperature of 23 °C is shown in Figure 6. From Figure 6, it can be seen that (1) the 50 Ω load always gives lower turn-on times than the 100 Ω load for a given drain current and (2) the switching turn-on time increases almost linearly with the drain current.

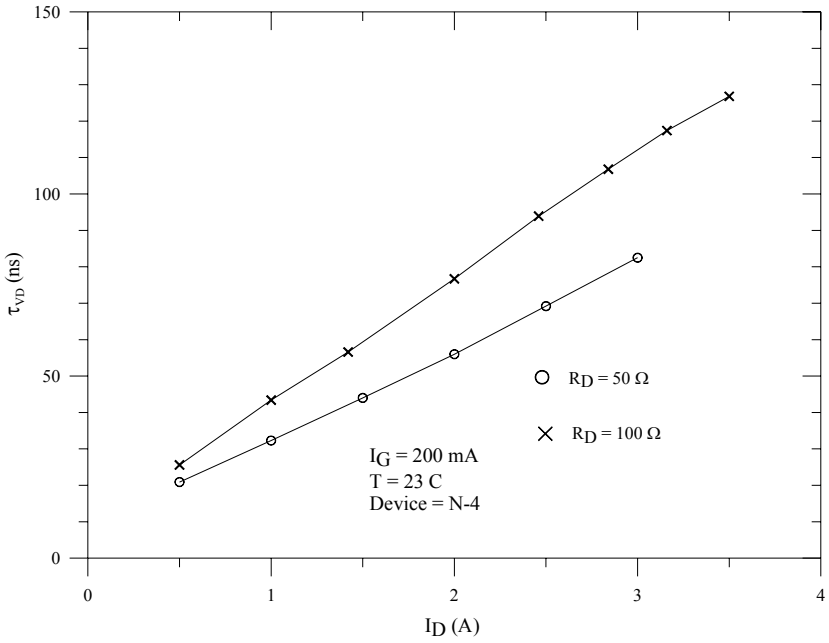

Figure 6.—Influence of the drain current magnitude on the drain voltage fall time at 23 °C for two values of the load resistor. Gate drive was a 200 mA current step.

V. Summary and Conclusions

Test results are presented for an experimental version of a 600 V, 3 A rated, Static Induction Transistor (SIT), or short, vertical channel JFET (VJFET), realized in 4H SiC. At zero gate bias, the gate p-n junction depletion layers extend far enough into the conduction channel to choke off conduction. Application of forward gate bias narrows the depletion regions, opening up the channel to conduction by majority carriers. The present device consists of a number of such short, vertically oriented channels working in parallel.

Statically traced drain current versus drain-to-source voltage curves, taken in the stepped gate voltage mode, unfortunately exhibit a well-known collapse as the temperature is increased. This property is reflected in pulse mode turn-on test results at selected temperatures, from room to 200 °C. Thus at 23 °C, 1 kW, or even more, could be pulse mode switched in 65 ns (10 to 90%) into a 100 Ω load. But at 200 °C, switching of just 1 A at this speed requires a gate pulse of about 400 mA. For currents above 1 A at 200 °C, the gate drive current becomes excessive.

The internal physics details of the normally-off SIT seem not to support hope for greatly improving the stability of the gate-to-drain transconductance characteristics over a wide temperature range, due to the inverse square law degradation of carrier mobility in the conduction channel with temperature. These 4H-SiC VJFET devices do not exhibit the increase in channel current with temperature reported by Rupp[8] for a normally-off 6H-SiC buried-gate JFET. Nevertheless, the SIT or VJFET structure has some points in its favor, compared to other SiC transistors under development. High carrier mobility in the conduction channel and the absence of a potentially unreliable gate insulation layer are advantages over present-day SiC MOSFETs. And minority carrier storage and diffusion seem not to detract from turn-on switching speed. But research literature[9–12] since the year 2000 indicates serious competition to the normally-off, 4H-SiC SITs coming from BJTs of the same material, suggesting that the characteristic curves of these BJTs do not collapse as much with temperature, at least to 200 °C.

References

[1]Zhao, J.H., et al., "6 A, 1 kV 4H-SiC Normally-off Trenched-and-Implanted Vertical JFETs", *Materials Science Forums,* Vols. 457–460, 2004, pp. 1213–1216.

[2]Zhao, J.H., et al., "Fabrication and Characterization of 11-kV Normally off 4H-SiC Trenched-and-Implanted Vertical Junction FET", *IEEE Electron Device Letters*, Vol. 25, No. 7, July 2004, pp. 474–476.

[3]Tone, K., et al., "4H-SiC Normally-Off Vertical Junction Field-Effect Transistor With High Current Density", *IEEE Electron Device Letters*, Vol. 24, No. 7, July 2003, pp. 463–465.

[4]Zhao, J.H., et al., "1710-V 2.77-mΩcm^2 4H-SiC Trenched and Implanted Vertical Junction Field-Effect Transistors", *IEEE Electron Device Letters*, Vol. 24, No. 2, February 2003, pp. 81–83.

[5]Sze, S.M., "*Physics of Semiconductor Devices*", 2nd edition, John Wiley, New York, 1981, Chapter 6.

[6]Kelner, G., et al., "α-SiC buried-gate junction field effect transistors", *Materials Science and Engineering*, Vol. B11, 1992, pp. 121–124.

[7]McLean, F.B., Tipton, C.W., and McGarrity, J.M., "Electrical Characterization of n-channel, 6H-SiC JFETS as a function of temperature", *5th SiC and Related Materials Conference*, Washington, DC, 1993. *Institute of Physics Conference Series*, No. 137, pp. 507–510.

[8]Rupp, R., et al., "Normally off 6H-SiC JFET and its high temperature operation", *5th SiC and Related Materials Conference*, Washington, DC, 1993. *Institute of Physics Conference Series*, No. 137, pp. 503–506.

[9]Zhao, J.H., et al., "A High Voltage (1,750 V) and High Current Gain (β = 24.8) 4H-SiC Bipolar Junction Transistor Using a Thin (12 μm) Drift Layer", *Materials Science Forums*, Vols. 457–460, 2004, pp. 1173–1176.

[10]Zhang, J., Alexandrov, P. and Zhao, J.H., "High Power (500 V – 70 A) and High Gain (44-47) 4H-SiC Bipolar Junction Transistors", *Materials Science Forums*, Vols. 457–460, 2004, pp. 1149–1152.

[11]Agarwall, A., et al., "SiC BJT Technology for Power Switching and RF Applications", *Materials Science Forums*, Vols. 457–460, 2004, pp. 1141–1144.

[12]Luo, Y., Fursin, L. and Zhao, J.H., "Demonstration of 4H-SiC power bipolar junction transistors", *Electronics Letters*, Vol. 36, No. 17, 17 August 2000, pp. 1496–1497.

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13. ABSTRACT ***(Maximum 200 words)***

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