Field Effect Transistor Behavior in Electrospun Polyaniline/Polyethylene Oxide Nanofibers

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Novel transistors and logic devices based on nanotechnology concepts are under intense development. The potential for ultra-low-power circuitry makes nanotechnology attractive for applications such as digital electronics and sensors. For NASA applications, nanotechnology offers tremendous opportunities for increased onboard data processing, and thus autonomous decision-making ability, and novel sensors that detect and respond to environmental stimuli with little oversight requirements. Polyaniline (PANi) is an intriguing material because its electrical conductivity can be changed from insulating to metallic by varying the doping levels and conformations of the polymer chain, and when combined with polyethylene oxide (PEO), can be formed into nanofibers with diameters ranging from approximately 50 to 500 nm (depending on the deposition conditions). The initial goal of this work was to demonstrate transistor behavior in these nanofibers, thus creating a foundation for future logic devices.

We have observed field effect transistor (FET) behavior in electrospun PANi/PEO nanofibers doped with camphorsulfonic acid. The nanofibers, nominally 100 nm in diameter and 200 – 400 microns long, were deposited onto Au electrodes that had been prepatterned onto oxidized silicon substrates, where the oxide thickness was 200 nm. We calculate PEO comprised about 9 weight percent of the composite nanofibers. Saturation channel currents were observed at source-to-drain voltages of -0.7 volts. The saturation drain current was controllable from 0.8 to 2.0 nanoamps by varying the gate voltage from +30 to -20 volts. The hole mobility in the depletion regime was 1.4×10^{-4} cm^2/V-sec, whereas the one-dimensional charge density (at zero gate bias) was calculated to be approximately 1 hole per 50 two-ring repeat units of polyaniline, consistent with the rather high channel conductivity (~10^{-3} S/cm). Reducing or eliminating the PEO content in the fiber is expected to enhance device parameters. Electrospinning is thus proposed as a simple method of fabricating one-dimensional polymer FET's.

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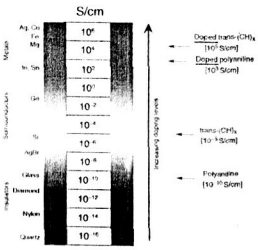
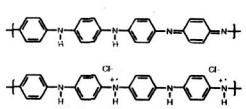
1. Introduction

Novel transistors and logic devices based on nanotechnology concepts are under intense development. The potential for ultra-low-power circuitry makes nanotechnology attractive for applications such as digital electronics and sensors. Furthermore, the ability to form devices on flexible substrates expands the range of applications where electronic circuitry can be introduced. For NASA, nanotechnology offers opportunities for increased onboard data processing and thus autonomous decisionmaking ability, and novel sensors that detect and respond to external stimuli with few oversight requirements. The goal of this work is to demonstrate transistor behavior in polyaniline/polyethylene oxide (PANi/PEO) nanofibers, thus creating a foundation for future logic devices.

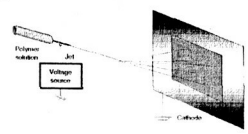
2. Nanofiber preparation



The electrical conductivity of bulk PANi can be varied from 10^{-10} to 6000 S/cm.

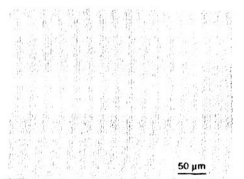


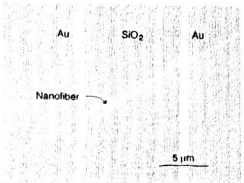
The fully reduced leucoeraldine base ($-(C_{24}H_{20}N_4)_x-$) form of PANi is an insulator and is made conductive upon protonation of the base by exposure to protonic acids or oxidative doping.



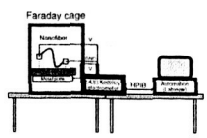
Electrospinning is used to form nanofibers. The accelerating voltage is 8 keV, and the anode-to-cathode distance is 25 cm.

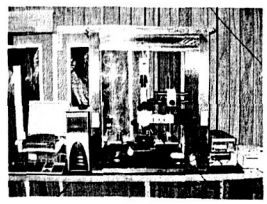
3. Electrical characterization





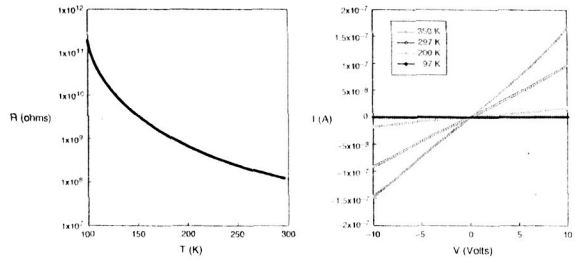
SEM images of nanofibers deposited on metallized SiO_2/Si substrates.





High-resistance measurements are taken using a Keithley model 6430 Sub-Femtoamp Remote Source meter. Samples are enclosed in a Faraday cage at 25 °C. The nanofibers can be optically imaged at magnifications up to 1600×.

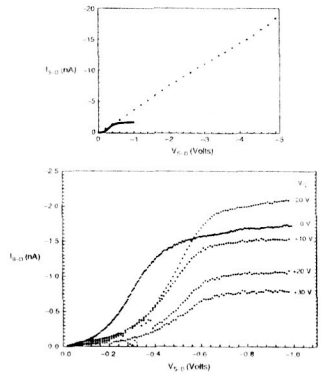
4. Electrical resistance



Electrical resistance as a function of temperature indicates the fibers are semiconducting

5. Transistor behavior

Transistor comprises fibers a and b with lengths equal to 12 and 18 microns, and diameters equal to 300 and 120 nm, contacting the two inner electrodes. The inset depicts a cross section of the device, showing a fiber bridging the gap between the source and drain.



I–V characteristics of the field effect transistor (FET) device made up of two nanofibers. The nanofiber is conditioned with a –5 V bias prior to displaying transistor behavior.

6. Conclusions

We have observed field effect transistor (FET) behavior in electrospun PANi/PEO nanofibers doped with camphor sulfonic acid. The nanofibers, nominally 100 nm in diameter and 200 to 400 microns long, were deposited onto Au electrodes that had been prepatterned onto oxidized silicon substrates where the oxide thickness was 200 nm. We calculate the PEO comprised about 9% wt of the composite nanofibers. Saturation channel currents were observed at source-to-drain voltages of –0.7 volts. The saturation drain current was controllable from 0.8 to 2.0 nanoamps by varying the gate voltage from 30 to –20 volts. The hole mobility in the depletion regime was 1.4×10^{-4} cm^2/V–sec, and the one-dimensional charge density (at zero bias) was calculated to be approximately one hole per 50 two-ring repeat units of polyaniline. Electrospinning is proposed as a simple method of fabricating one-dimensional polymer FETs.

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