ARCING IN LEO - DOES THE WHOLE ARRAY DISCHARGE?

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Abstract:

The conventional wisdom about solar array arcing in LEO is that only the parts of the solar array that are swept over by the arc-generated plasma front are discharged in the initial arc. This limits the amount of energy that can be discharged. Recent work done at the NASA Glenn Research Center has shown that this idea is mistaken. In fact, the capacitance of the entire solar array may be discharged, which for large arrays leads to very large and possibly debilitating arcs, even if no sustained arc occurs. We present the laboratory work that conclusively demonstrates this fact by using a grounded plate that prevents the arc-plasma front from reaching certain array strings. Finally, we discuss the dependence of arc strength and arc pulse width on the capacitance that is discharged, and provide a physical mechanism for discharge of the entire array, even when parts of the array are not accessible to the arcplasma front. Mitigation techniques are also presented.

Nomenclature

- A = Amperes of current
- C = Capacitance
- F = Farads of capacitance
- I = current
- LEO = Low Earth Orbit
- q = charge
- $\tau = \text{pulse width}$
- t = time
- x = dimensionless time
- V = voltage, electrical potential relative to space plasma

I. Introduction

Modern solar arrays have areas of tens of square meters, and they operate with bus voltages often exceeding 100 volts. Electrostatic discharges (arcs) are undesirable and detrimental events for spacecraft function, and preventing these events and/or mitigating their consequences are of primary importance for spacecraft designers. There are two types of plasma-related arcs that may occur in space. The first, the primary or trigger arc, is a transient event that discharges some spacecraft capacitance. The second type, the sustained arc, can occur between two solar array strings, and may be powered by the array's current generating capacity. In this paper, we consider only the transient trigger or primary arcs.

Ground tests of small samples of large solar arrays have been used to provide the necessary information regarding arc inception voltages and expected arc damage for an entire array during its lifetime in space. However, the volume of the space plasma and the size of the test arrays that may be simulated in ground tests is limited by the size of the test vacuum chamber, and this fact necessitates the installation of additional capacitance between the sample and ground to simulate the actual capacitance of a spacecraft and its solar array discharging through the arc plasma. The magnitude of the capacitance to be added has been the subject of discussions for many years (see for example Ref. 3). If the discharge of a space solar array capacitance is caused by an arc plasma front propagating along the array surface (see Ref. 1, p.

31), this magnitude is limited to about 1 microF, because the array capacitance is approximately 0.25 microF/m², and the propagation distance of the dense arc plasma is less than a few meters under the conditions of a typical LEO plasma.

On the other hand, if the entire array discharges through a current channel created by an arc, this capacitance can even reach 10^3 microF. The amplitude and width of an arc current pulse are both increasing functions of the capacitance discharged, and that is why the damage inflicted on the solar array by an arc depends on the capacitance discharged in the arc. Is it the capacitance reached by the dense arc-plasma front, or is it the much larger capacitance of the coverglasses of the entire array that is discharged?

The experiments described below confirm that the entire array capacitance discharges through the arc current channel even under conditions when the arc-plasma front is prevented from propagating along the sample surface. Thus, the proper value for an additional capacitor must be high ($\sim 10^3$ microF) for ground tests of arrays in order to properly simulate the damaging effects that may occur for arcs on spacecraft with large arrays.

II. Experimental Setup

All of our tests were done in the National Plasma Interactions Facility (N-PI Facility) at the NASA Glenn Research Center, Cleveland, Ohio. In our tests, the LEO space plasma was simulated in a large vacuum chamber (2 m in diameter and 3 m high) equipped with four oil diffusion vacuum pumps that provided a background pressure about 0.5 microTorr (66.6 microPascals). One Kaufmann-type plasma source generated a xenon plasma with an electron temperature of 1-1.3 eV, an electron number density of $(4-5)x10^5$ cm⁻³, and a neutral gas pressure of about 50 microTorr (6.67 milliPascals).

Two solar array samples (on fiberglass) were mounted on an aluminum sheet and installed vertically in the middle of the chamber (Fig.1). One sample (strings 1,2, and 3) represented a silicon solar array with UVR coverglasses of 300 micrometer thickness. That corresponds to a capacitance of 4344 pF/string. Another sample (strings 4, 5, and 6) had a capacitance of 7020 pF/string because of its thinner coverglasses (150 micrometer). The additional capacitor was chosen to have a capacitance of C = 0.03 microF (±10%) for the convenience of measurements - such a choice provided comparable currents in all branches of the bias circuit. However, some measurements were done with a higher capacitance (0.25 microF) to reveal the dependence of the arc current pulse characteristics on the value of this capacitance. Four current probes provided measurements of discharge currents flowing in essential branches of the circuit (Fig.2). For the second series of measurements, a grounded aluminum plate was installed between the samples to prevent the propagation of the arc-plasma front from one sample to the other.

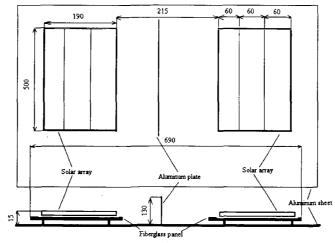


Figure 1. Two solar array samples are mounted on an aluminum sheet and installed vertically in a large vacuum chamber. All dimensions are shown in mm.

A. Experimental Results

All four current pulse wave forms were registered by a four channel digital oscilloscope and stored in a computer for further processing. Twenty events (arcs) were observed for each configuration (positions of keys 1-4, and capacitance C). That amounted to 260 files, one of which is shown in Fig.3. Each file was used to obtain the following data:

1) I_p - peak arc current; 2) $\tau_{0.5}$ - pulse width at 0.5 of the peak current value; 3) Δq_i -net electrical charge flowed through the corresponding branch; 4) t_{ij} - time interval between current pulse peaks in the different circuit branches.

The magnitude of the net electrical charge flowing through a branch was calculated as

$$\Delta q_i = \int I_i(t) dt \tag{1}$$

Then, the average and standard deviation over several measurements were calculated, and the resultant value was compared with the theoretically predicted value. For example, the ratio of charges for string #1 (Δq_1) and capacitor (Δq_2) was calculated by

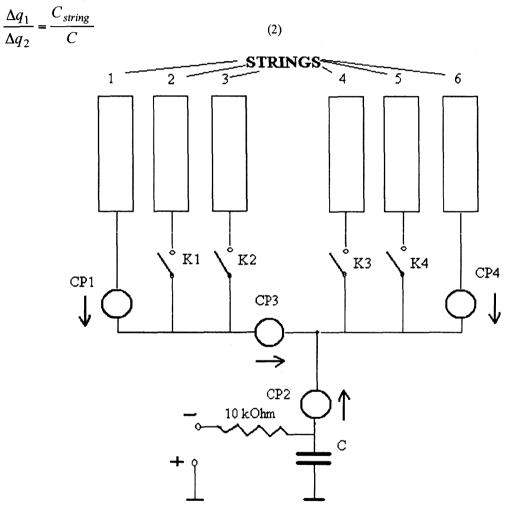


Figure 2. Four current probes were used to measure the discharge currents in four different branches of the circuit. The additional capacitance was chosen to be 0.03 microF to obtain comparable current magnitudes for all probes. A few measurements were done with C=0.25 microF.

It should be noted that the possible errors in the calculations of string capacitances could not be estimated properly because of unknown errors in the corresponding geometrical and electrical parameters. However, the consistency of all or our final results is a very convincing argument that the calculations of array capacitances were done with an error of less than 10%. Also, the following ratio

$$\frac{\Delta q_{arc}}{\Delta q_2} = \frac{\sum C_{string} + C}{C}$$
(3)

was verified for all events when the experimental setup made it possible to do so. This equality means that the array capacitance that discharged through the arc current channel is independent of the distance between the arc site and other strings, and the array discharged fully with or without an aluminum plate installed between the two samples.

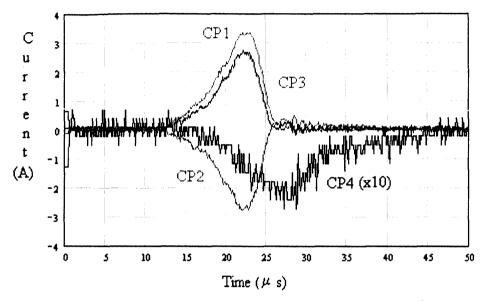


Figure 3. One example of an arc pulse current sequence for C=0.03 microF, and for switches K1&K2 in the closed position. CP1 is the most positive current. The arc was initiated at time t=0.

The results of our measurements and theoretical	l estimates are compiled	1 in Table 1. Standard deviations	(1σ) of the
measurements are shown in parenthesis.			

Table 1. Measurement Results and Theoretical Estimates											
	No	. Key	#: Arc c	on :	$\frac{\Delta q_i}{\Delta q_2}$:	$rac{\Delta q_i}{\Delta q_2}$:	$\frac{\Delta q_{arc}}{\Delta q_2}$:	$\frac{\Delta q_{arc}}{\Delta q_2}$	Bias
		<u>Closed:</u>	string#	<u>:</u> m	easured	:	<u>estimate</u> :	measured		estimate	<u>(V)</u>
	1	None	1	(0.25(0.03	3)	0.234(0.02)	1.186(0.11)	1.379(0.05)	300
	2	None	6	(0.17(0.03	3)	0.145(0.015)	1.077(0.04)	1.379(0.05)	300
	3	Κ	1/2	(0.25(0.02	24)	0.234(0.02)	1.41(0.08))	1.52(0.06)	300
	4	K1	6	0	.16(0.02)	0.145(0.015)	1.22(0.08)		1.52(0.06)	300
	5	K1&K2	2/3	0	.25(0.02	6)	0.234(0.02)	1.4(0.08)		1.67(0.07)	300
	6	K1&K2	6	0	.217(0.0	6)	0.434(0.04)	1.49(0.07)		1.67(0.07)	300
	7	K1&K2	2/3	0	.26(0.03	4)	0.234(0.02)	1.43(0.1)		1.67(0.07)	280
	8	K1&K2	6	0	.21(0.05)	0.434(0.04)	1.46(0.1)		1.67(0.07)	280
	9	All	4/5	0).19(0.05)	0.234 (0.02)			. ,	280
	10	All	2/3,6		``			1.85(0.06)		2.14(0.1)	280
	3 4 5 6 7 8 9	K K1 K1&K2 K1&K2 K1&K2 K1&K2 All	1/2 6 2/3 6 2/3 6 4/5	0 0 0 0 0 0	0.25(0.02 0.16(0.02 0.25(0.02 0.217(0.0 0.26(0.03 0.21(0.05	24) (6) (6) (4)	0.234(0.02) 0.145(0.015) 0.234(0.02) 0.434(0.04) 0.234(0.02) 0.434(0.04)	1.41(0.08) 1.22(0.08) 1.4(0.08) 1.49(0.07) 1.43(0.1) 1.46(0.1))	1.52(0.06) 1.52(0.06) 1.67(0.07) 1.67(0.07) 1.67(0.07) 1.67(0.07)	300 300 300 300 280 280 280

The numbers shown in Table 1 demonstrate a very good agreement between the measured parameters and their theoretical estimates. We believe that some insignificant differences can be explained by our poor knowledge of the string capacitances, possibly by a somewhat incomplete discharge of the panels, and possibly by a somewhat inhomogeneous plasma potential distribution. However, the considerably smaller-than-expected discharge of string #6 observed during two different runs (run numbers 6 and 8 above) cannot be explained to date. These results look particularly strange if one takes into account the very good agreement between the measurements for strings#2/3 and their estimated values (run numbers 5 and 7 above), because these two runs were supposed to be symmetrical to each other.

In the second stage of the experiment, an aluminum panel was installed between the two samples to prevent the propagation of the arc plasma from the arc site to the other sample (Fig.1). Measurements were done with the same additional capacitor (0.03 microF, $\pm 10\%$) and with another capacitor (0.22 microF, $\pm 5\%$) connected in parallel with the first one. The results are shown in Table 2.

	•	: Arc on string# :	$: \frac{\Delta q_i}{\Delta q_2}$ measured :	$\frac{\Delta q_i}{\Delta q_2}$ estimate	$: \frac{\Delta q_{arc}}{\Delta q_2}$: measured	$\frac{\Delta q_{arc}}{\Delta q_2}$: estimate	Bias (V)
1	K1&K2	2/3	0.21(0.03)	0.234(0.02)	1.32(0.07)	1.67(0.07)	450
-	K1&K2	1	. ,	• •	1.59(0.07)	1.67(0.07)	450
3	K1&K2	2/3) 0.956(0.02)	1.08(0.05)	400
4	K1&K2	1	0.028(0.002)	0.028(0.003	1.084(0.04)	1.08(0.05)	400
5	K1&K2	2/3	0.191 (0.02)	0.234(0.02)	1.39(0.06)	1.67(0.07)	400
6	K1&K2	1	0.203(0.024)	0.234(0.02)	1.63(0.1)	1.67(0.07)	400

Table 2. Experimental Results with Aluminum Panel installed.

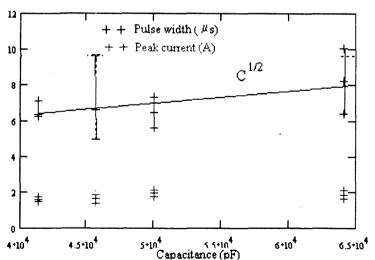
B. Analysis

It can be seen from the data in Tables 1&2 that those strings which were not arcing discharged fully in both cases - with or without the aluminum panel between the samples. Thus, the mechanism of discharge of an entire array can only be explained by an electron current flowing from the negatively charged conductor (or semiconductor) to the surrounding plasma through the arc-plasma conductive channel. When the arc occurs, the arc site comes toward the plasma potential, and the array capacitance pushes the coverglass potentials positive. The positive charge of the coverglass is neutralizing by ambient plasma electrons that are attracted by the (now) positive potential of the coverglass.

The dependences of the arc current pulse width and amplitude on the net capacitance were found from the experiments shown in Table 1. However, the narrow range of capacitances used (0.042-0.064 microF) and large deviations in the measured values did not allow us to confirm (or to reject) any expected square root dependence (Fig 4). For a discussion of the square root dependence, see Ref. 2.

For some measurements (shown in Table 2), a bigger additional capacitor (0.25 microF) was used, and this provided the opportunity to verify the expected dependence of the pulse width on the capacitance (Fig.5). It turned out that this dependence is slower than an expected (about 0.3 in power-law index, rather than the expected 0.5 [as Snyder depicted in Ref. 5]).

Figure 4. Arc current amplitudes and pulse widths vs. net capacitance are shown for the experiments without a conducting plate between the samples. Pulse width measurements are at top and peak current measurements are at bottom. Units are as in the legend at top.



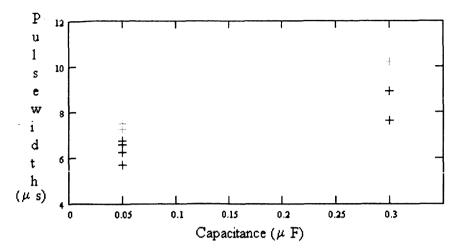


Figure 5. In spite of large deviations, a square root dependence of pulse width on capacitance can be excluded. The actual dependence is closer to a $C^{1/3}$ dependence.

One more interesting feature of the discharge process is a time delay between the instant of the peaks in the arc-current pulse and in the discharge current of those strings not arcing (Fig.3). We believe that this delay is caused by a changing plasma potential during the discharge process (which corresponds to the spacecraft potential for LEO orbit). In actuality, in the simple situation when all keys (K1-K4) are open, and the arc occurs on string #1, the relaxation current on string #6 satisfies the following equation (Eq. 4):

$$\frac{dI_4(x)}{dx} + I_4(x) = -\frac{C_{str}}{C} \cdot I_1(x)$$
(4)

where $x = \frac{t}{\tau_{str}}$, and τ_{str} is the string relaxation time.

The solution of the Eq.4 with the initial condition $I_4(0) = 0$ can be written as

$$I_4(x) = -\frac{C_{str}}{C} \cdot \exp(-x) \cdot \int_0^x I_1\left(\frac{C_{str}}{C}t\right) \cdot \exp(t) \cdot dt$$
(5)

If the arc current pulse is simulated by two exponents or by a Gaussian curve, the solution of Eq. (5) is shown in Fig.6.

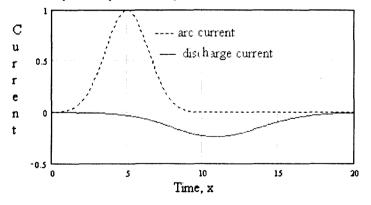


Figure 6. The theoretical time delay (in x units) between peaks of arc current and string discharge current is similar to the observed one.

The measured time delay between current peaks in strings 1 and 6 was:

- 1. With 280 V, no plate, 0.03 capacitor 2.6(0.8) microseconds;
- 2. With 450 V, plate, 0.03 capacitor 4.88(1.68) microseconds.

III. Conclusion

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The results of our current experiments and their analysis confirm the necessity of using a large additional capacitance (0.3-0.5 of the expected entire spacecraft solar array capacitance) in ground tests in order to adequately simulate the consequences of arcing on solar arrays in orbit. Spacecraft solar arrays that have very large capacitances connected to spacecraft ground may be damaged by even transient arcing events unless mitigation techniques are used. For example, a spacecraft solar array with a 300 V power system and 10 microfarad surface capacitance may be subject to arcs of more than 1000 amp peak strength and total energies greater than 0.4 Joule, even if the arcs do not become sustained by the array power. Miller⁴ showed that even arcs of 40 A peak strength may severely damage solar cell interconnects.

IV. Mitigation (reprinted from Ref. 1, p. 38)

The design of a solar array must consider the plasma environment and interactions with that environment. Arc prevention is extremely important. The following techniques have been shown in ground and flight tests to prevent arcs or minimize their damage:

1. If possible, use array string voltages of less than 55 V. No trigger arcs have been seen on LEO arrays of less than about 55 V string voltage even under simulated micrometeoroid bombardment. Solar arrays coming out of eclipse will generate more voltage than when they operate at their max power point.

2. If solar array cell edges or interconnects are exposed to the LEO plasma and string voltages are greater than 55 V, the strings should be laid out on the substrate such that no two adjacent cells have a voltage difference of greater than 40 V. Sometimes a leapfrog arrangement will be sufficient. In other high voltage arrays, the strings should be arranged parallel to each other. Serpentine strings can be used to prevent the array width from becoming prohibitive. If the string layout cannot be modified to prevent cells with more than 40 V difference being adjacent to each other (anything less than about 1 cm may be considered adjacent) then the total string voltage must be kept low enough that the initial (trigger) arcs do not take place. The lowest known array trigger arcing has occurred on thin-coverglass cells at about 75 volts (See Ref. 7, PASP Plus results).

3. For array string voltages greater than about 75 V, trigger arcs in LEO can only be completely prevented by encapsulating the cell or array edges so they do not see the ambient plasma. If encapsulation is not possible, a thorough array bakeout on-orbit (1 week at 100 C or more) may get rid of contaminants and prevent trigger arcing up to about 300 V, or possibly more (see Ref. 8). Re-contamination may occur on "dirty" spacecraft (spacecraft with excessive venting, cold gas nozzles, etc.). Good encapsulation may prevent arcing up to 1000 V string voltage.

4. Sustained (or continuous) arcs may occur whenever trigger arcs occur and adjacent cells have more than 40 V potential differences. However, sustained arcs, in addition to this voltage threshold, have a current threshold, below which they will not occur. It is believed that the current threshold is greater than about 0.5 Amp. If the current produced by each cell is above this threshold, a single string may sustain arcs. If each cell is below this current threshold, then isolating separate strings of solar cells from each other will prevent other strings from "feeding" the arc site, and will prevent sustained arcs. This isolation can be achieved by using blocking diodes in each string (EOS-AM1, now called Terra, e.g. Ref. 6, for instance). Care must be taken that the power bus and/or other components do not have the conditions necessary for sustained arcing. On the Terra arrays, for instance, it was found that diodes used to block interstring currents did not prevent the bus power traces from having sustained arcing events. Covering all exposed bus conductors with Kapton® insulation finally solved the problem. Low-outgassing RTV may be used to cover bare conductors as well.

5. RTV grout between adjacent solar cells and strings that have a high voltage with respect to each other has been shown to effectively block sustained arcs between cells and strings. The degree of coverage, etc., is important in determining the final voltage threshold for sustained arcing.

6. Arrays of 300 V and greater string voltage must be fully encapsulated in order to prevent arcing.

7. Finally, although design and construction are important in preventing trigger arcs and sustained arcs, each new solar array implementation must be tested in a simulated LEO plasma before it can be sure not to arc. This step must not be omitted. The test bias voltage relative to the plasma should include the maximum when the arrays come out of eclipse (or the highest potential expected on the "floating" spacecraft). The interstring

voltage should be at least as great as that expected anywhere on the solar array on-orbit. Tests should ideally be conducted at sample temperatures as low as the eclipse-egress temperature.

V. Mitigation Techniques on Other Spacecraft

On the International Space Station (ISS), ground-testing of the solar arrays showed that the arrays did not arc at negative voltages less than about 250 volts. This is much less than the system operating voltage (160 V), so in the absence of auroral charging, ISS is never expected to charge more than 160 V negative. And, if trigger arcs do not occur, sustained arcs will not. However, ISS did take the precaution of incorporating a system of PCUs (plasma contactor units) to prevent structure charging by the solar arrays and to prevent dielectric breakdown of anodized aluminum surfaces.

The LEO Design Guidelines (Ref. 1) referenced above were based on partly on ground tests done for the SS/Loral satellite series and the EOS-AM1 spacecraft (now called Terra). Mitigation techniques called out above were the partly the result of those tests, and therefore should be considered to be based on real spacecraft experience in failure modes and failure investigations.

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