MODELING OF METAL-FERROELECTRIC-SEMICONDUCTOR FIELD EFFECT TRANSISTORS

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The characteristics for a MFSFET (metal-ferroelectric-semiconductor field effect transistor) is very different than a conventional MOSFET and must be modeled differently. The drain current has a hysteresis shape with respect to the gate voltage. The position along the hysteresis curve is dependent on the last positive or negative polling of the ferroelectric material. The drain current also has a logarithmic decay after the last polling. A model has been developed to describe the MFSFET drain current for both gate voltage on and gate voltage off conditions. This model takes into account the hysteresis nature of the MFSFET and the time dependent decay. The model is based on the shape of the Fermi-Dirac function which has been modified to describe the MFSFET's drain current. This is different from the model proposed by Chen et. al.[1] and that by Wu[2].

Keywords: ferroelectric transistors; hysteresis modeling; ferroelectric time decay

INTRODUCTION

Several Integrated Circuits containing PZT channel metal-ferroelectric-semiconductor field effect transistors (MFSFET) were obtained from Radiant Technologies Incorporated located in Albuquerque, New Mexico. The transistors were fabricated from silicon but have the channel fabricated from thin film PZT. This allows the gate to source voltage to either open or close the channel. The channel will remain opened or closed even after the gate to source voltage is removed. These transistors were characterized by recreating a circuit and reproducing the data as described in a correspondence from Radiant Technologies in April, 1993[5][6].

TESTING THE MFSFET

Test Setup

The tests were performed by setting up the circuit shown in Figure 1.

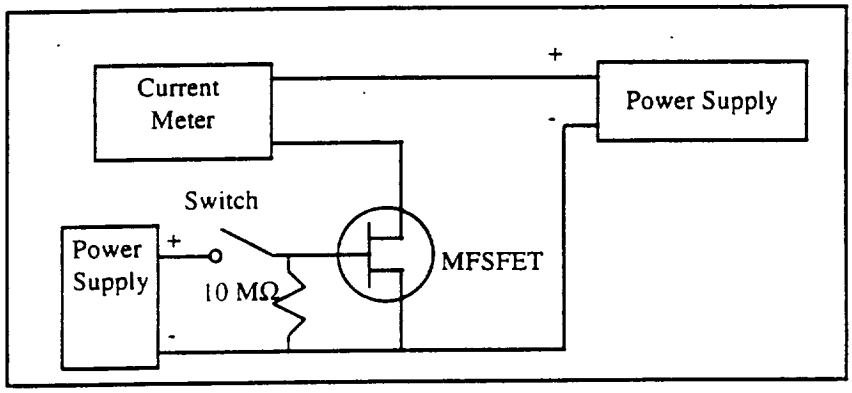


FIGURE 1. Ferroelectric Field Effect Transistor Test Setup

With the Drain to Source voltage held constant, a series of pulses were sent to the Gate of the MFSFET. To establish the initial conditions, a -8.0 volt polling pulse was applied. This polling pulse saturated the ferroelectric channel in the open position. The Gate pulses started at 0.0 volts and was increased by 0.50 volts until the pulses reached +8.0 volts. The amplitude of the pulses was then decreased by 0.50 volts until 0.0 volts was again reached. Then a +8.0 polling pulse was applied. This polling pulse place the ferroelectric channel into saturation with the channel closed. Negative pulses were then applied every 0.50 volts from 0.0 volts to -8.0 volts and back to 0.0 volts. Figure 2 shows the series of pulses that were applied to the MFSFET Gate.

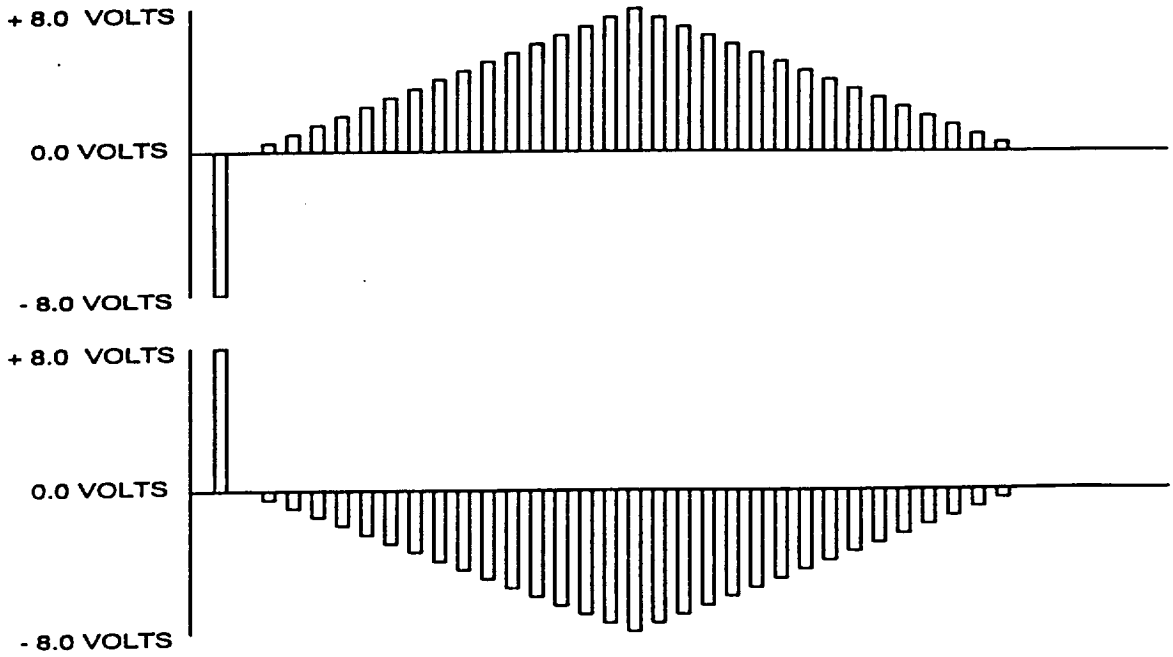
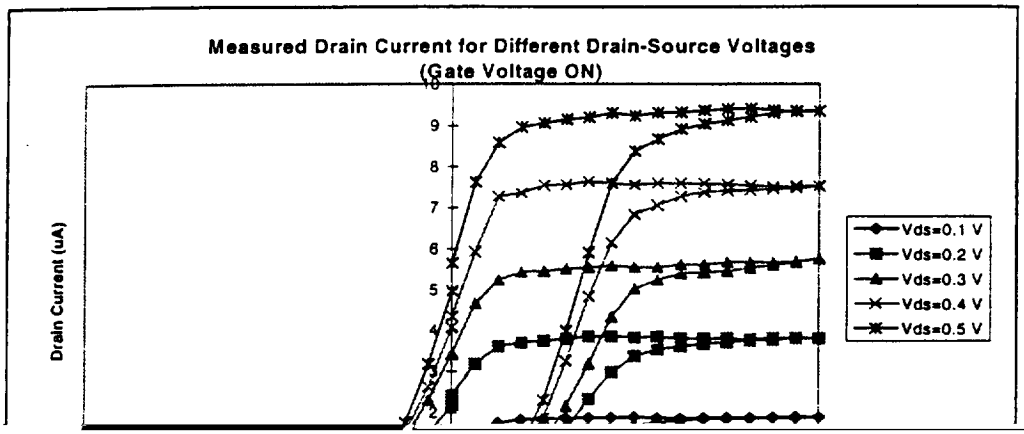


FIGURE 2 Pulse Pattern Sent to MFSFET Gate

When the switch is thrown applying voltage to the Gate, a reading is made of the channel current. This is described as the "On" current because it is the current flowing when the MFSFET is actively be operated. The switch is then closed, removing any voltage to the Gate (the 10 megaohm resistor insures that the Gate and Source are at the same voltage when the switch is open). A second reading of channel current is then made. This current is described as the "Off" current because the transistor is not actively being operated. This "Off" current will continue to flow as long as a voltage is applied from the Drain to the Source.

The Drain to Source voltage is nominally set at 0.4 volts. To characterize the effects of Drain to Source voltage on channel polarization retention, the voltage was varied from 0.1 volts to 0.5 volts. After the Drain to Source voltage was set, the gate was pulsed with pulses in the same manner as was done to characterize the effects of Gate voltage. Figure 3 shows the effects of varying the Drain to Source voltage on the MFSFET transistor.


Measured Drain Current for Different Drain-Source Voltages
(Gate Voltage ON)
Drain Current (uA)
10
9
8
7
6
5
4
3
2
Vds=0.1 V
Vds=0.2 V
Vds=0.3 V
Vds=0.4 V
Vds=0.5 V

Remnant Current Retention

The ferroelectric transistor must be able to store data for long periods of time. To measure the polarization retention characteristics of the MFSFET, measurements were made of the channel current over long periods of time. The channel was set to the open state by sending a -8.0 volt pulse to the Gate. This causes the ferroelectric channel to be saturated. The voltage to the Gate is removed and the current is measured for up to 7000 seconds. Figure 4 shows the retention data for the ferroelectric MFSFET.

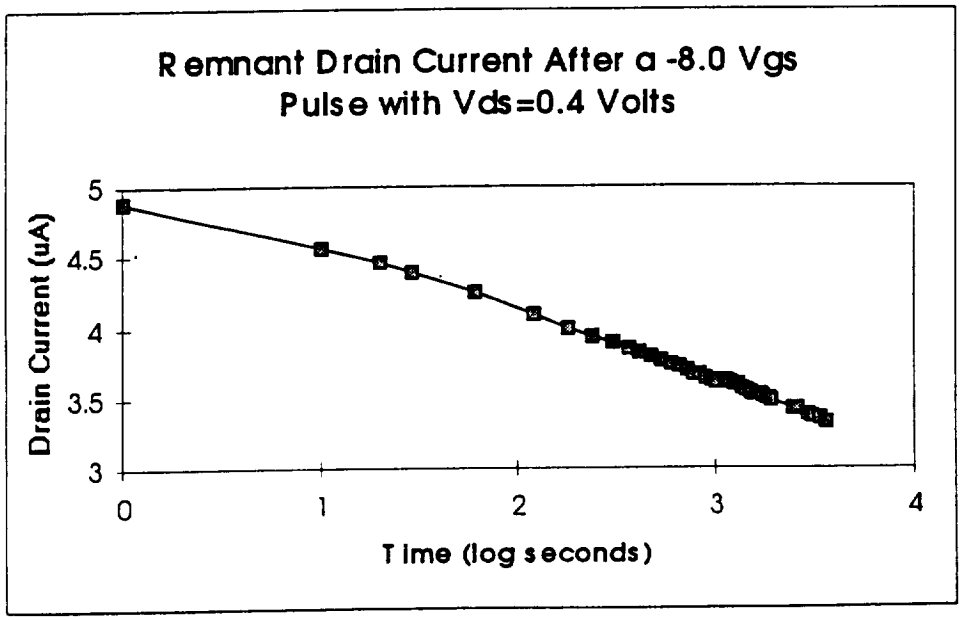


Figure 4 Ferroelectric MFSFET Remnant Current Data

The MFSFET retention data shows that the degradation of the Drain current is linear with the logarithm of time. The relationship can be given by the equation:

$$I_D = A - B \log (\text{time}) \qquad (1)$$

Where:

I_D = the current flowing through the Drain

A = the initial current flow through the Drain

B = the coefficient that gives the rate of current decay

Using the least squares method of data reduction the coefficients A and B can be calculated. Table 1 shows the calculation of A and B for the transistor at room temperature with Vds at 0.4 volts .

N	Time (s)	I_D (mA)	Log (t)	Log $(t)^2$	Log (t)* I_D
1	1	4.89	0	0	0
2	10	4.56	1	1	4.56
3	100	4.06	2	4	8.12
4	500	3.79	2.69897	7.28444	10.2290963
5	1000	3.6	3	9	10.8
6	2000	3.47	3.30103	10.8968	11.4545741
7	4000	3.32	3.60206	12.9748	11.9588392
N=7	Sum:	27.69	15.6021	45.1561	57.1225096
			$I_{D\ ave}$ =	3.95571	

A	B	$I_{D\ est}$	r_{ss}	t_{ss}	$R^2=(t_{ss}-r_{ss})/t_{ss}$
4.942	**-0.44261**	4.942226	0.00273	0.87289	**0.99545334**
		4.499619	0.00365	0.36516	
		4.057012	8.9E-06	0.01088	
		3.747643	0.00179	0.02746	
		3.614405	0.00021	0.12653	
		3.481167	0.00012	0.23592	
		3.347929	0.00078	0.40413	
		Sum:	**27.69**	**0.0093**	**2.04297143**

Table 1 Calculation of retention Coefficients for Ferroelectric Field Effect Transistors

MODELING OF THE MFSFET

There are two types of standard Field Effect transistors; Enhancement mode and Depletion mode. An Enhancement mode MFSFET allows no current to flow between the source and the drain when the gate voltage is zero. As the gate voltage increases from zero, the source drain current increases until it is saturated. A Depletion mode MOSFET allows current to flow between the source and drain when the gate voltage is zero. As the gate voltage increases from zero, the source-drain current is pinched off until it reaches zero. The ferroelectric MFSFET acts as both an enhancement mode and a depletion mode transistor. If the gate has received a negative pulse, negative polled, then the MFSFET will act as depletion mode transistor. If the MFSFET has received a positive pulse, positive polled, it will behave as an enhancement mode MOSFET.

Two separate models must be used to characterize an MFSFET, one enhancement mode model and a depletion mode model.

The first attempt to model the MFSFET was to use the standard MOSFET model. For a depletion mode MOSFET, Boylestad[3] gives the equation for the drain current

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2 \qquad (2)$$

Where

I_D = drain current

I_{DSS} = the drain-source current with the gate and source shorted

V_{GS} = the gate source voltage

V_p = the pinch-off voltage where I_D equals 0

This equation yields a the following curve depicting drain current versus gate voltage .

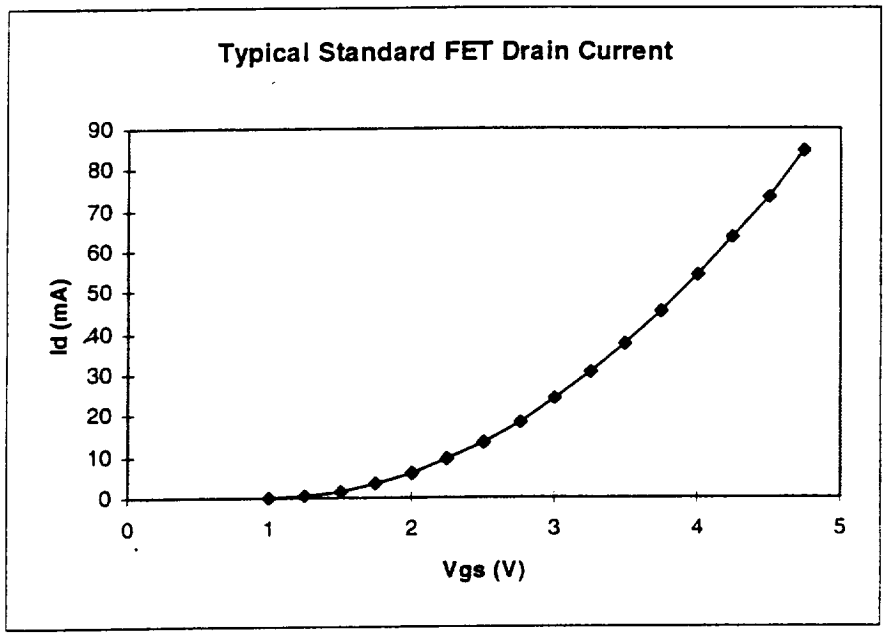


FIGURE 5 Drain current from Standard MOSFET Model

This curve does not fit the MFSFET drain current curve at all. Even though the MFSFET is structurally very similar to a standard MOSFET, the current characteristics are very different. A different type of equation is needed to model the MFSFET. The equation that has the most similar shape to the MFSFET is the Fermi-Dirac function. This function describes the distribution of electrons at different energy levels. Lo[4] gives the Fermi-Dirac function as

$$f(E) = \frac{1}{e^{(E-Ef)T} + 1} \tag{3}$$

Where

f(E) = the probability of finding an electron at Energy E at Temperature T

E_f = called the Fermi level for a particular electron shell

T = the absolute temperature in Kelvin

The use of this equation to describe the drain current in an MFSFET is only because of its shape and not because drain current is related to the distribution of electrons within an atom's energy shells. The Fermi-Dirac function must be changed to be used to model the MFSFET. The following equation was created to model the MFSFET drain current with the gate voltage ON.

$$I_D = \frac{I_{DSAT} - B * Log(t_1)}{e^{k(Vp-Vgs)} + 1} \tag{4}$$

and

$$I_D = \frac{I_{DSAT} - B * Log(t_1)}{e^{k(Vgs-Vp)} + 1} \tag{5}$$

when the gate voltage is OFF.

Where

I_D = the drain current

I_{DSAT} = the value for the drain current when the MFSFET is saturated

B = the decay coefficient

t_l = the time in seconds since the last polling

Vgs = the gate to source voltage

Vp = the gate voltage at which half of the saturation current is achieved (Each MFSFET has two Vp's one for the negatively polled current and one for the positively polled current thus giving the hysteresis characteristic.)

k = a constant that defines the rate of change of the function

For the MFSFET in this research, the following values for the variables are used to model the drain current.

For the gate voltage ON

Vp = 2.5 V for positively polled

Vp = -0.5 V for negatively polled

k = 1.7

I_{DSAT} = 9.0 uA for Vds= 0.5 V

7.2 uA for Vds= 0.4 V

5.3 uA for Vds= 0.3 V

3.5 uA for Vds= 0.2 V

1.8 uA for Vds= 0.1 V

For the model with the gate voltage OFF

Vp = -4.2 V for positively polled

Vp = 1.5 V for negatively polled

k=1.7

I_{DSAT} = 6.5 uA for Vds= 0.5 V

5.2 uA for Vds= 0.4 V

4.0 uA for Vds= 0.3 V

2.5 uA for Vds= 0.2 V

1.2 uA for Vds= 0.1 V

t_1= 1 second if immediately after polling

or

t_1 is increased by 20 seconds for each measurement

Using the above values for the drain current model yields the following curves shown in figures 6 and 7.

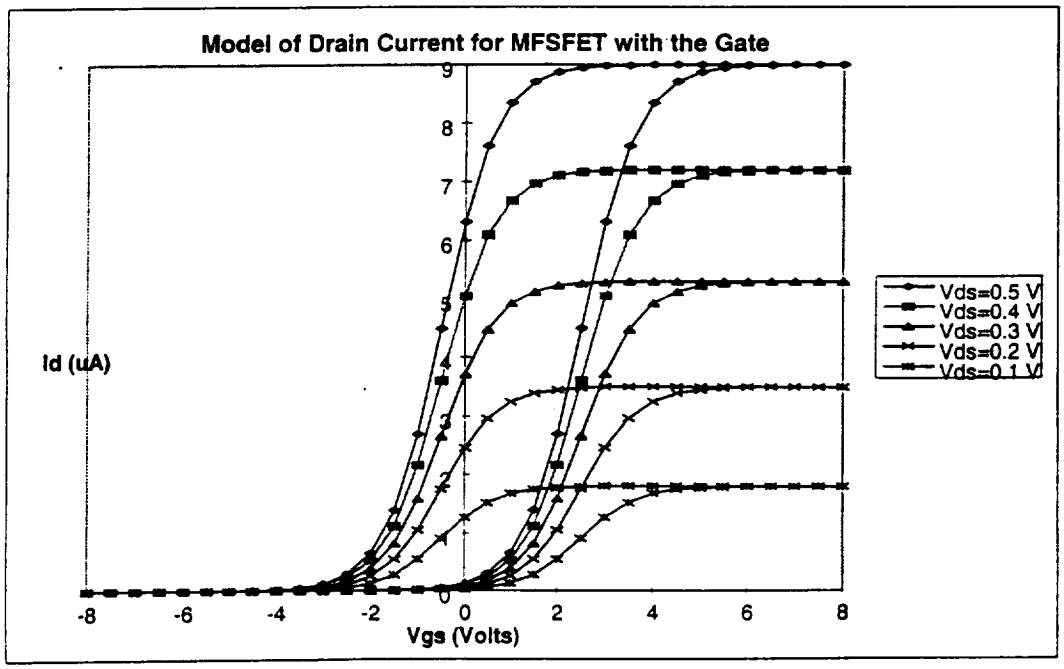


FIGURE 6 Predicted Drain Current using MFSFET Model (Gate ON)

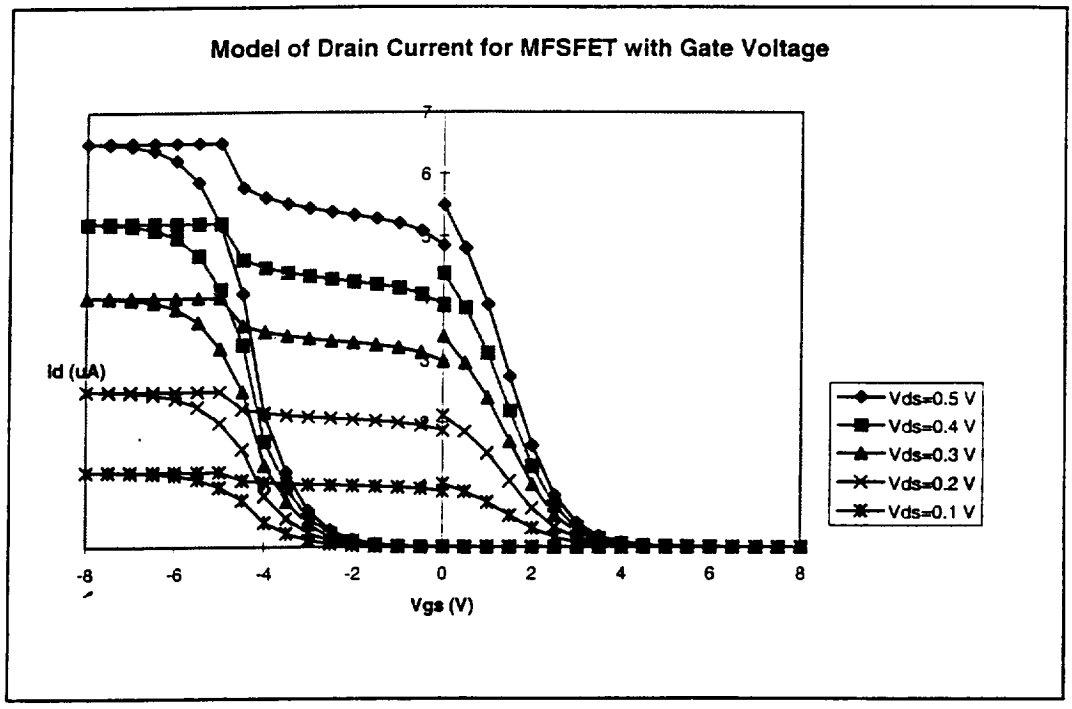


FIGURE 7 Predicted Drain Current using MFSFET Model (Gate OFF)

When these curves are compared with the observed data in Figure 3, the predicted drain current is very close the measured data. The Data used to create the MFSFET model is shown in Table 2.

Vgs	Id=.5	Id=.4	Id=.3	Id=.2	Id=.1	k	Vp	Id_{sat} .5	0.4	0.3	0.2	0.1	Delay time
0	5.495	4.396	3.382	2.113	1.015	1.7	1.5	5.924	4.739	3.646	2.278	1.094	11
1	3.892	3.113	2.396	1.497	0.719	1.7	1.5	5.556	4.444	3.419	2.136	1.026	51
2	1.622	1.297	0.998	0.624	0.299	1.7	1.5	5.417	4.333	3.334	2.083	1	91
3	0.386	0.309	0.238	0.148	0.071	1.7	1.5	5.329	4.263	3.28	2.049	0.984	131
4	0.074	0.059	0.046	0.028	0.014	1.7	1.5	5.265	4.212	3.241	2.024	0.972	171
5	0.017	0.014	0.01	0.006	0.003	1.7	1.5	6.5	5.2	4	2.5	1.2	1
6	0.003	0.002	0.002	0.001	6E-04	1.7	1.5	6.5	5.2	4	2.5	1.2	1
7	6E-04	5E-04	3E-04	2E-04	1E-04	1.7	1.5	6.5	5.2	4	2.5	1.2	1
8	1E-04	8E-05	6E-05	4E-05	2E-05	1.7	1.5	6.5	5.2	4	2.5	1.2	1
7	3E-08	3E-08	2E-08	1E-08	6E-09	1.7	-4.2	6.5	5.2	4	2.5	1.2	1
6	2E-07	2E-07	1E-07	7E-08	4E-08	1.7	-4.2	6.5	5.2	4	2.5	1.2	1
5	1E-06	8E-07	6E-07	4E-07	2E-07	1.7	-4.2	6.5	5.2	4	2.5	1.2	1
4	5E-06	4E-06	3E-06	2E-06	9E-07	1.7	-4.2	5.769	4.615	3.55	2.218	1.065	21
3	3E-05	2E-05	2E-05	1E-05	5E-06	1.7	-4.2	5.513	4.41	3.393	2.12	1.018	61
2	1E-04	1E-04	9E-05	5E-05	3E-05	1.7	-4.2	5.392	4.313	3.319	2.073	0.996	101
1	8E-04	6E-04	5E-04	3E-04	1E-04	1.7	-4.2	5.311	4.249	3.269	2.042	0.981	141
0	0.004	0.003	0.003	0.002	8E-04	1.7	-4.2	5.252	4.201	3.232	2.019	0.97	181
-1	0.022	0.018	0.014	0.009	0.004	1.7	-4.2	5.204	4.162	3.203	2.001	0.961	221
-2	0.12	0.096	0.074	0.046	0.022	1.7	-4.2	5.164	4.13	3.178	1.985	0.954	261
-3	0.59	0.472	0.363	0.227	0.109	1.7	-4.2	5.129	4.103	3.157	1.972	0.947	301
-4	2.12	1.696	1.305	0.815	0.392	1.7	-4.2	5.099	4.079	3.139	1.961	0.942	341
-5	5.172	4.138	3.183	1.989	0.955	1.7	-4.2	6.5	5.2	4	2.5	1.2	1
-6	6.209	4.967	3.821	2.388	1.146	1.7	-4.2	6.5	5.2	4	2.5	1.2	1
-7	6.445	5.156	3.966	2.479	1.19	1.7	-4.2	6.5	5.2	4	2.5	1.2	1
-8	6.49	5.192	3.994	2.496	1.198	1.7	-4.2	6.5	5.2	4	2.5	1.2	1
-7	6.5	5.2	4	2.5	1.2	1.7	1.5	6.5	5.2	4	2.5	1.2	1
-6	6.5	5.2	4	2.5	1.2	1.7	1.5	6.5	5.2	4	2.5	1.2	1
-5	6.5	5.2	4	2.5	1.2	1.7	1.5	6.5	5.2	4	2.5	1.2	1
-4	5.608	4.486	3.451	2.156	1.035	1.7	1.5	5.608	4.486	3.452	2.156	1.035	41
-3	5.442	4.353	3.35	2.092	1.005	1.7	1.5	5.445	4.355	3.351	2.093	1.005	81
-2	5.334	4.267	3.283	2.051	0.985	1.7	1.5	5.348	4.278	3.292	2.056	0.988	121
-1	5.205	4.164	3.204	2.001	0.961	1.7	1.5	5.28	4.223	3.25	2.03	0.975	161
0	4.848	3.878	2.984	1.864	0.895	1.7	1.5	5.226	4.181	3.217	2.009	0.965	201

TABLE 2 Data used to create MFSFET model (Gate Off)

CONCLUSIONS

Because of the hysteresis characteristic of the MFSFET the model is complex, but by using the modified Fermi-Dirac shaped function a very accurate model of the MFSFET is possible.

Acknowledgments

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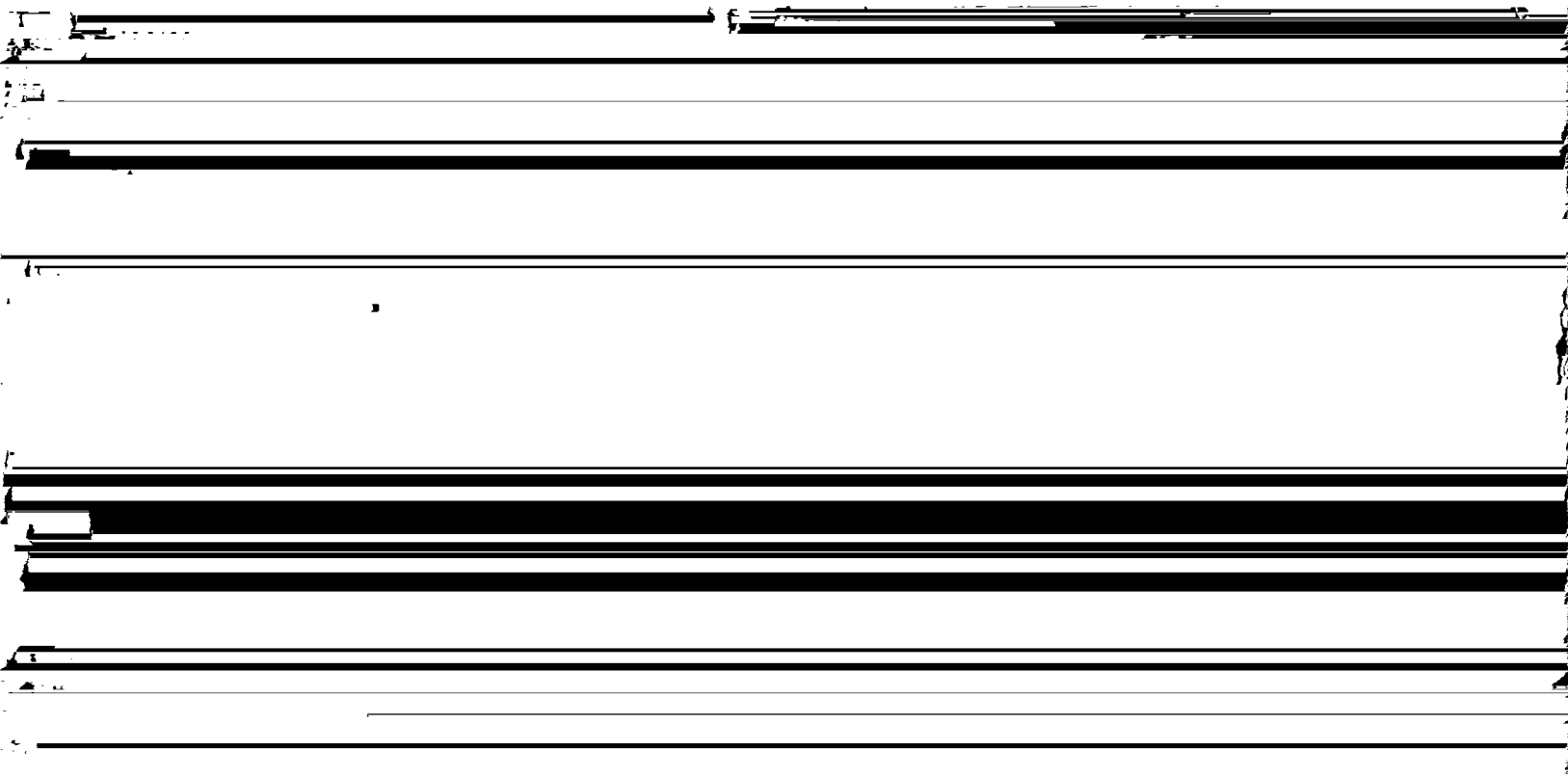

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