# EMBEDDED MULTIPROCESSOR TECHNOLOGY FOR VHSIC INSERTION

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- A Workshop

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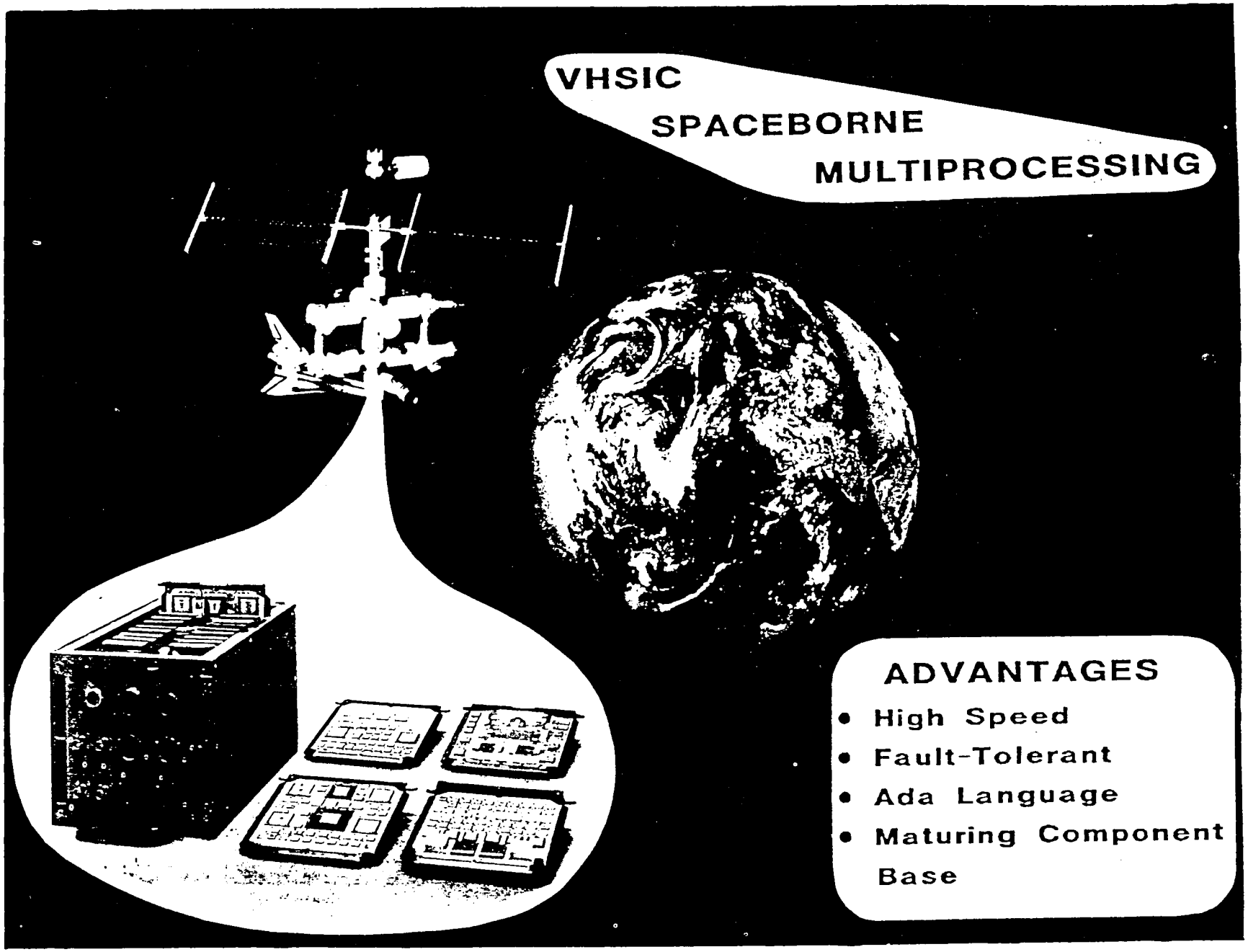
NASA


VHSIC
SPACEBORNE
MULTIPROCESSING
ADVANTAGES
• High Speed
• Fault-Tolerant
• Ada Language
• Maturing Component Base

# NASA MULTIPROCESSOR TECHNOLOGY

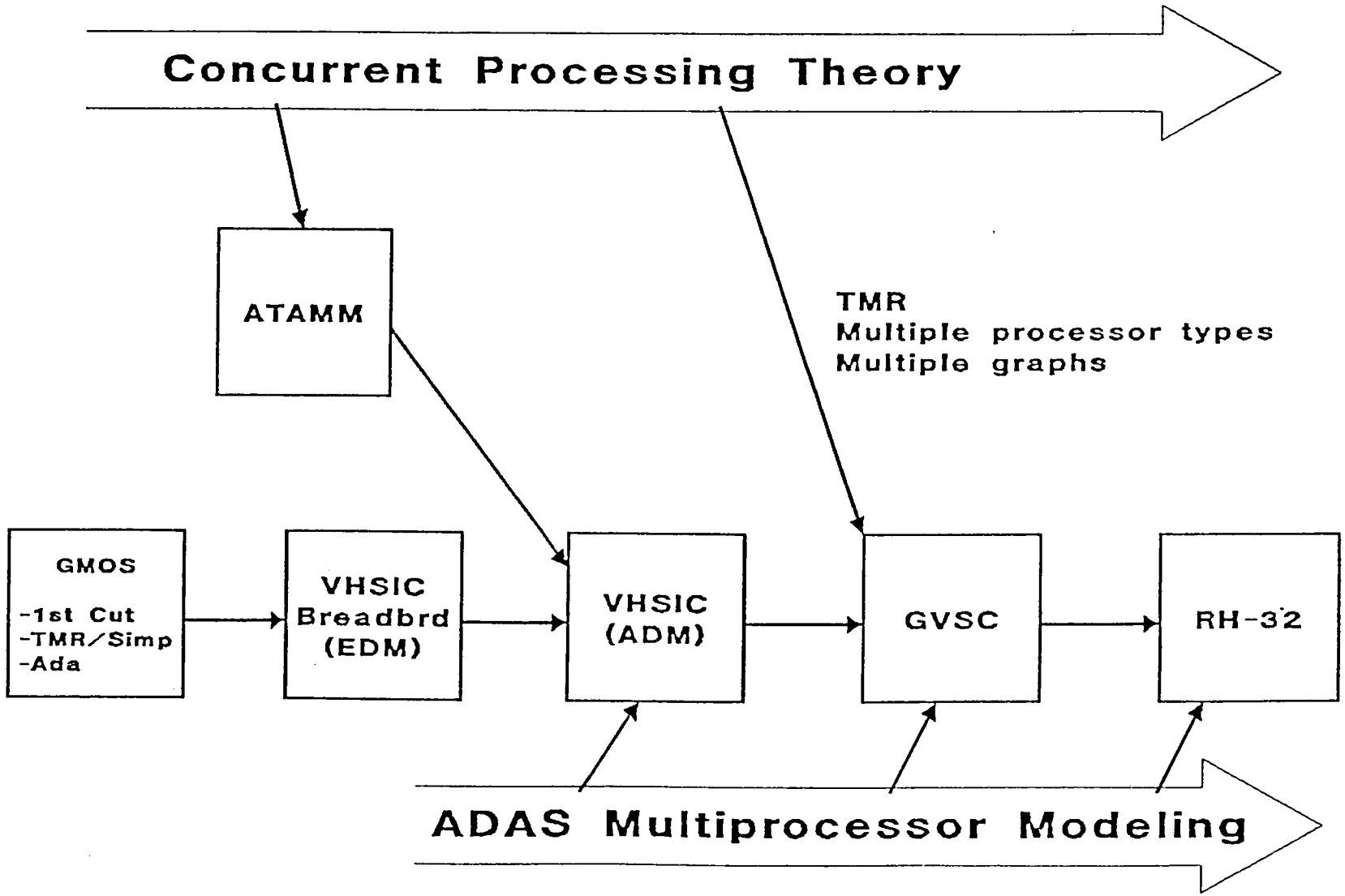
## OBJECTIVE

Develop multiprocessor system technology providing user-selectable fault tolerance, increased throughput, and ease of application representation for concurrent operation.

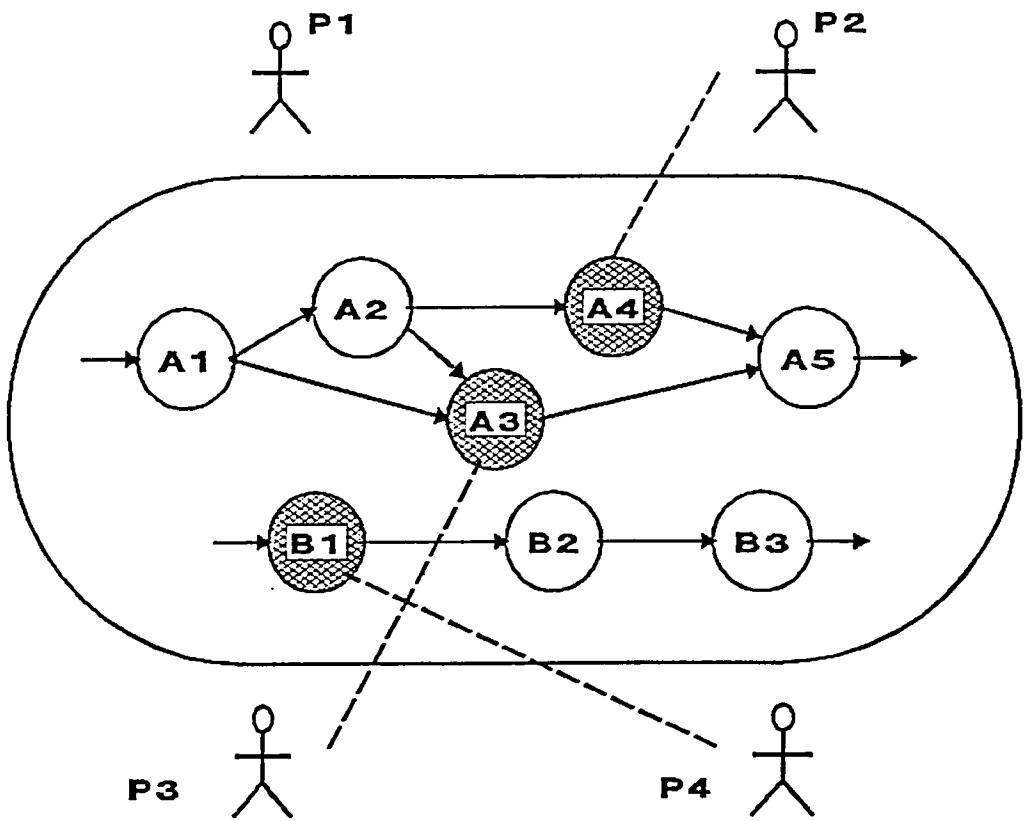
## APPROACH

Develop graph management mapping theory for proper performance, model multiprocessor performance, and demonstrate performance in selected hardware systems.

# MULTIPROCESSING TECHNOLOGY



# Graph Management Operating System (GMOS)




Processor Assignment for Node Execution

## Features

- Distributed O/S and Nodes
- Real-Time Node Assignment
- Application Graph
- Node-Selectable Fault Tolerance
- Ada
- VHSIC 1750A

# GMOS FUNCTIONAL FEATURES

- EXECUTES DIRECTED GRAPH - SINGLE GRAPH
  - MULTIPLE GRAPH
- GRAPH NODE CRITICALITY - TMR OR SIMPLEX
- GRAPH NODE SCHEDULING

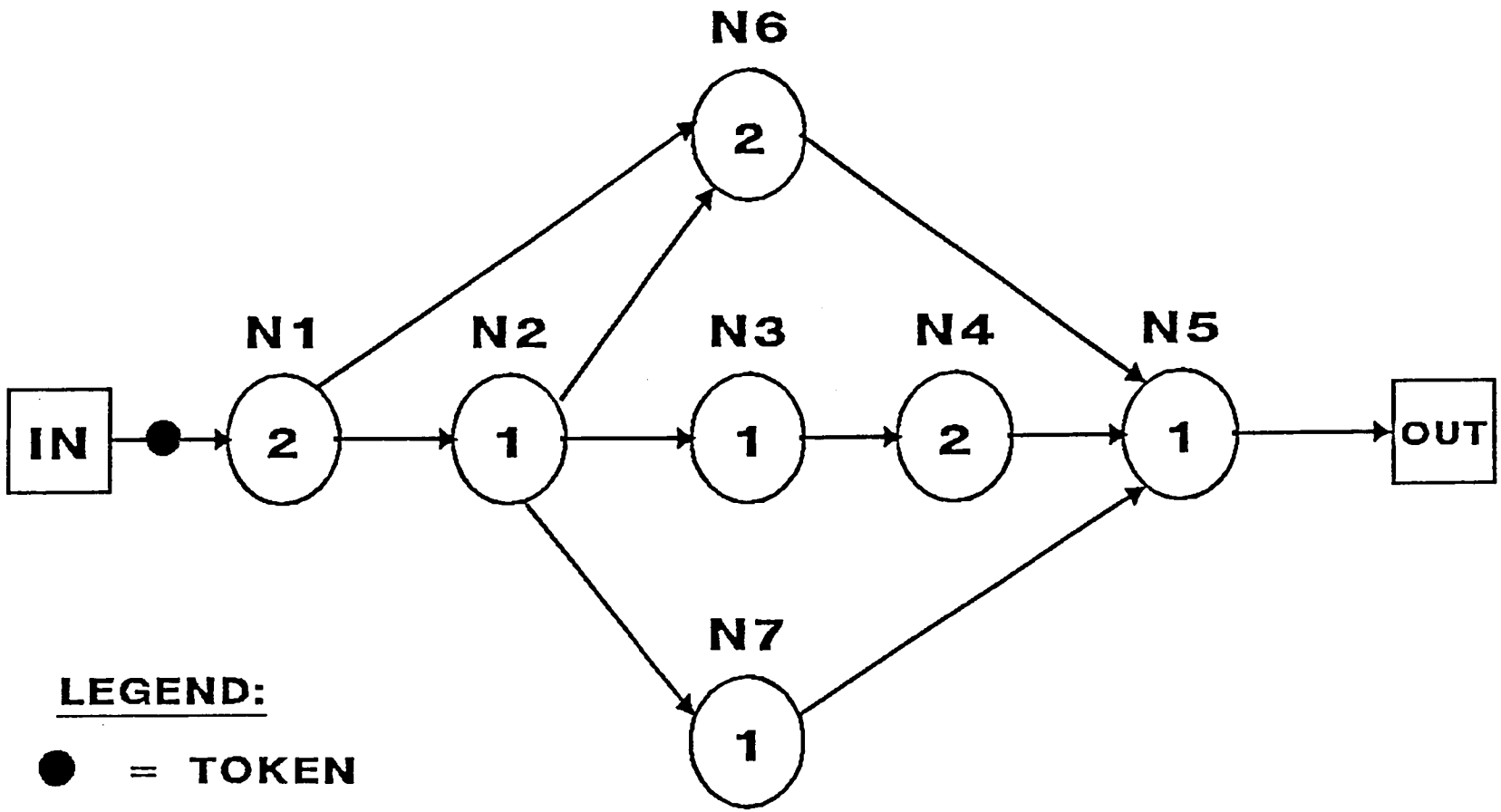
  A) DATA DRIVEN - EVENT FLAG
  - SEMAPHORE (MULTIPLE EVENTS)
  - AND/OR LOGIC

  B) DEMAND DRIVEN - PERIODIC TIMER
  - ONE-SHOT TIMER
- BACKUP NODE ALLOCATION
- FAULTY PROCESSOR EXCLUSION, SELF TEST, REBOOT

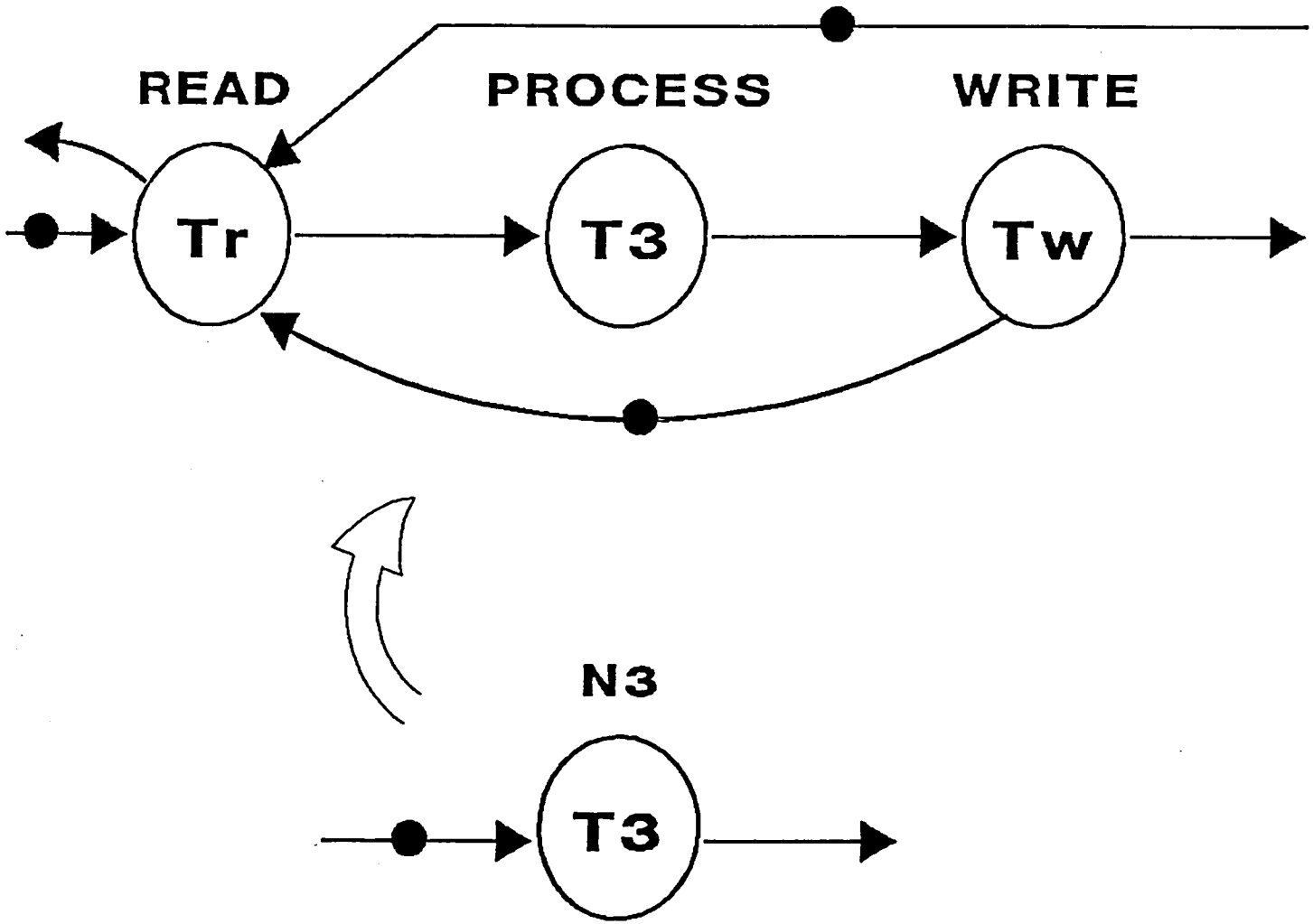
# ALGORITHM TO ARCHITECTURE MAPPING MODEL (ATAMM)

- A strategy for the real-time assignment of the nodes of a data-driven algorithm graph to parallel processors
- Based on Petri-Net marked graph theory
- Aimed at large-grain graph applications
- Provides:
  - deadlock-free performance
  - optimum time performance
  - operating system rules
  - performance prediction

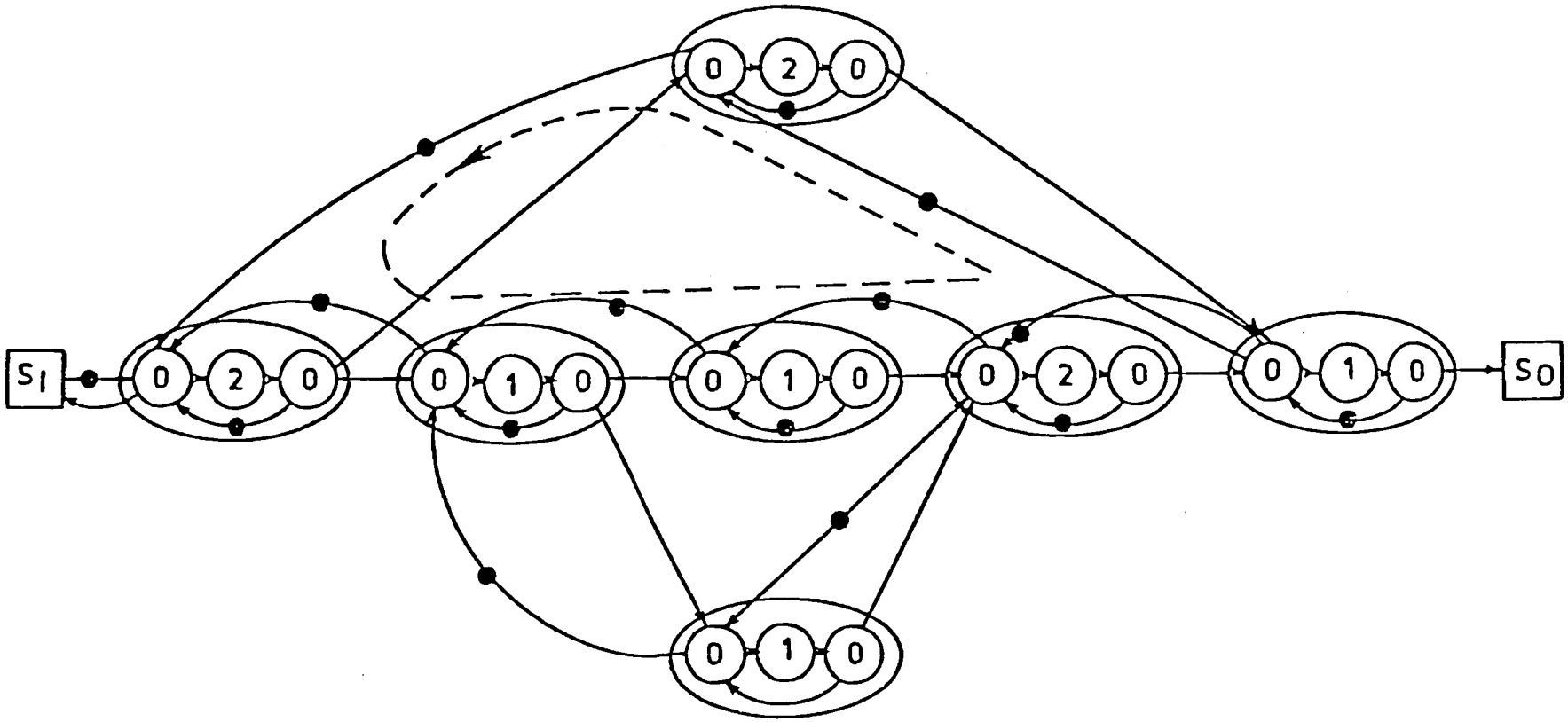
# ALGORITHM MARKED GRAPH (AMG) FOR 7-NODE EXAMPLE GRAPH



# NODE MARKED GRAPH (NMG) FOR DATA HANDLING



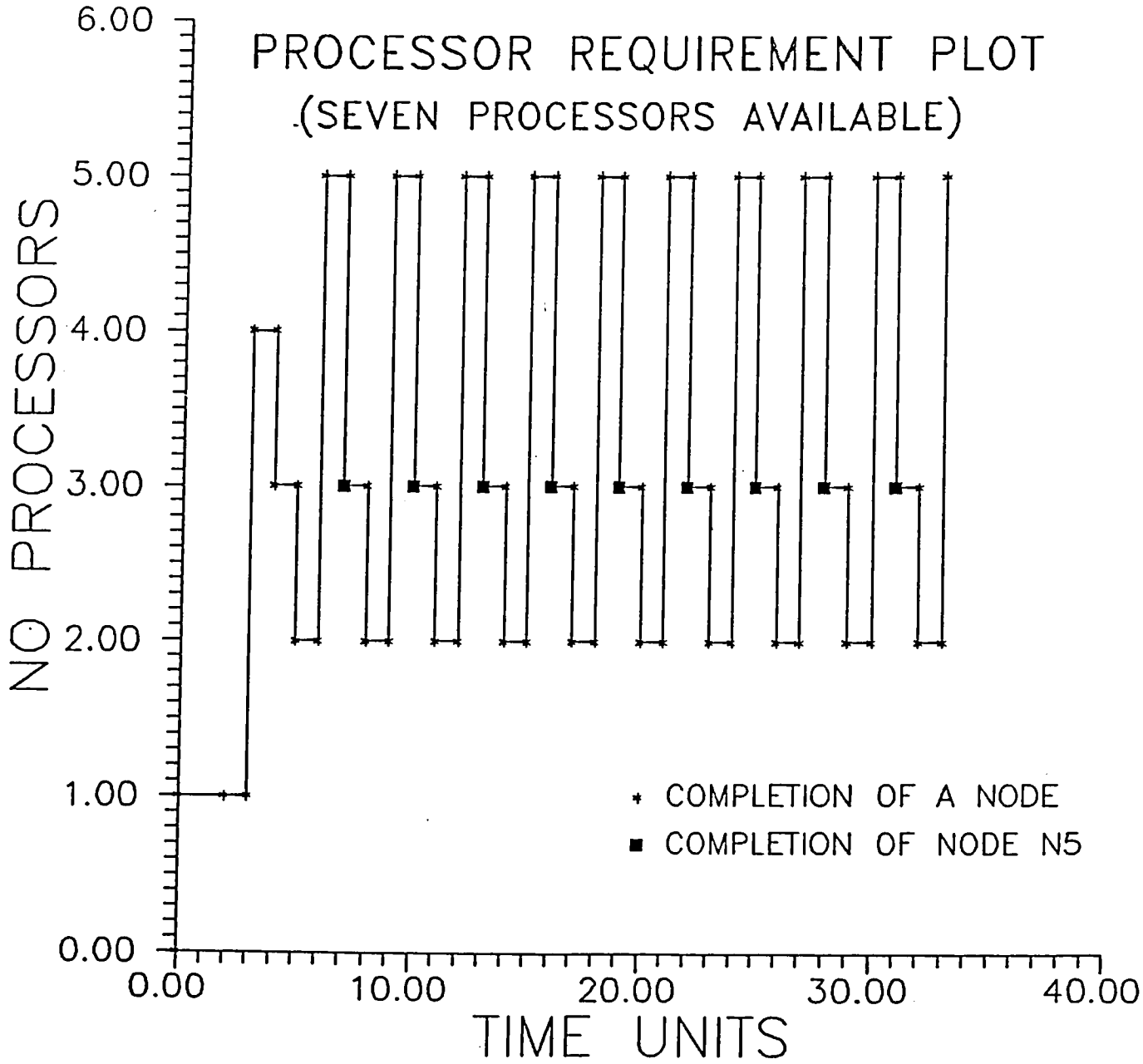
# GRAPH FOR ANALYSIS



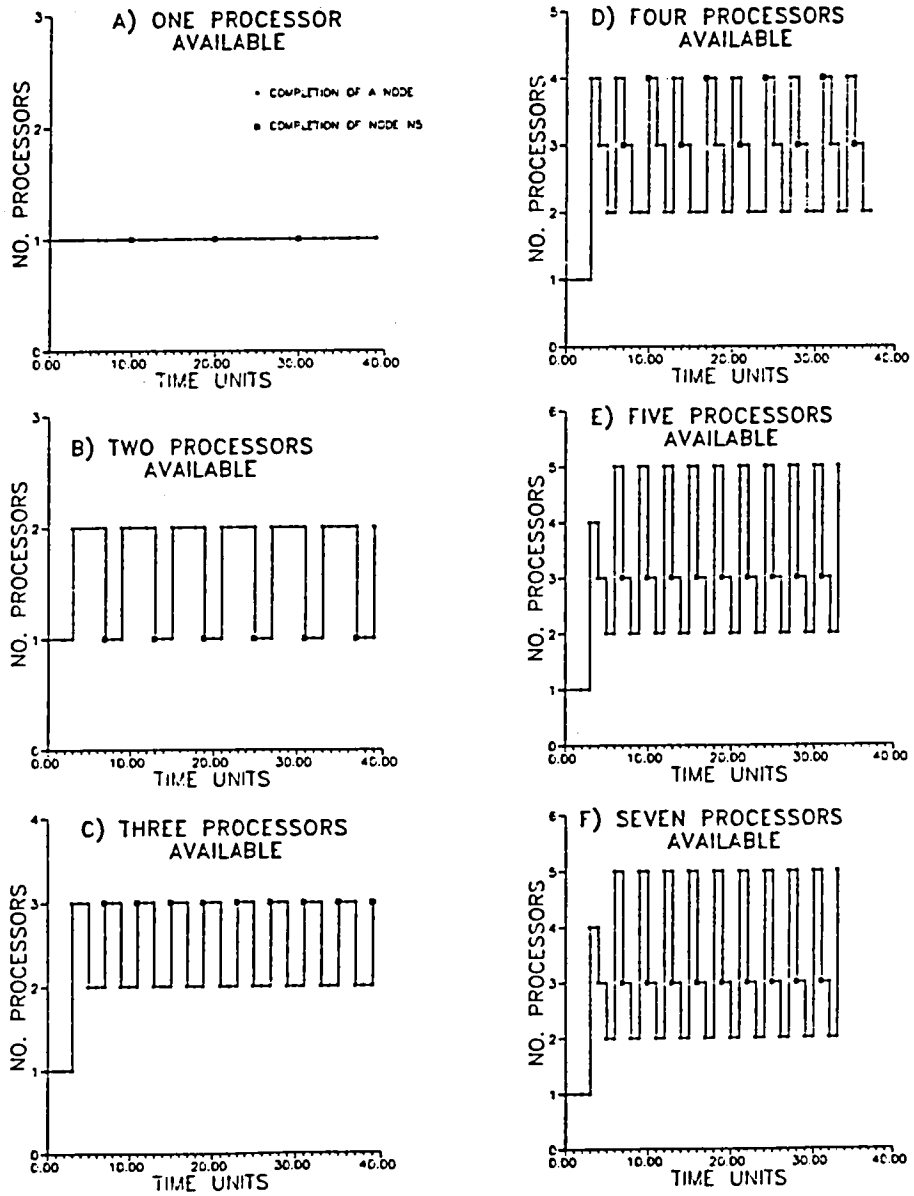

TBO = TIME BETWEEN SUCCESSIVE OUTPUTS

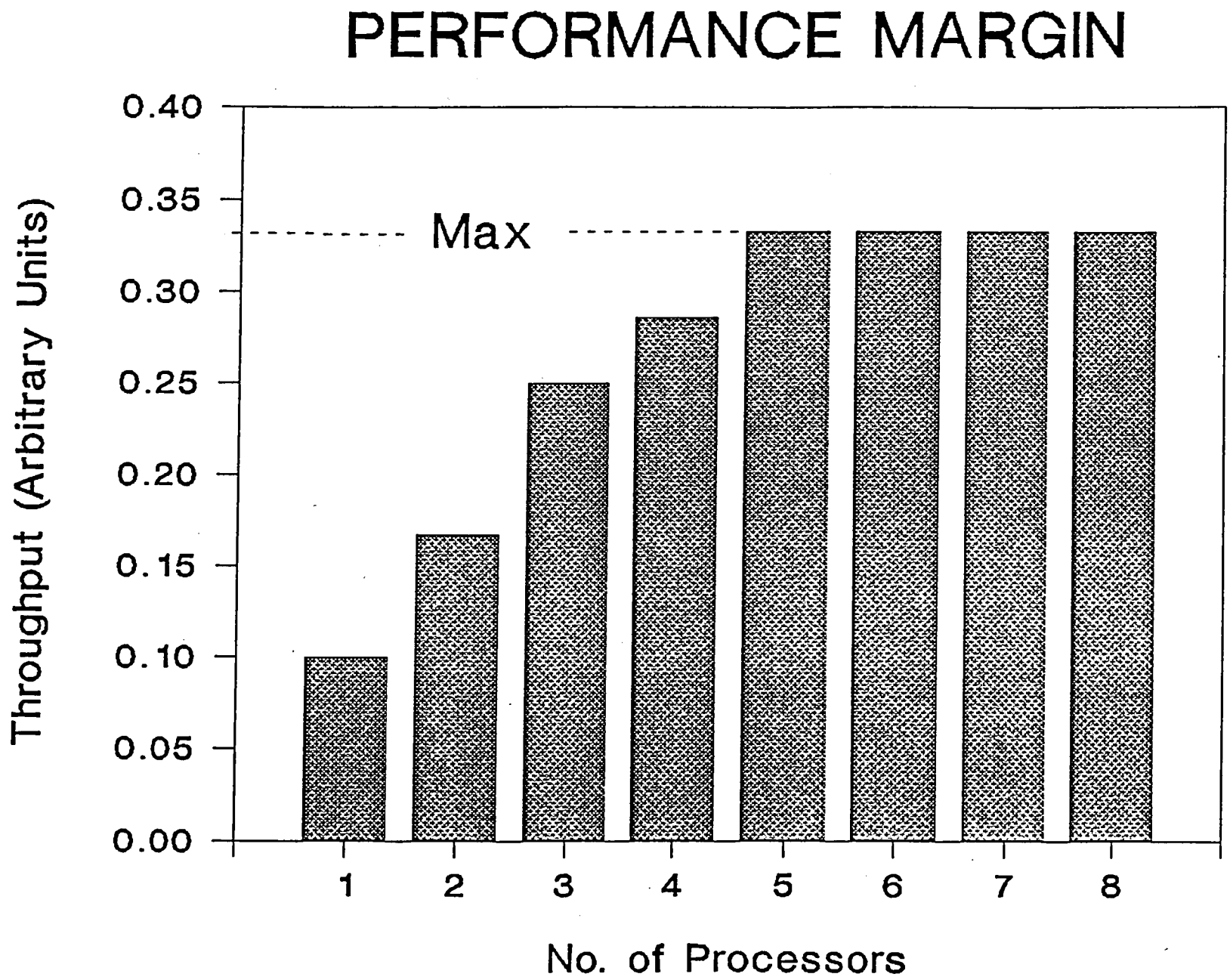
$TBO_M$ = MINIMUM VALUE FOR TBO

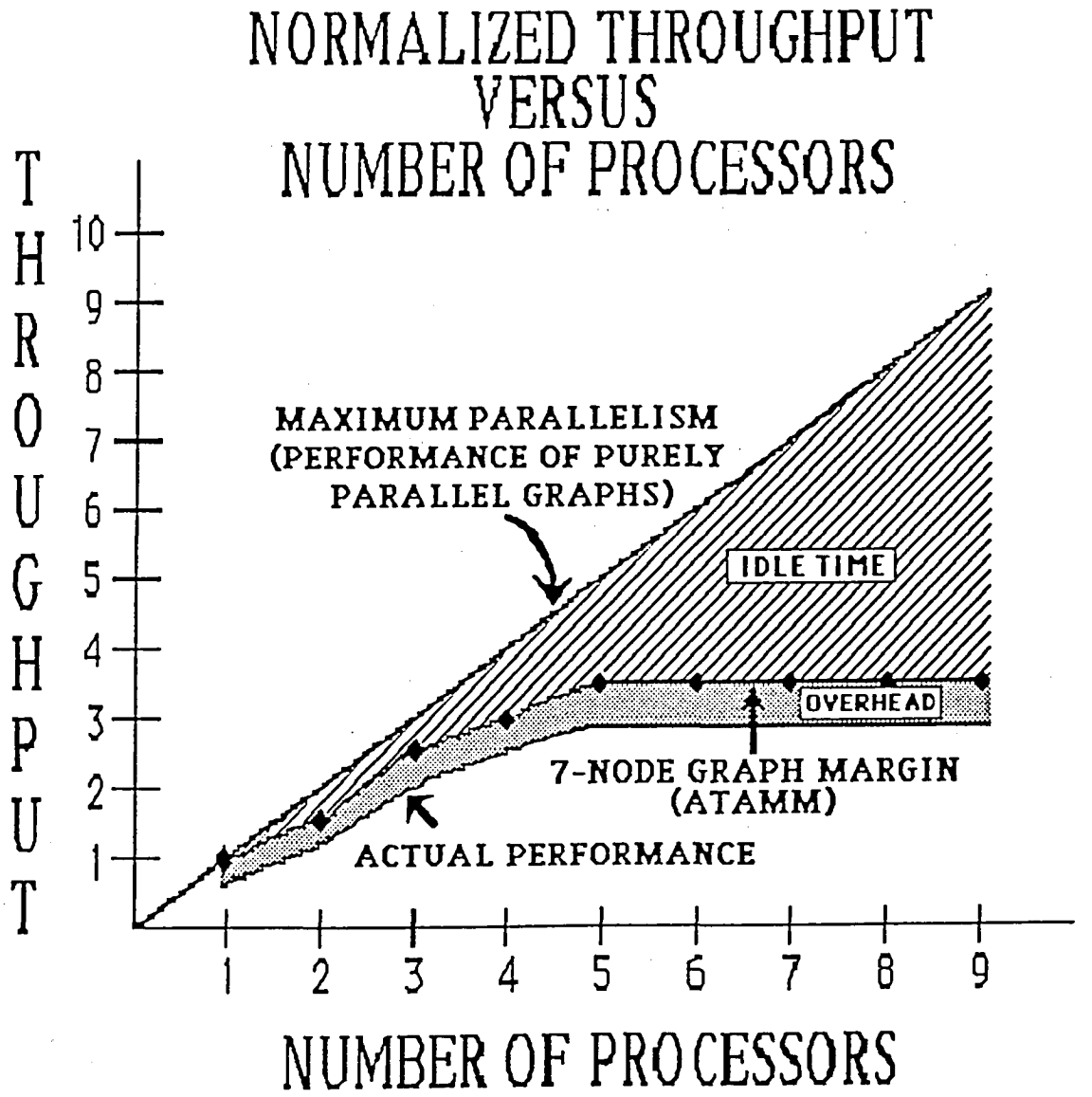
= MAX (TIME/NO. TOKENS)$_i$ = 6/2 = 3


PROCESSOR REQUIREMENT PLOT
(SEVEN PROCESSORS AVAILABLE)
NO PROCESSORS
6.00
5.00
4.00
3.00
2.00
1.00
0.00
0.00
10.00
20.00
30.00
40.00
TIME UNITS
COMPLETION OF A NODE
COMPLETION OF NODE N5

# PROCESSOR REQUIREMENT PLOTS




PERFORMANCE MARGIN
Throughput (Arbitrary Units)
0.40
0.35
0.30
0.25
0.20
0.15
0.10
0.05
0.00
Max
1
2
3
4
5
6
7
8
No. of Processors


NORMALIZED THROUGHPUT
VERSUS
NUMBER OF PROCESSORS
THROUGHPUT
10
9
8
7
6
5
4
3
2
1
MAXIMUM PARALLELISM
(PERFORMANCE OF PURELY
PARALLEL GRAPHS)
IDLE TIME
OVERHEAD
7-NODE GRAPH MARGIN
(ATAMM)
ACTUAL PERFORMANCE
1
2
3
4
5
6
7
8
9
NUMBER OF PROCESSORS

# ATAMM PROVIDES A NEW CAPABILITY SET

- Mathematically proven lock-free performance
- Operating system rules to manage the assignment of graph nodes to processors
- Prediction of graph's performance bounds
  - Maximum data rate
  - Maximum number of processors
  - Dependency of data rate on number of processors



C-3

# ATAMM DEVELOPMENT/DEMO PLANS

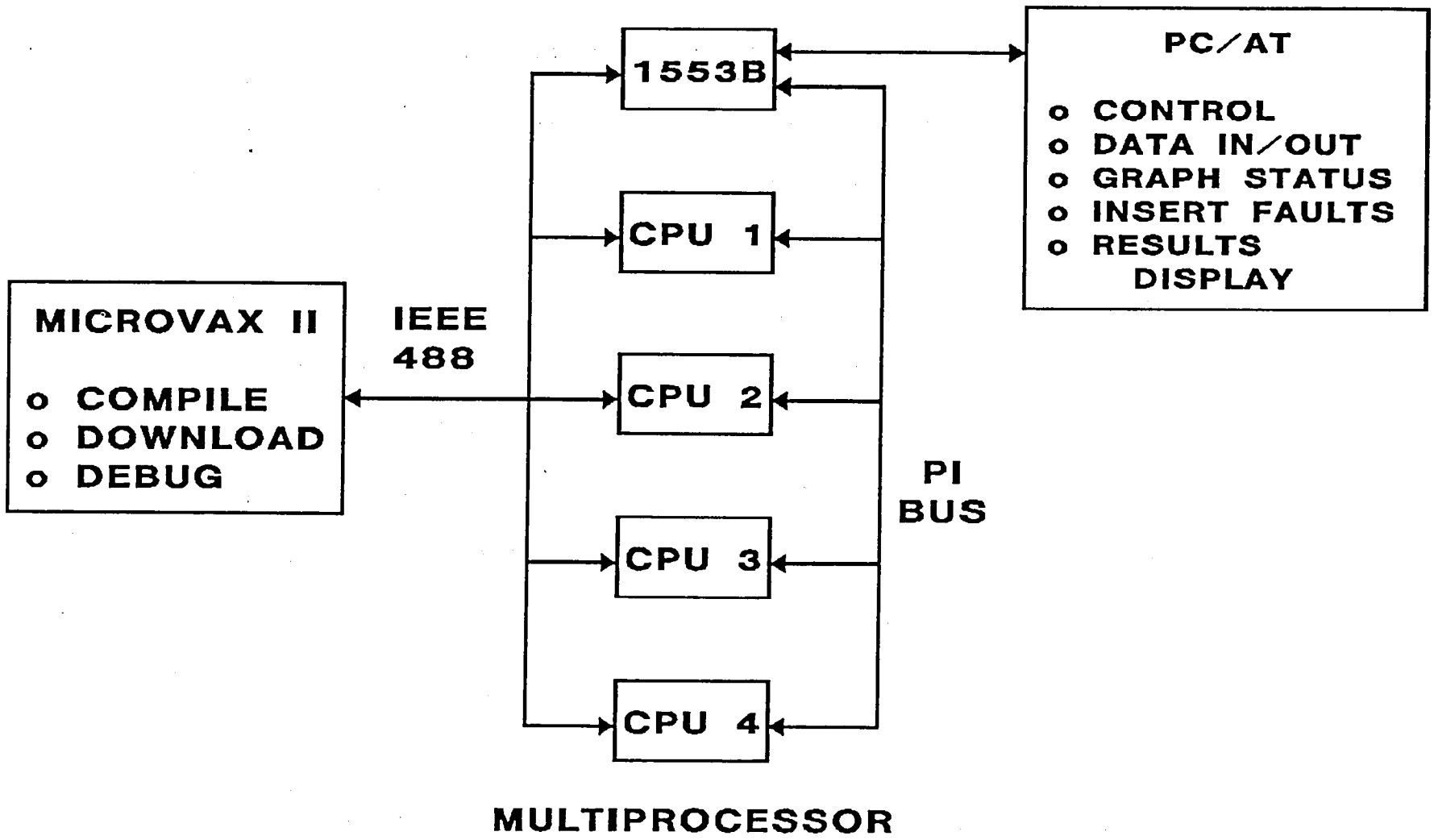
| STATUS | FEATURE | DEMO |
|---|---|---|
| Initial ATAMM | o Single graphs<br>o Simplex<br>o Identical processors (HW & SW) | ADM |
| Current Update | o Triple Modular Redundant (TMR)<br>o Graph optimization for specific no. processors | |
| Future Features | o Multiple graphs<br>o Multiple iterations of the same graph<br>o Multiple processor types<br>o Variable node-latency times | GVSC and/or RH-32 |

# MAJOR RESEARCH THRUST FOR FY90

- Implement ATAMM Rules into KOS
  - Simpler operating system than previous GMOS
  - Use Westinghouse Directed Graph Tool
  - Use 1553B to provide data I/O and monitor graph status
  - Improved version of Ada compiler
  - 2.5 MIPS VHSIC ADM 1750A processor

- Demo/Evaluate with Ada Algorithms
  - Test Algorithm (Scan-to-scan track correlation for SDIO)
  - Time-simulated graphs
  - Simplex/TMR
  - Fault injection and continued processing

# MULTIPROCESSOR INTERFACE DIAGRAM



## V1750A ADM Chassis/Module

- 1.25$\mu$ CMOS VHSIC
- $\mu$-Coded CPU Plus 256K RAM
- Surface-Mounted Devices; Dual Board Module
- 5.88 x 6.44 Inches (SEM-E)

# MAJOR PROGRAM MILESTONES

| | FY |
|---|---|
| 1) Integrate/Demo ATAMM and SDIO Algorithm on Avionics Advanced Development Model (ADM) | 90 |
| 2) Adapt/Demo ATAMM-Based OS on GVSC | 91 |
| 3) Expand ATAMM Capability and Adapt/Demo on RH-32 | 94 |