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DIFFUSED P^+-N SOLAR CELLS IN BULK GaAs*

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SUMMARY

Recently melt grown GaAs, made by liquid encapsulation techniques, has become available. This material is of sufficiently good quality to allow the fabrication of solar cells by direct diffusion. This talk will describe results obtained with p^+-n junction solar cells made by zinc diffusion, and will evaluate the quality of bulk GaAs for this application.

INTRODUCTION

Gallium arsenide solar cells are conventionally made by the epitaxial growth of a junction structure on a heavily doped substrate. This process has been necessitated by the poor quality of starting bulk material, which is highly defected. Recently, however, melt grown GaAs made by liquid encapsulated Czochralski (LEC) techniques combined with in-situ compounding, has become available (ref. 1,2). These materials are of sufficiently good quality to allow the fabrication of solar cells by direct diffusion.

This paper outlines results obtained with large area (0.5 cm^2) p^+-n junction solar cells formed in this way, using precisely controlled p^+-diffusions made by an open tube process.

EXPERIMENTAL

Tellurium-doped n-type gallium arsenide of (100) orientation and 5 - 8 x 10^{16} cm^{-3} concentration, made by the LEC process, was used for this study. Slices were cut into suitable pieces, and given a brief Caro's etch ($H_2SO_4 : H_2O_2 : H_2O$ = 10 : 1 : 1 by volume) before use.

The diffusion technique has been detailed previously (ref. 3), and will be summarized here. First, samples were placed on the platform of a resistance-heated susceptor in a cold wall reactor held at 350°C. A 1000 Å layer of ZnO-SiO_2 was

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deposited on the samples, by the simultaneous pyrolysis of diethylzinc $[(C_2H_5)_2Zn]$ and silane (SiH_4) in oxygen. This served as a doped oxide source for the subsequent diffusion step.[4]

Next, without removing the samples, a 2000 Å cap layer of P_2O_5-SiO_2 was grown over the doped oxide layer. This layer was also grown at 350°C by the simultaneous pyrolysis of phosphine (PH_3) and SiH_4 in oxygen.

Diffusions were made in an open tube furnace with flowing nitrogen gas, and at temperatures from 500°C to 600°C. Junction depths from 500 - 1000 Å were obtained in this manner. No PSG cap layer was used on the back face because of the low temperatures involved. However, the back face of the slices was subsequently etched to remove surface damage caused during diffusion. Ohmic contacts were made by evaporating 1000 Å of Au-Ge of eutectic composition (12% Ge by wt), and heat treating in a N_2/H_2 gas mixture of 450°C for 1 minute.

Solar cells of 0.5 cm^2 area, were made as follows: After diffusion, positive photoresist was applied to delineate a grid patterned cell, and buffered HF used to cut the underlying glass layers. The grid structure was then electrolytically plated in a gold bath. A second photoresist layer was applied to define a rectangular pattern and the uncovered oxide regions were etched in BHF. Next, a rectangular mesa was etched in the GaAs, using Caro's etch. The cell was coated with 800 Å of Sb_2O_3, after the removal of the remaining photoresist and glass layers. This film is easily deposited, and serves as an antireflective coating.

A number of small area cells of both the Schottky and p^+-n junction type were also made for diagnostic purposes. These were used to test the quality of starting materials and its stability to thermal processing.

The photoresponse of large area cells was measured in our laboratory at AM1 (simulated with an ELH source and a detector calibrated against a Bureau of Standards secondary standard). Some cells were measured by NASA at AMO as well. Finally, spectral response measurements were made on the large area devices.

RESULTS AND DISCUSSION

The Schottky devices, made on as-purchased GaAs, provided a baseline for the starting material. Schottky devices, on which the processing associated with the diffusion was simulated, provided information on the changes undergone by the GaAs due to this heat treatment. The short circuit current density for these cells, measured with no AR coating under simulated AM1 conditions, was found to be only slightly changed (from 13.1 - 13.6 mA/cm^2) after thermal processing at 600°C for 30 minutes under the PSG cap layer. Small area p^+-n cells, on the other hand, exhibited a consistently higher value of short circuit current (15.6 mA/cm^2). The reasons for this improvement, caused by the in-diffusion of zinc, are under investigation at the present time.

Table I shows the measured performance of a large area AR-coated cell made by this diffusion process. Both data at AM1 and AMO are provided for comparison purposes. As expected, the short circuit current density is 24% larger under AMO

conditions, but the fill factor and efficiency are essentially unchanged. Analysis of ℓn I vs. V characteristics has shown that the relatively low fill factor in these cells is caused by a high value of ideality factor ($n \simeq 1.6$) which was typical for p^+-n junctions in the LEC material.

Figure 1 shows the results of spectral response measurements on a large area cell, as well as a computer simulation based on a device with the following parameters:

Junction depth	= 1000 Å
Zero-bias depletion layer width	= 1000 Å
Surface recombination velocity	= 10^6 cm/sec
Hole diffusion length	= 1.4 µm

Experimental measurements of junction depth and hole diffusion length (ref. 4) agree well with those used in the model. Computer simulations have also indicated where device design and material properties must be altered (improved) in order to optimize this cell structure.

CONCLUSION

This work has demonstrated the feasibility of making large area solar cells in bulk GaAs, by a simple open tube diffusion process. A cell efficiency of 12.2% has been achieved for AMO conditions, even though no attempts have been made to optimize the cell design or the AR coating. Computer simulation has shown directions for obtaining improved cell performance. Further work, involving deep level transient spectroscopy, is in progress to understand the effects of zinc diffusion into gallium arsenide.

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TABLE 1: RESPONSE OF LARGE AREA GaAs SOLAR CELL

Conditions	J_{sc}(mA/cm^2)	V_{oc}(V)	FF	Efficiency (%)
AM1	19.1	0.894	0.75	12.6
AMO (NASA)	23.6	0.921	0.77	12.2

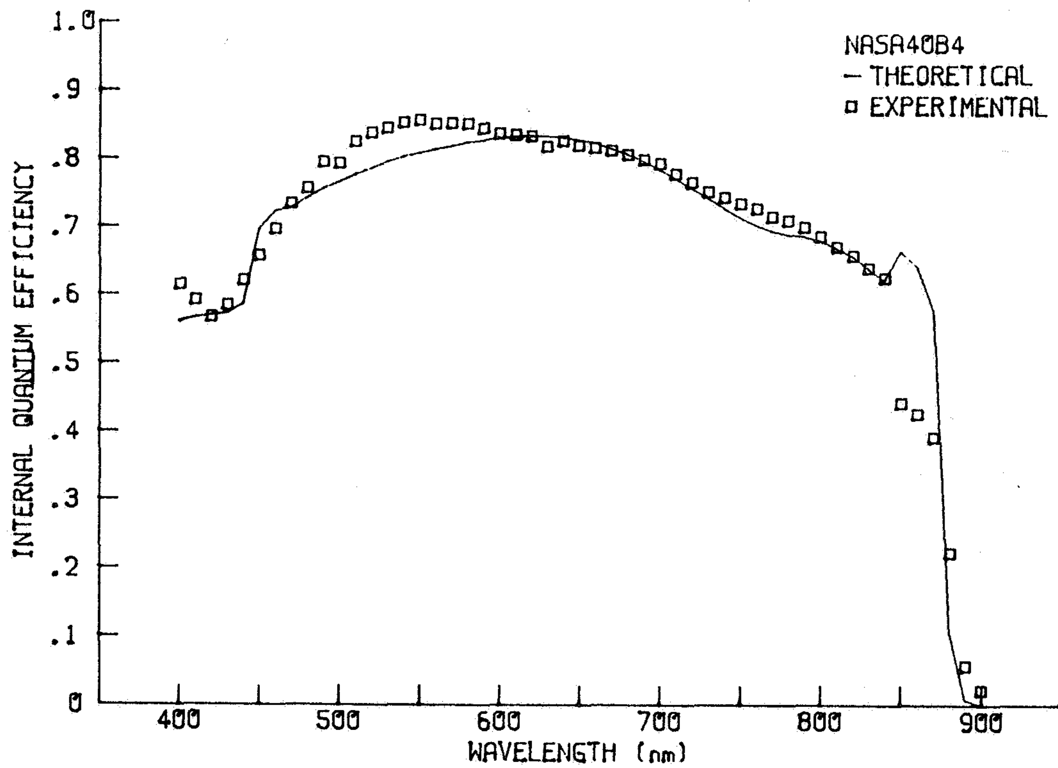

FIGURE 1

ADVANCES IN LARGE-DIAMETER LIQUID ENCAPSULATED CZOCHRALSKI GaAs*

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SUMMARY

We have evaluated the purity, crystalline perfection, and electrical properties of n- and p-type GaAs crystals grown by the liquid encapsulated Czochralski (LEC) technique. This study included the determination of the dislocation density, incidence of twinning, microstructure, background purity, mobility, and minority carrier diffusion length. The properties of the LEC GaAs crystals are generally comparable to, if not superior to those of small-diameter GaAs material grown by conventional bulk growth techniques. As a result, LEC GaAs is suitable for application to minority carrier devices requiring high-quality and large-area substrates.

INTRODUCTION

The availability of high quality, large-diameter GaAs substrates is the key to the successful development and production of high-speed GaAs integrated circuits and high efficiency minority carrier devices, such as solar cells. The liquid encapsulated Czochralski (LEC) technique (refs. 1-6) has provided a means for producing large-diameter GaAs with reproducible and thermally-stable semi-insulating properties suitable for GaAs integrated circuits and microwave devices. The purpose of this work was to further demonstrate the capability of the LEC growth technique to produce large-diameter, high-quality GaAs substrates suitable for minority carrier device applications. Attention was focused on materials properties relevant to minority carrier devices, including the dislocation density, incidence of twinning, microstructure, background impurities, mobility, and minority carrier diffusion length. We have evaluated these properties in n- and p-type 3-inch-diameter LEC GaAs crystals, and the results were compared with those from small-diameter GaAs crystals grown by conventional bulk growth techniques.

LEC CRYSTAL GROWTH

The doped and undoped, 3-inch diameter GaAs crystals used in this study were grown in a high pressure "Melbourn" (Metals Research Ltd.) puller using the LEC technique. The LEC growth configuration is shown in Figure 1. The crystals were grown in the $< 100 >$ direction from 6-inch-diameter quartz and pyrolytic boron nitride (PBN) crucibles. The GaAs melt was prepared by in-situ synthesis (ref. 1), starting with a charge of high purity (6-9's) Ga and As weighing 3 Kg. The crystals typically weighed from 2.2 to 2.4 Kg. The ambient pressure (Argon) during growth

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was typically 300 psi. The seed and crucible were both rotated counter-clockwise at 6 and 15 rpm, respectively. For n- or p-type doping, zone-refined Si, high purity (5-9's) Ga_2Se_3, or Zn_3As_2 was added to the charge. The resulting carrier densities ranged from 1×10^{15} to $1 \times 10^{19} cm^{-3}$.

The crystal diameter was controlled by adjusting the heater temperature and the cooling rate in response to changes in the differential weight signal obtained from the "load cell", a special weighing device on which the pull shaft was mounted. An increase or decrease of the differential weight indicated a corresponding expansion or contraction of the crystal. Growth was typically initiated by reducing the diameter of the crystal below that of the seed. This procedure is referred to as Dash-type seed necking (ref. 7). The diameter was then allowed to expand controllably, forming the "cone". Expansion was terminated at the "shoulder", and the diameter of the crystal was held constant for the remainder of the growth process, forming the "body".

Figure 2 shows a 3.6 Kg, 3-inch diameter, (100) LEC GaAs ingot grown at our laboratory illustrating the excellent diameter control ($\leqslant \pm$ 2mm) that can be achieved. Approximately 130, (100) wafers with a thickness of about 0.025 inch can be obtained from such an ingot.

CHARACTERIZATION METHODS

The crystals were evaluated in terms of crystalline perfection, electrical properties and purity. The wafers used for analysis were cut from the front, middle and tail of the crystals, then lapped and polished on both sides. Dislocation densities and distributions were evaluated by preferential etching (KOH for 25 min. at 400°C). This etch attacks dislocations intersecting the surface of the sample, forming hexagonal etch pits. The microstructures were examined by transmission electron microscopy (TEM). A chemical jet etching technique using $10HCl:1H_2O_2:1H_2O$ etching solution was applied to produce TEM foils with thicknesses less than 4000Å. The background impurities were determined by secondary ion mass spectrometry (SIMS). Carbon was determined by infrared localized vibrational mode (LVM) absorption measurement (ref. 8). The carrier concentration and mobility were determined by Hall effect measurement, and the minority carrier diffusion length by SEM-EBIC measurement (refs. 9-12).

RESULTS AND DISCUSSION

Reduction of Dislocation Density

A principal cause of dislocations in bulk GaAs crystals is stress induced by thermal gradients (refs. 13-16) during crystal growth. The relatively high dislocation density observed in large diameter ($>$ 2 inch) LEC GaAs has been a source of some concern in applying large-diameter material to minority carrier devices. In the present study, we have investigated optimum growth parameters to substantially reduce the dislocation density in 3-inch LEC GaAs crystals.

The distribution of dislocations across wafers exhibits four-fold symmetry indicative of the $< 100 >$ crystallographic orientation, as shown in figure 3. A microscopic view of the dislocation distribution, as shown in figure 4, clearly shows large variations in etch pit density (EPD). The main features of the distribution are: (1) minimum EPD occurs over a large annulus between the center and