HIGH TEMPERATURE LSI

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Summary

The General Electric Company has been involved in developing Integrated Injection Logic (I^2L)[1,2] tech ology for reliable operation under a -55°C to +300°C, temperature range. Experimental measurements indicate that an 80 mv signal swing is available at 300°C with 100 μA injection current per gate. In addition, modeling results predict how large gate fan-ins can decrease the maximum thermal operational limits. These operational limits and the long-term reliability factors associated with device metallizations are being evaluated via specialized test mask.

The correct functional operation of large scale integrated circuits in a -55°C to +300°C temperature environment for long periods of time will provide substantial immediate benefits for digital jet aircraft engine control and geothermal or deep fossil-fuel well logging. Most commercially available LSI technologies are inoperable or suffer long-term instabilities under these conditions.

Introduction

There is no inherent reason why silicon bipolar devices will not operate at +300°C for extended periods of time, provided the circuit has been properly designed to tolerate leakage currents in that environment. A calculation using extrapolated diffusion coefficients for aluminum in silicon (the worst-case dopant) at 500°C indicates that p-n junctions would not move appreciably in 1000 years. However, other contaminants such as gold or copper not commonly desired in unlimited quantities have diffusion coefficients at least ten orders of magnitude higher. In addition, the metal interconnection system on the chip's surface must provide good ohmic contact and resist the effects of electromigration. This paper will report on the effort at General Electric to develop reliable high-temperature integrated circuits. That work has been and is focused on both the design of silicon bipolar devices and the metallization system.

SILICON I^2L-DEVICE DESIGN CONSIDERATIONS

The operational limits of I^2L gates at high temperatures may be described by a variety of methods. Measurements of ring-oscillator propagation delays as a function of current and temperature provide a direct indication of the operating regions with unity fan-in but do not provide any information on noise margins.

A second method of determining I^2L operating limits enables an evaluation of the noise margin and signal swing. Two I^2L gates are connected in series with the first connected to a switch to provide a zero or one input (see Figure 1). Voltage measurements at the point between the gates are V_{BE} of the second gate's NPN transistor, with a zero input by the switch and V_{SAT} on the first gate collector with a one input.

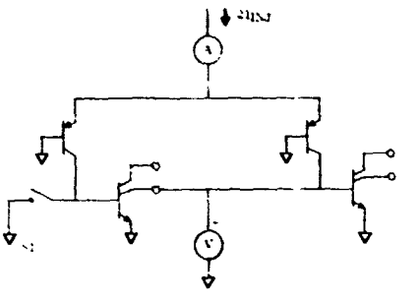

Figure 1. Measurement Method for Determining I^2L Voltage Swing.

Figure 2 plots the measured base-emitter forward-biased voltage drop for a gate input and the NPN collector saturation voltages for a gate output as a function of temperature. During operation, the PNP injection forward biases the NPN base-emitter junction and, with the collector conducting, a low (zero) logic level is supplied to the following stage. The collector sinks injection current intended for the following stage, bringing its input voltage down to the V_{SAT} level of the collector. This turns off the following stage, producing a high (one) output-logic level.

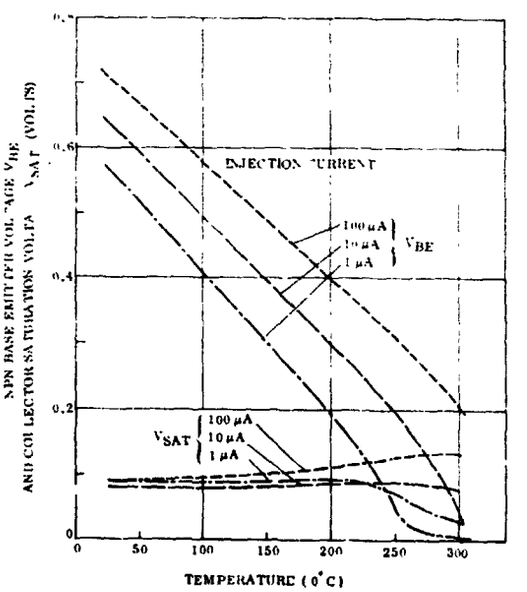

Figure 2. Measured NPN Base Emitter Voltage and Collector Saturation Voltage versus Temperature

The effect of the voltage-swing margin may be observed from the data presented in Figure 2. The V_{BE} for 100 μA injection current is about 550 mV at about 125°C and steadily decreases with rising temperatures to about 200 mV at +300°C. The V_{SAT} for a 100 μA injection increases to a 120 mV level at this same temperature, resulting in a voltage noise margin of 80 millivolts. The voltage noise margin may be obtained for the complete operating region from the difference between the voltages at similar injection currents.

Figure 2 indicates that signal amplitude and noise margin can be improved by increasing the injection-current density.

A third method of determining I^2L thermal operating regions is provided by the digital effective gain, which may be measured or calculated by computer modeling techniques. The effective gain is defined as

$$\beta_{eff} = \frac{\text{collector current sinking capability}}{\text{base current removed from gate input}} \quad (1).$$

I^2L logic signals will propagate as long as the digital effective gain is greater than one. The mechanism by which the effective digital gain decreases at high temperatures is through collector leakage. The total leakage currents in all the OR-tied collectors (fan-in) connected to a gate input rob that gate of some fraction of its injected base current and thus its collector-current sinking capability. This phenomenon is observed in Figure 3. As the fan-in is increased, the total collector leakage removes an appreciable fraction of the injected base current in the I^2L gate at lower temperatures. The effective gain is forced to less than one. This also imposes a design rule on the gate fan-in for a given gate to perform correct logical operations at some specified temperature and injection current.

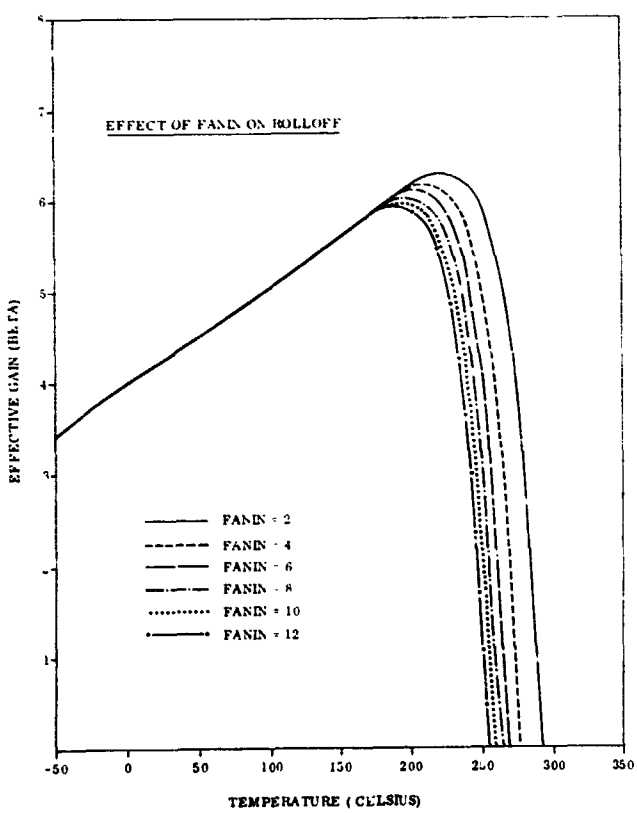

Figure 3. Modeled Temperature and Gate Fanin Influences on Effective Digital Gain

HIGH TEMPERATURE METALLIZATION

The production of a stable, highly-reliable metallization system is equal in importance to the silicon gate design in the production of high-temperature LSI. The metal system chosen for the high-temperature applications is platinum silicide/titanium-tungsten/gold.

Platinum silicide forms stable ohmic contacts to silicon, and gold was chosen for its ability to interface easily the chip to the outside world. However, unlimited gold diffusing into the silicon would seriously affect device performance, and silicon diffusing into the gold metallization can produce reliability problems due to the creation of voids. As a result, a thin titanium-tungsten barrier metal system is employed to separate those materials.

Verification of high reliability metallizations and silicon devices require accelerated aging to compress time scales to reasonable durations. Since most failure mechanisms in integrated circuits are temperature dependent, an activation energy may be obtained for the dominant failure modes. A reaction rate or failure rate may then be predicted at various other temperatures by the Arrhenius equation:

$$R = Ae^{-E/kT} \quad (2).$$

However, activation energies determined from high-temperature testing may be invalid if a phase change has occurred. This is a problem that provides considerable complications in producing high reliability circuits for 300°C operation; these circuits must be accelerated-life tested at temperatures above 350°C.

An independent test mask was designed for metallization evaluations. The mask consists of a repetition of the 190 × 186 mil master cell shown in Figure 4. The master cell is divided by scribe lanes into four separable chip types. Each chip, therefore, has an area of 95 × 93 mils. Within each chip are two different test element cells. Cells A1, A2, A3, A4, B1, B2, and B3 are metallization test elements. The final cell is an I^2L active test circuit.

The metallization test cells were designed to investigate the electromigration effect on the thin metal layer as a function of the metal linewidth and metal line spacing at elevated temperature. The electromigration effect could eventually cause metal-line runoff and resulting open circuits and short circuits between separated metal lines. The metal test elements were designed with a four-point probe capability to enable precise measurements to be made in order to detect effects of electromigration long before catastrophic failure.

The test elements were also designed in a manner that enables ohmic contact resistance to be accu-

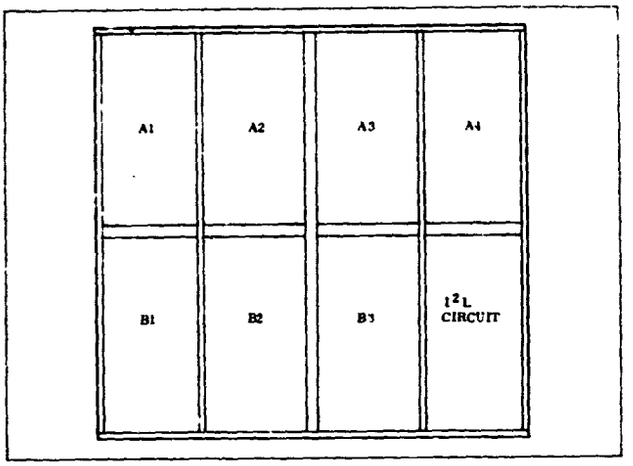

Figure 4. Master Cell Block Diagram

rately measured from external package leads, series resistance to be accurately measured while arbitrary current levels are passed through a metal thin-film conductor element, arbitrary voltage levels to be applied between adjacent metallization runs using external package leads, I^2L logic-gate digital gain to be measured from external package leads, and I^2L propagation delay to be externally measured using seven-stage ring oscillators. In addition, various gate sizes and styles were used in the ring oscillators to provide a convenient method of comparing the effects of different current densities.

Figure 5 shows a plot of a typical metallization test pattern. To cover the range of the current I^2L fabrication process, four different minimum dimensions were chosen: 0.2, 0.25, 0.3, and 0.4 mil. The metal stripe spacing was matched to the metal stripe width in each test element. The metallization test elements also investigate the effect of contact-hole size on the ohmic contact resistance for each type of doped region.

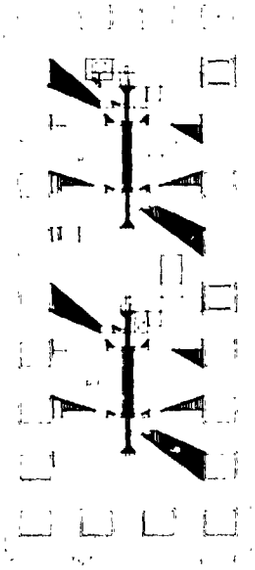

Figure 5. Plot of the Mask Pattern for a Typical Metallization Test Element

On each metallization test cell (from A1 to B3), the top and bottom four pads were used for ohmic contact studies. For reliability studies of the electromigration effect at elevated temperature, each of the two electromigration test vehicles contains three parallel metal stripes that are greater than 10 mils in length. The stress pull test on wire bonding can be done on the 8 mil × 8 mil enlarged metal pad near the center of the test chip.

Steps in the surface contour of a monolithic circuit are known to degrade the useful resolution capability of any given metallization system as well as to increase electromigration effects. To reveal possible problems, various combinations of these steps were intentionally designed into the metal test elements. Thus, seven test-element cells are devoted to the evaluation of conductor line-width, spacing, and ohmic contact resistance. Table I summarizes the permutations provided on the metal test cells.

TABLE I. METAL TEST CELL FEATURES

Cell Designation	Cell Features		
	Oxide Feature Under Four-Probe Electro-Migration Line	Contact Opening, Line Width, and Line Spacing (mils)	Contact Test
A1	p p	0.25 0.3	p p
A2	n n	0.25 0.3	n n
A3	pn -	0.25 0.25	np Schottky
A4	pn -	0.3 0.3	np Schottky
B1	pn -	0.4 0.4	np Schottky
B2	p n	0.4 0.4	p n
B3	n -	0.2 0.2	np p

Figure 6 shows a comparative photograph of the B3 metal test configuration along with the I^2L test cell. The test cell's purpose is to evaluate I^2L active circuits with the barrier metallization system. The I^2L circuits' test cell consists of the following components: a rectangular symmetrical gate cell and a slanted, symmetrical gate cell[3], each cell containing a dual output logic gate and a quad output logic gate; seven-stage ring oscillators using these basic gates; and a reduced geometry rectangular symmetrical gate seven-stage ring oscillator.

INITIAL EVALUATION RESULTS

Accelerated life tests are being carried out on the integrated-injection-logic ring oscillators. The oscillators were powered at 100 microamperes per gate during stress tests at 340°C. Out of 23 initial samples, one failure occurred at 24 hours, leaving 22 active devices. Of these remaining devices 6 have been under test for 580 hours, while the remaining 16 have been stressed for 247 hours. None of the has degraded.

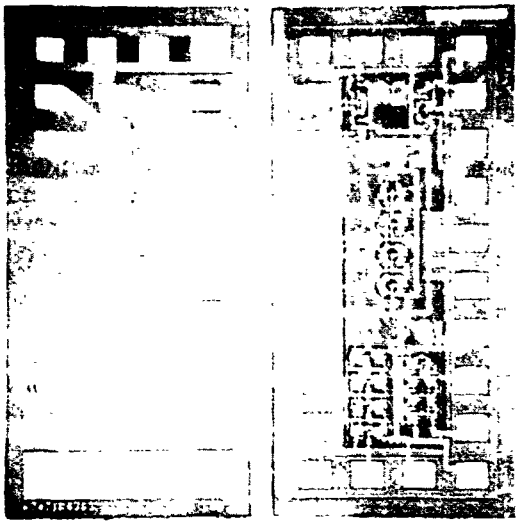

Figure 6. Photograph of the B3 Metallization Test Element and the Active I^2L Circuits

CONCLUSIONS

Integrated Injection Logic is a viable approach for large-scale integrated circuits that will tolerate 300°C. Silicon I^2L gate designs have been shown to be operable at these temperatures. In addition, a high-temperature barrier-metallization system has been chosen and an evaluation mask designed. Initial stress test results are encouraging, even though the metallization system has not been optimized.

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