SOLID STATE MICROELECTRONICS TOLERANT TO RADIATION AND HIGH TEMPERATURE

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Abstract

The nuclear and space industries require electronics with higher tolerance to radiation than that currently available. The recently developed 300°C electronics technology based on JFET thick film hybrids was tested up to 10^9 rad gamma (Si) and 10^{15} neutrons/cm^2. Circuits and individual components from this technology all survived this total dose although some devices required 1 hour of annealing at 200 or 300°C to regain functionality. This technology used with real time annealing should function to levels greater than 10^{10} rad gamma and 10^{16} n/cm^2.

Introduction

The need for high temperature electronics in many fields has been amply defined in the past.[1] Recent events suggest an urgently needed technology extension: temperature and radiation hardened microelectronics. The salient applications are nuclear reactor instrumentation and space probes. In particular, instrumentation within the containment structure of a nuclear power plant must be capable of withstanding a peak of 200°C and a total of 2×10^8 rad gamma dose during a 40-year plant lifetime followed by a loss of coolant accident. Additional temperature and radiation resistance is needed for monitors placed within the reactor vessel over the lifetime of the power plant: 325°C with 5×10^8 rad gamma and 10^{15}n/cm^2 near the vessel top and 350°C with 10^{10} rad gamma and 10^{16}n/cm^2 closer to the fuel assembly. Intense radiation belts near Jupiter and the Sun demand enhanced radiation tolerant electronics in certain extended space missions. Although critically dependent on orbit parameters, a dose of 10^7 rad over one year may be absorbed by a Jupiter satellite. Radiation levels elsewhere within the solar system and interstellar space are expected to be relatively low; however, the accumulated dose for long missions can easily exceed existing electronic tolerances.

Typical tolerances for present electronics are 2×10^6 rad gamma and 10^{12}n/cm^2 for commercial hybrids and ICs, and 10^6 rad gamma and 10^{14}n/cm^2 for specially fabricated or selected rad hard devices (Harris, for example). The numbers in Table I are somewhat arbitrary since different degrees of device parameter degradation are possible in different circuits.

Most radiation tests on electronics to date have been motivated by nuclear weapon applications. These tests therefore predominantly involve pulses of fast neutrons and X-rays, with a gamma dose that is only incidental to the neutron presence and usually less than 10^6 rad. Therefore, tests involving large gamma dose alone have not been common. Also because of the weapon orientation of most radiation-electronics tests, the interaction of operational temperature and sustained irradiation was not investigated. The recent development of circuitry operational to 300°C opens the possibility of real time annealing at high radiation levels.

Table I

Hardness / Technology	Gamma (rad Si)	Neutrons (cm^{-2})	Temp. (°C)
Consumer	2×10^4	10^{12}	85°C
Military Hardest	10^6	10^{14}	125°C
Thick Film/ JFET	$>10^9$	$>10^{15}$	>300°C

The components and hybrid circuits chosen for this initial investigation were from Sandia's high temperature circuitry development. There are two basic ideas behind this choice: first, to maximize the rate of annealing the operational temperature must be as high as possible, and secondly, several main failure modes are initiated both by elevated temperature and radiation (ion mobilization, lattice and chemical reactions).

We will discuss both gamma and neutron tests. Each section will briefly describe the radiation facility and the effects on passive components, active components, and hybrid microcircuits.

Gamma Tests

Two facilities for gamma irradiation were used. Both used Cobalt 60 (1.17 and 1.33MeV photons) with dose rates of 1.7 and 4.3Mrad (Si)/hr. respectively. Both sources generated enough heat to raise the sample temperature by about 15°C. Interactions between gamma photons and a steel liner between the weaker source and the sample chamber created some Compton electrons which also had measurable effects on the devices.

Passive

Passive components were tested in the weaker source with no biasing during irradiation. At 5 points during exposure, the samples were removed, tested, and returned for more radiation. The components were exposed for a total of 800 hours or 1.36×10^9 rad gamma (Si).

Thick film resistors in the 500 and 900 series of Cermalloy and axial lead units from Caddock were found to change less than 0.1% during this exposure. This constancy was somewhat surprising due to positive drifts seen in earlier tests[3] and attributed to Compton electron bombardment.

The high temperature capacitors tested were: Philips solid aluminum electrolyte, K&D Mica, Erie red cap, and several thick film dielectrics (TFS 1005, ESL 4515, ESL 4301, Cermalloy 905HT). Most capacitor systems tested remained functional throughout the test (ESL excepted) but all showed some change in capacitance and degradation in dissipation factor and insulation resistance (Figures 1 and 2). The best performers were the discrete mica and the 500°C thick film formulation 9015HT. The ESL thick film dielectric systems that showed considerable change and instability due to exposure were returned to near pretest parameters by a 1 hour bake at 300°C. Capacitance and dissipation factor were measured at 0.12, 1, and 10KHz. Insulation resistance was measured at 10 volts, with the reading being taken 15 seconds after voltage application.

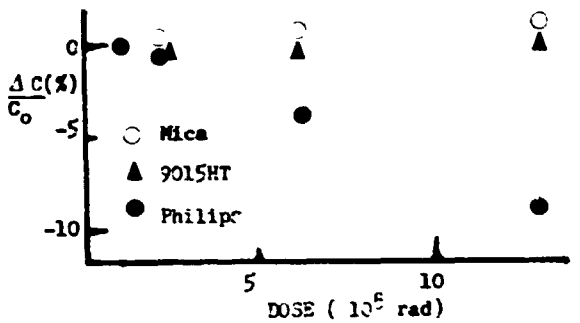

Fig 1. Capacitance Change with Gamma Dose

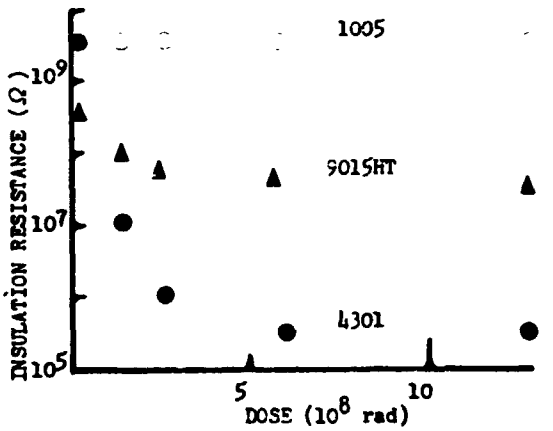

Fig 2. IR change with Gamma Dose

Active

To test the effects of gamma radiation on p-n junctions at various temperatures, 24 diodes were exposed at a dose rate of 4.3Mrad/hr. (Si) for 23 hours, yielding a total dose of ~1 x 10^8 rad (Si). The diodes were grouped into 3 modules, each containing 2 gallium phosphide, 2 gallium arsenide, 2 low minority carrier lifetime (gold doped) silicon, and 2 high lifetime silicon diodes. The thick film hybrid modules were then heated to 50, 175, and 300°C respectively. During most of the test one of each type of diode at each temperature was AC biased. Each diode was monitored periodically for reverse leakage current, forward resistance, reverse breakdown voltage and sharpness of reverse breakdown.

In general radiation effects were minimal. Measured photocurrents were negligible (<16μA/cm²) for all devics. AC biasing had no measurable effect on diode performance over the span of the test. Low lifetime diodes (GaAs, GaP, and gold doped Si) displayed little or no change in characteristics over the 23 hour test; however, the high lifetime silicon diode reverse leakage current increased appreciably. This effect was, presumably, caused by degradation of minority carrier lifetime (increase in generation rate) due to lattice imperfections created by gamma/silicon interactions. A control group of identical high lifetime silicon diodes aged for 24 hours at 300°C without radiation was found not to show this increase in leakage current, indicating that the effect was not caused by junction poisoning due to unwanted diffusion at elevated temperature.[4]

In another experiment, several types of n-channel silicon JFETs (Motorola 2N4220 and 2N4391 series) were exposed at room temperature to a gamma dose rate of ~1.7Mrad/hr. (Si) up to 1.36 x 10^9 rad (Si) total dose. The transconductance and I_{DSS} vs. accumulated dose for a typical transistor are plotted in Figure 3. Cutoff voltage, $V_{GS\ off}$, remained essentially constant for all transistors during the test, indicating that carrier removal effects were minimal. However, transconductance (and I_{DSS}) decreased monotonically for all devices, an effect most likely due to a reduction of carrier mobility in the channel. Both gamma photons and Compton electrons could have created the lattice damage necessary for this phenomenon to occur.

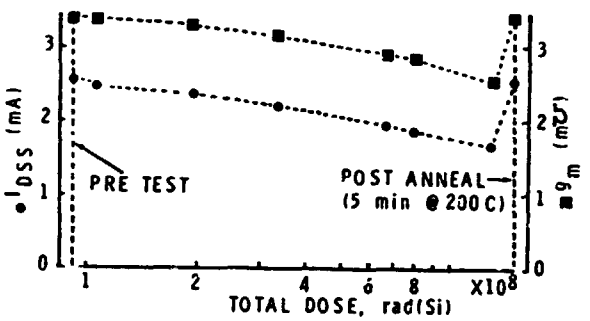

Figure 3. Motorola 2N4220A JFET Parameters vs. Total Dose

Because of the layout of the gamma test facility used in this JFET experiment, it was impossible to study the simultaneous effects of radiation and elevated temperature. Instead, the devices were annealed for 5 minutes at 200°C after a total dose of 1.36×10^9 rad was reached. As Figure 3 shows, 100% recovery was obtained with respect to g_m and I_{DSS}. This indicates that extremely high total doses (>10^{10} rad) may be tolerated by JFETs if accompanied by moderate heating, as expected in a loss of coolant accident. It should be noted that devices held below 30°C for several weeks after irradiation showed no annealing.

Hybrid

Tests were also performed on a simple hybrid microcircuit containing 6 JFETs and 3 thick film 500-series Cermalloy resistors. Circuit performance did not change throughout the test (1.36×10^9 rad total). The same technology used for this circuit is employed in the complete line of Sandia's geothermal high temperature instrumentation, including voltage regulators, V/F converters, pulse stretchers, and multiplexers.[5]

Neutrons

The neutron tests have not been concluded as of this writing. A pulsed reactor with a fast neutron product was used. The pulse is about 70μsec long and exposes the samples to approximately 3×10^{14}n/cm² during each pulse. This source also produces sample irradiation of 6×10^5 rad gamma for each 10^{14}n/cm².

Passive

Initial exposures of 7×10^{13}n/cm² were used in order to induce only a small change in passive component parameters. As in the case of gamma tests, the resistors remained stable. This is in agreement with previously reported investigations.[3] Although several capacitors showed slight changes in dissipation factor due to this neutron flux, they were all circuit functional. The extreme tolerance of these components suggested an ongoing test series which will reach 10^{17}n/cm². As with gamma tests the source time and cost may eventually necessitate extrapolation to higher expo ures.

Active

To study the effects of neutron irradiation and thermal annealing on diode reverse leakage current, several silicon diodes (all TRW SA1813) were exposed to 10^{14}n/cm². The results of thermal annealing runs on one particular (but typical) diode are shown in Figure 4. Unfortunately, pre-irradiation data was not available for these early tests, but measurements made on a non-irradiated control group yielded 25°C leakage currents ranging from 5.5 to 11nA at -10 volts, with most values in the 6 to 8nA range. As can be seen, recovery of the reverse characteristics is initially rapid but not complete. Similar effects were noted for JFETs. The higher temperatures within the reactor vessel (the only anticipated application where significant neutron fluences would be encountered) may improve annealing.

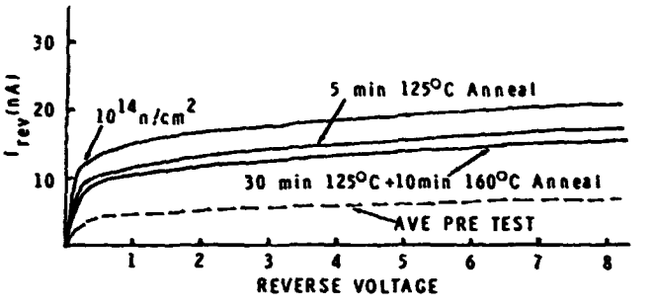

Figure 4. Diode Neutron Irradiation/ Thermal Annealing Behavior

An interesting and, as yet, unexplained phenomenon was discovered in another phase of this experiment. While attempting to anneal the neutron damage by injecting forward current across the p-n junction, it was found that short applications (~1 minute or less) actually caused an increase in reverse leakage current. This increase could, in turn, be annealed by subsequent heat treatment. Non-irradiated parts did not exhibit this effect, and currents applied for much longer times initiated thermal annealing. While the exact mechanism behind this behavior is not certain, it is thought that charge trapping in gamma induced states in the passivation layer near the edge of the junction may play an important role. (As mentioned previously, the neutron facility also has a significant gamma output.) If this is the case, a similar effect should be noted on gamma irradiated devices. This experiment is still in the planning stage.

Neutron effects on JFETs used extensively in Sandia's high temperature circuits (Motorola 2N4220 and 2N4391 series) were examined in another set of experiments in which the devices were irradiated to a level of ~7×10^{13}n/cm². As can be seen in Table II drastic changes occurred in transistor characteristics. In most cases the magnitude of $V_{GS,off}$ increased markedly (average ~8%), indicating carrier removal effects were occuring. Transconductance and I_{DSS} decreased by more than an order of magnitude. Partial annealing was obtained after 1.5 minutes at 200°C, with only slightly greater annealing effected at 300°C. The relatively slow recovery confirms the fact that, unlike the simple defects created by γ photons and Compton electrons, neutron damage is additionally composed of more stable cluster defects. It is interesting to note that, at each temperature used in the annealing experiments, recovery was extremely slow after 2 minutes; even when the device was held at temperature for periods of up to an hour, no further improvement was evident. An increase in temperature was required to effect further annealing. While operation at high temperature may provide the simultaneous annealing necessary for operation in high neutron fluence environments, it is doubtful that JFET operation will survive levels much above 10^{16}n/cm².

Table II

	$V_{gs,off}$	g_m (m℧) @V_{gs} = -0.2	I_{dss} (mA)
PRE TEST	1.15	2.00	1.160
$7X10^{14}$ n/cm^2	1.24	0.20	0.073
ANNEAL: 1.5 min@200°C	(1.36)	0.80	0.360
ANNEAL: 11.5 min@200°C	1.15	0.84	0.362
ANNEAL: 11.5 min@200°C +10 min @300°C	1.13	1.08	0.439
ANNEAL: 11.5 min@200°C +80 min@300°C	1.14	1.04	0.488

Motorola 2N4220 JFET Parameters

Hybrid

The same hybrid circuit which saw 1.3 x 10^9 rad gamma was exposed to 7 x 10^{14}n/cm^2. After a 5 minute. 200°C post exposure anneal the circuit functioned normally.

Summary

It is clear from these initial tests that the traditional limits ascribed to solid state electronics in radiation environments can be vastly exceeded. For example, the thick film/JFET technology with no modifications to its high temperature form can survive more than 10^9 rad (Si). The quick annealing of passive and active devices at 200°C strongly suggests that operation to 10^{10} rad is possible, a level exceeding any application now envisioned. Annealing effects seen in diodes and passive components after neutron exposure also demonstrate the enhanced radiation tolerance possible by high temperature operation. The JFET response to neutrons defines the extent of radiation possible with this hybrid technology. Additional tests with high temperature operation during irradiation up to 10^{17}n/cm^2 are necessary before the circuitry tolerance to neutron flux can be ascertained. This limit is projected as well above 10^{15}n/cm^2, however.

This investigation is only the first step toward ultra high rad electronics. Several programs must follow. For example, the development of JFET ICs will allow increased complexity and reliability. During the next year, hybrid prototypes of a control rod position sensor and a containment vessel pressure monitor will be fabricated and tested to the appropriate radiation level. Device tests will be expanded to include bipolar transistors, op amps, I^2L microprocessors, and MOS structures.

Although this thick film/JFET technology appears suitable for reactor instrumentation in both the containment and reactor vessels, power and volume restrictions on space probes may demand the CMOS technology which is now used for similar reasons in weapons.

Analysis by other researchers has indicated that CMOS should not necessarily be discarded for use in extremely high radiation environments, as long as elevated temperature provides some annealing of the trapped charge in the oxide.[6,7] Detailed experiments along these lines are planned for the near future. Although the CMOS technology has not been addressed in this report nor extensively tested at these high radiation levels, it is important to note that at least two solid state microelectronics options exist which have capability to the highest radiation levels expected for nuclear reactor and space needs.

Acknowledgements

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