RELIABILITY STUDY OF REFRACTORY GATE GALLIUM ARSENIDE MESFETS*

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Summary

Refractory gate MESFETs have been fabricated as an alternative to aluminum gate devices, which have been found to be unreliable as RF power amplifiers. The reliability of the new structures has not yet been determined, and this work was undertaken to provide statistics of failure and information about mechanisms of failure in refractory gate MESFETs. Test transistors were stressed under conditions of high temperature and forward gate current to enhance failure; results of work at 150 °C and 275 °C are reported here.

Introduction

Until recently, the semiconductor industry metal standard for MESFET fabrication was aluminum, particularly for the gate. The reliability of aluminum metallized MESFETs has been extensively studied,[1-10] and certain failure mechanisms have been identified, all involving the aluminum gate metallization. The most important of these are aluminum electromigration and gold-aluminum phase formation. The failure problem in aluminum metallized power MESFETs has become so acute that the aluminum gate is being abandoned, and a refractory gate is being introduced in its place. This gate consists of a refractory metal Schottky contact and a conducting gold metallization, separated by some intermediate metal to provide metallurgical stability; the most common refractory gate is titanium-platinum-gold. The reliability of refractory gate MESFETs has been assumed to be better than that of aluminum gate MESFETs. However, electromigration has been observed in gold[11-12] and in titanium-gold[13-14] films, and failure modes in refractory gate devices similar to those in aluminum gate devices are possible. This work was undertaken to obtain statistics on failure for and to determine failure modes of refractory gate MESFETs.

Experimental Procedure

The MESFET used in this work is the Texas Instruments MS801 gallium arsenide transistor in the stripline package. Each packaged chip consists of two individual cells, each cell delivering 250 mW of microwave power at 8 GHz; only one of the cells is used in the MS801. Normally, the chip is sealed in epoxy for protection; however, the epoxy fails near 200 °C, so that the devices tested here were unencapsulated to permit measurements at higher temperatures. Source and drain ohmic contacts are formed by evaporating a gold-germanium-nickel layer over the entire contact region and alloying, evaporating titanium-gold or chrome-gold, then gold-plating the source and drain pad regions. The source-drain separation is 6 μm; four central gate stripes, 2 μm by .006 inch, are connected in parallel at the gate pad. The gate stripes and pad are formed by electron beam evaporating successive layers of titanium (the Schottky contact), platinum and gold.

The test fixture is made from a nickel-clad high temperature laminate; contact is made between a high temperature PC board connector and the device leads by way of striplines patterned in the nickel. The connectors accomodate two fixtures side-by-side; a stainless steel tray holds fourteen connectors, so that up to twenty-eight devices can be stressed simultaneously. The temperature test chamber is a 315 °C inert gas oven configured for nitrogen flow. A three inch diameter feedthrough port, capped with a PTFE feedthrough, completes the test chamber arrangement. A thermocouple measures the temperature at the geometric center of the tray at sample height.

The devices were stressed electrically at two channel temperatures, 150 °C and 275 °C. Electrical stress consisted of biasing each device near I_{dss} and driving the gate into forward condition, in some cases, quite heavily. The devices could not be biased at the same values of I_{dss}, and simultaneously at the same drain-source voltages, because of their different characteristics; in order to maintain equal DC channel power dissipation, and equal channel temperatures for all devices during stress, the device with the lowest I_{dss} curve ($V_{gs} = 0$) was biased at the intersection of the load line and the I_{dss} curve and the other devices (at the same chamber temperature) were biased at a drain current equal to that value of I_{dss}. For equal load lines, all devices then were biased at the same quiescent value of V_{ds}. Although the other devices were biased below their I_{dss} values, forward gate current flowed for sufficient positive gate-source voltage swing. The gate-source voltage swings were set to provide equal drain-source voltage swings, in order to obtain the same AC channel power dissipation.

The output resistance of the MESFET becomes negative at certain values of the drain current and drain-source voltage. If the load line passes through a region of device negative resistance, there is a considerable possibility of oscillation, so that the drain resistance must be such as to limit operation to a safe region, that is, to a region of positive output resistance. The safe value of the drain resistance is obtained by drawing a load line which begins at the drain bias voltage on the V_{ds} axis and which crosses the I_{dss} curve at its corner, just below the point at which the output resistance becomes negative. This value is, of course, different for different devices, and even for a single device at various temperatures. I_{dss} decreases with increasing temperature; for a given transistor, a drain resistor will have its highest safe value at the highest test temperature. If that highest value is chosen as the drain load, the load line will be safe at all lower temperatures. Furthermore, if that safe value is calculated on the basis of the lowest I_{dss} curve cut of the entire set of transistors, that value will assure a safe load line for every device in the set, at any temperature below the maximum test temperature. (This assumes that all devices exhibit roughly the same percentage decrease in I_{dss} with increasing temperature; the assumption was validated by comparing the behavior of several devices.) If the same load resistance is used for every test device, each MESFET can be biased to the same quiescent point, and driven with identical AC swings. The average drain power dissipated is the

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same for each device, so that power (of channel temperature) is the same; however, if the gate of each device is driven into forward conduction, the forward current drawn by each gate is different for equal drain current swings (for different I_{dss} values). The statistically significant stress is then the forward gate current.

The gate voltage was varied around its quiescent point, so that forward current flowed only during part of the AC cycle. Very low reverse gate currents flowed when the drain current was below I_{dss}, that is, for negative gate-source swings, so that a roughly half-wave rectified forward gate current was obtained; true sinusoidal behavior could not be obtained because of the non-linearity of the diode curve. The high temperature stress was interrupted at logarithmic time intervals and the devices were cooled down to room temperature for failure characterization. The stress periods were nominally 20, 50, 100, 200, 500, and 1000 hours.

Electrical Measurements

Five measurements were originally planned for high temperature characterization and failure analysis: the characteristic curves, from which the transconductance, g_m, could be obtained; the pinch-off voltage, V_{po}; an I_{dss} *vs.* V_{ds} curve; the gate-source reverse leakage current (drain-source short), I_{rgss}; the forward gate-source current-voltage characteristics (drain-source short), I_{fgss}; and the zero bias gate-source capacitance (drain-source short), C_{gss}. The capacitance measurement could not be performed because of the very high parasitics associated with the test assembly. The gate leakage current measurements were not made at elevated temperatures, inasmuch as the very high reverse gate-source currents made these measurements impractical. The time required to make a complete series of measurements at high temperatures for the total number of devices involved was long enough to be comparable to the stress periods between room temperature measurement; elimination of the reverse leakage measurement, which is primarily of value as a room temperature failure criterion, reduced the total high temperature measurement time significantly. In order to reduce the time even more, high resolution pinch-off voltage measurements were not made at elevated temperatures; that is, V_{po} could be estimated from the high temperature characteristic curves, but no special measurement was made. The pinch-off voltage, like the gate-source reverse leakage, is a useful room temperature failure criterion. However, the characteristic curves, I_{dss}, and I_{fgss}, can be related theoretically to temperature; these measurements were performed for every device at high temperature. The forward gate-source current measurements are particularly important, inasmuch as they provide the n-factors and saturation currents (and barrier heights) for the gate Schottky diodes. Characterization of the devices was performed initially at room temperature and each time the devices were cooled back to room temperature (nominally at 20, 50, 100, 200, 500, and 1000 hours) after a high temperature stress. High temperature measurements were made after the oven temperature had stabilized at its high temperature value, just before the oven power was turned off to cool the devices, and at daily intervals in between.

Results and Discussion

I_{dss} *vs.* V_{ds} curves were obtained and provided values of I_{dss} at V_{ds} = 2.5 V and at V_{ds} = 0.5 V; the latter is essentially the slope of the I_{dss} curve before current saturation, and is related to the channel resistance. The pinch-off voltage was defined as the gate-source voltage required to reduce the drain current, at V_{ds} = 2.5 V, to 20% of the value of I_{dss} at that voltage. Inasmuch as I_{dss} changed during the stress, two pinch-off measurements were made; one was based on the original value of I_{dss} before stress, I_{dsso}, and the other, on the value of I_{dss} at the time of the pinch-off voltage measurement. The characteristic curves were also obtained and the values of the transconductance, g_m, were calculated at the point of intersection of the load line and V_{ds} = 2.5 V. The reverse leakage current, I_{rgss}, was measured at a negative gate-source voltage of 4 V, with a drain-source short. Finally, the forward gate-source diode characteristics, with a drain-source short were measured. The high temperature measurements were made under the same conditions, except that the pinch-off voltage and the reverse gate leakage current were not measured. The zero voltage saturation current, I_s, and the ideality factor, n, were calculated from the measured forward gate-source diode characteristics. The barrier height at the gate-source interface was estimated from the values of I_s at room temperature and at the stress temperature. Failed devices were examined under a microscope, and their appearance was compared with the appearance of similarly stress unfailed devices.

Ten devices out of twenty-one failed as a result of stress at 150 °C; seven failed catastrophically because of damage to the gate lead and pad (five) or to the drain pad (two), and three exhibited electrically degraded behavior. Two of the latter became leaky, while the third exhibited a sharp reduction in I_{dss}; no physical changes could be seen in the three under the microscope. There was no clear change in any of the measured electrical parameters for any device preceding failure, nor for any unfailed device to the end of stress, either at room temperature or at 150 °C; in other words, there was no obvious electrical indication of degradation or as a precursor for catastrophic failure. No evidence of electromigration could be seen by optical microscopy in any device, failed or not. These results at 150 °C are consistent with results obtained in other DC and RF measurements.[15]

Twenty devices were stressed at 175 °C; seventeen failed catastrophically. Six of the catastrophic failures were infant failures, occurring at the stress temperature within five hours of the beginning of the stress. The electrical failure mode here was high gate leakage and high channel resistance; microscopic examination revealed gate pad damage in every case, with a burned area bridging the gate pad and source pad. Some drain-source common damage was also observed, but this may have been spill-over. The other eleven devices failed at times up to 1000 hours; six had high gate leakage and five were open gates. The open gate devices had lost their gate leads; the gate pads were blackened and heavily damaged. Four of the six devices with high gate leakage displayed the same kind of gate pad-source pad damage and bridging as did the infant failures. It was not possible to determine from the microscopic examination whether the gate pad

failed, or if it fused as the result of failure elsewhere in the device.

The eleven devices failed at the stress temperature also. All failed before the final room temperature measurements, at 1000 hours, could be performed. However, certain room temperature trends could be established by 500 hours of stress. In general, I_{dss} decreased from its pre-stress value, on the average, by 12%, although decreases as great as 25% were observed; channel resistance increased by around 15%; differential transconductance remained about the same, although the absolute transconductance decreased because of the compression of the characteristic curves; pinch-off voltage decreased because of the reduction in I_{dss}; the reverse leakage current became very high, in the order of microamperes. The zero bias saturation current showed considerable variation; it is difficult to obtain precise values of I_s inasmuch as an extrapolation to zero voltage is required, and a small change in the slope (the ideality factor, n) of the forward log current vs. voltage curve will introduce considerable inaccuracy. The ideality factor, n, increased from between 1.12 and 1.28 to around 1.18 to 1.47. The barrier height at the gate-substrate interface was estimated, and decreased, in general, from around 0.8 eV to 0.7 eV.

The devices which did not fail catastrophically exhibited the same trends, except that the changes after 1000 hours of stress were greater than those after 500 hours for the failed devices. I_{dss} decreased by an average of 17%; channel resistance increased by around 10%; the reverse leakage current was in the order of tens of microamperes; the change in n was about the same as for the failed devices; and the estimated barrier height decreased from some 0.8 eV to 0.6 eV.

Excluding the infant failures, all devices, including those which did not fail catastrophically, showed significant alterations in the drain stripe metallization. There was also some lifting of the silicon nitride overcoat; this is probably an effect of the high stress temperature, inasmuch as it also occurred in the adjacent cell, which had no gate or drain connection, and carried no current. There was a build-up of metal at the gate pad end of the drain stripes, appearing as raised hillocks, and a thinning of the drain stripes near the drain pad. This is a surprising result, and does not agree with other observations on similar devices under RF conditions,[16] in which the direction of metal migration is toward the drain pad end of the drain stripes. The latter results, however, were obtained with essentially linear operation, and in the stresses imposed in this work, substantial forward gate current (between 50 mA and 100 mA) flowed. No control measurements on only DC biased devices were made at 275 °C, so that it is not possible to assess the effects of the forward gate current at this time

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