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FABRICATION AND HIGH TEMPERATURE CHARACTERISTICS OF ION-IMPLANTED GaAs BIPOLAR TRANSISTORS AND RING-OSCILLATORS*

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INTRODUCTION

A growing need is developing for monolithic semiconductor circuits for high temperature environments. Si-devices have been reported to operate up to 300°C.[1,2] Because the upper operating temperature of a bipolar device is determined by the bandgap of the semiconductor material, GaAs (1.43eV) has a theoretical advantage over silicon (1.12eV). Based on bandgap considerations exclusively, GaAs could be expected to be useful up to 450°C; in fact, transistors have been operated at this temperature.[3] Based on these assessments a special program to study the high temperature aspects of GaAs bipolar transistors was initiated in 1966. The results of this program, which were reported in 1968[4], showed: GaAs transistors were limited by leakage currents, which exhibited a temperature dependence with an activation energy of 0.7eV. The current gain h_{fe} decreased rapidly with increasing temperature with an activation energy of approx. 0.2eV, apparently due to a decrease of the minority carrier lifetime. Devices which operated above 400°C could be made, but the fabrication yield was extremely small. The technology available at this time was constrained to sulfur and magnesium diffusions at temperatures at which surface decomposition could not sufficiently be suppressed. Doping control was poor. The devices had mesa structures with little surface passivation. The fabrication of a sophisticated GaAs IC was beyond reach.

During the recent years the GaAs technology progressed rapidly, motivated mainly by the excellent performance of microwave FET's. Ion implantation and annealing techniques were developed to form reproducibly thin layers of controlled doping levels. This progress made it desirable to re-evaluate the GaAs bipolar device performance. Potential advantages of a GaAs bipolar technology include: short minority carrier lifetime; high electron mobility at low electron fields; use of saturated drift velocity for load resistors (small area requirements); isolation by boron implantation (requires less area than junction isolation); higher operating temperature than silicon devices. The bipolar technology would permit the application of established Si bipolar circuit concepts and models with only minor modifications. Some disadvantages of GaAs, namely the low hole mobility and the comparatively low maximum donor concentration will remain with us. The possibility of modifying the bandgap by using GaAlAs, e.g. for wide band gap emitters, and of incorporating opto-electronic principles make this technology particularly exciting. The main difference between the situation a decade ago and today is that ion-implantation offers the reproducible production of p-n junctions, avoiding the damaging high temperature diffusions. Originally our present program was designed to study the feasibility of a GaAs bipolar IC technology but not specifically the high temperature aspects. Results obtained with a 15-stage ring-oscillator were reported recently.[5] It will be apparent that specific modifications will have to be incorporated to extend performance and reliability to higher temperatures, such as the replacement of the alloyed gold contacts. This paper will discuss the fabrication and high temperature performance of discrete bipolar transistors and of a 15-stage ring oscillator.

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DEVICE FABRICATION

The fabrication of GaAs bipolar transistors by ion implantation into bulk GaAs has been reported previously.[6] The fabrication of the ring-oscillator requires an epitaxial n/n^+ structure. The starting GaAs substrates, purchased from commercial suppliers, come from Bridgman-grown single crystals. The $AsCl_3$-Ga-H_2 vapor phase epitaxial process is employed to deposit 2 layers: first an approx. 3 micron thick layer with a donor concentration of approx. 8×10^{17} cm^{-3}, followed by an undoped layer, approx. 1 micron thick. The VPE technology, as applied to microwave devices in our laboratory, has previously been described in the literature.[7]

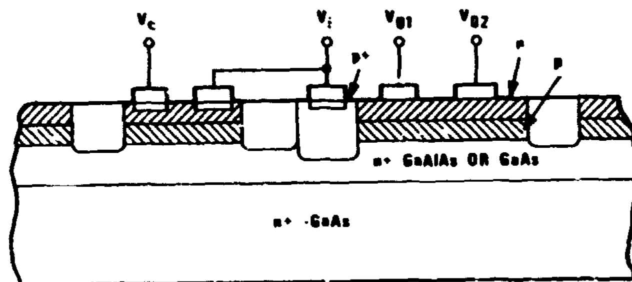

Fig. 1 Cross-section of a bipolar IC structure

The cross-section of a bipolar IC-structure is shown in Fig. 1. The npn transistor operates in the "up"-mode: the n^+-epitaxial layer/substrate acts as emitter, the surface n-layer is the collector. Also shown is the load resistor. The fabricated structures differ from Fig. 1 in one respect: they have only one alloyed collector contact on the n-type surface layer.

The formation of the n- and p- layers employs ion-implantation. The details of the donor implantation are drawn from extensive experience with GaAs FET's.[8] The base-layer is formed by a deep implant of Be, which is known to have high activation at low anneal temperatures.[5,10] Preservation of the GaAs surface morphology during the high temperature

annealing step is achieved by the proximity annealing technique.[8,11] The sequence of fabrication steps for the bipolar structure is as follows:

1. Shallow Se implant (1×10^{13} cm^{-2}, 150 keV plus 2×10^{13} cm^{-2}, 360 keV at 350°C).

2. Anneal at 850°C for 30 min.

3. Deep Be implant (6×10^{12} cm^{-2}, 180 keV) to form the base layer.

4. Anneal at 800°C, 30 minutes.

5. Localized Be implants to form the p^+ contact regions (1×10^{14} cm^{-2} at 40 keV plus 1.5×10^{14} cm^{-2} at 80 keV).

6. Anneal at 700°C, 30 minutes.

7. Localized Boron implant to form the isolation region (2×10^{12}, 4×10^{12}, 6×10^{12} cm^{-2} at 50, 140, 320 keV, respectively).

Si_3N_4 serves as implant mask and for device passivation. Contacts are alloyed Au-Ge-Ni for the n-type material and alloyed Au-Zn for the p-type base. Ti - Au is used for interconnections. Stripes of GaAs, whose width is adjusted by a Boron implant, serve as load resistor.

The doping profile of the complete structure is presented in Fig. 2. The ion-implanted profiles are calculated according to the LSS-theory, modified by experimentally observed activations. The transition from the n^+ epilayer to the surface n-layer was established by C-V profiling.

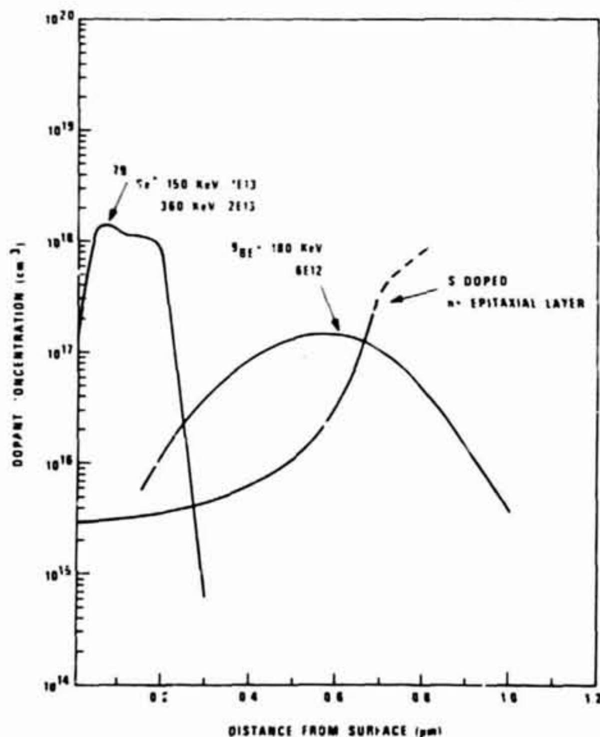

Fig. 2 Doping profile

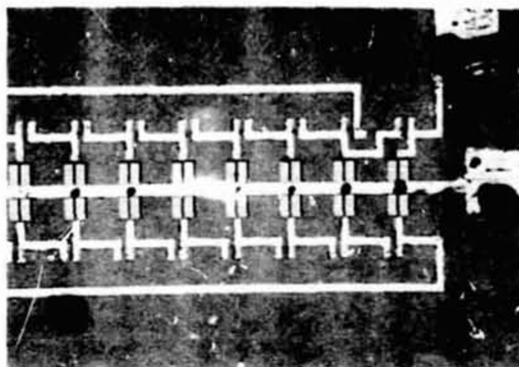

Fig. 3 GaAs Ring-Oscillator

DEVICE PERFORMANCE

A 15-stage ring oscillator was tested in the temperature range of 25°C - 390°C. Fig. 3 shows a micrograph of the circuit after this test. The circuit was mounted in a ceramic IC-package and placed in an oven. The package was not sealed, i.e. the GaAs device was exposed to hot air during the test. The bias voltage was 1.75 volt, resulting in a total input current of 5 mA at 25°C, increasing to 7mA at 385°C. Fig. 4-6 present the output signal at 25°, 240°C, 385°C. The gate delay time increases from 3.3ns at 25°C to 6.7ns at 385°C. The time constant of the circuit is dominated by the product of the capacity of the forward biased emitter diode times the load resistor. The decrease of the electron mobility in the GaAs load resistor causes the time constant to increase. The output signal of the ring oscillator approx. triples with rising temperature. Two effects contribute to this effect: 1. the increased value of the load resistor; 2. The shift of the Fermi levels towards the center of the bandgap with increasing temperature decreases the built-in voltage of the emitter junction, thereby increasing the injection current and decreasing the saturation voltage. The ring oscillator failed at 390°C. The examination of the failed device shows a damaged metallization in the via holes of the voltage supply bar, as shown in Fig. 3. This was probably caused by a realloying of the Au contacts, and a subsequent break in the metallization on the via sidewalls.

A discrete bipolar transistor on this same chip was subsequently characterized in detail. The transistor characteristics were measured both for "down"-mode (surface layer as emitter) and the "up"-mode (surface as collector, corresponding to the mode in the ring-oscillator). Furthermore the leakage currents of the emitter diode, the collector diode and I_{CEO} were determined between 25°C and 400°C. Fig. 7-10 present some curve tracer pictures of the transistor characteristics at different temperatures. The device exhibits current gain beyond 400°C. The useful temperature range is limited by junction leakage currents. Fig. 11 presents plots of I_{CEO}, in both "up" and "down" mode, and the emitter and collector diode leakage currents at 2 volts vs the reciprocal temperature. Both diodes have very similar leakage currents with a temperature dependence corresponding to an activation energy of approx. 1eV. I_{CEO} is temperature insensitive to about 200°C; then it becomes dominated by the leakage current of the reverse biased collector junction. The difference in I_{CEO} in the

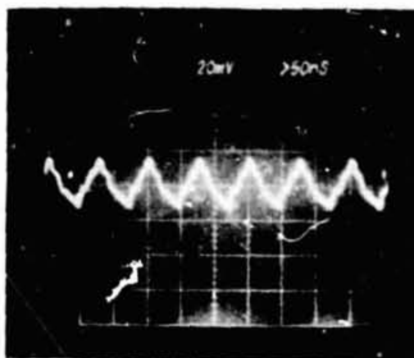

Fig. 4 GaAs Ring-Oscillator, 25°C

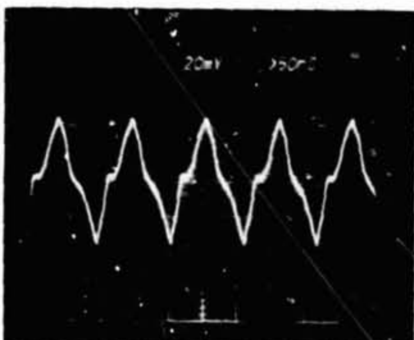

Fig. 5 GaAs Ring-Oscillator, 240°C

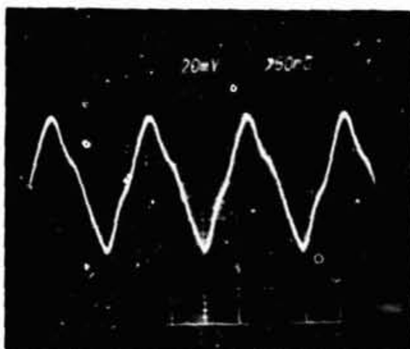

Fig. 6 GaAs Ring Oscillator, 385°C

Fig. 7 GaAs bipolar transistor at 25°C, "down"-mode

Fig. 8 GaAs bipolar transistor at 25°C, "up"-mode

Fig. 9 GaAs bipolar transistor at 390°C, "down"-mode

Fig. 10 GaAs bipolar transistor at 400°C, "up"-mode

two modes is probably caused by the asymmetry of the doping profile and the geometry of the transistor structure. The current gain as a function of temperature is presented in Fig. 12. In the "up"-mode h_{fe} is temperature insensitive to approx. 350°C. This performance is in contrast with results obtained previously[4] from diffused transistors where the current gain of the best device began to decrease already below 250°C.

CONCLUSION

Ion-implantation techniques permit the reproducible fabrication of bipolar GaAs IC's. A 15-stage ring oscillator and discrete transistor was characterized between 25° and 400°C. The current gain of the transistor was found to increase slightly with temperature. The diode leakage currents increase with an activation energy of approx. 1 eV and dominate the transistor leakage current I_{CEO} above 200°C. Present

devices fail catastrophically at ~ 400°C because of the Au-metallization. For the development of a reliable GaAs bipolar IC-techology for the 350°C-range the following subjects have to be addressed: Implementation of refractory-metal contacts; raising of doping levels to minimize the depletion layer width and to decrease the temperature sensitivity; improvement of surface passivation. The performance of GaAlAs structures should be studied with respect to leakage currents and surface degradation. It is known, e.g. that the addition of small Al concentrations to the active zone of injection lasers reduce degradation.

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REFERENCES

1. D.C. Dening, L.J. Ragonose, S.C.Y. Lee, "Integragrated Injection Logic with Extended Temperature Range Capability", IEDM, Washington, 1979.
2. D.W. Palmer, R.C. Heckman, "Extreme Temperature Range Microelectronics", IEFE Transact. on components hybrids and manufacturing technology, Vol. CHMT-1, No. 4, Dec. 1978, p. 333-340.
3. H. Strack, "Iron Doped GaAs Transistors", GaAs, Proceedings of the First International Symposium, Reading G.B. 1966, Institute of Physics and Physical Society, Conference Series No. 3 p. 206.
4. F.H. Doerbeck, E.E. Harp, H.A. Strack, "Study of GaAs Devices at High Temperature", GaAs, Proceedings of the Second International Symposium Institute of Physics and Physical Society, Conference Series No. 7. p. 205.
5. H.T. Yuan, F.H. Doerbeck, W.V. McLevige and G.E. Dierschke, "GaAs Bipolar Integrated Circuit Technology". IEDM Technical Digest, Washington D.C. 1980.
6. H.T. Yuan, F.H. Doerbeck, W.V. McLevige, "Ion Implanted GaAs Bipolar Transistors", Electronic Letters, 31 July 1980, Vol. 16, No. 16. p. 637-638.
7. F.H. Doerbeck, "Materials Technology for X-band GaAs FET's with Uniform Current Characteristics", Inst. Phys. Conf. Ser. No. 45, 1979, p. 335-41.
8. F.H. Doerbeck, H.M. Macksey, G.E. Brehm, and W.R. Frensley, "Ion-implanted GaAs X-band power FET's, Electron. Lett., 1979, 15, p. 576-577.
9. M.J. Helix, K.V. Vaidyanathan, B.G. Streetman, and P.K. Chatterjee, "Planar GaAs p-n junctions by Be ion implantation", IEDM Technical Digest, 1977, p. 195-197.
10. W.V. McLevige, M.J. Helix, K.V. Vaidyanathan, and B.G. Streetman, "Electrical profiling and optical activation studies of Be-implanted GaAs", J. Appl. Phys., 1977, 48, p. 33-42.
11. W.M. Duncan, F.H. Doerbeck, G.E. Brehm, "Proximity Annealing of Ion implanted GaAs for Microwave Devices", Workshop: Process Technology for direct ion-implantation in semi-insulating III-V Materials, Santa Cruz, Cal. Aug. 12-13, 1980.

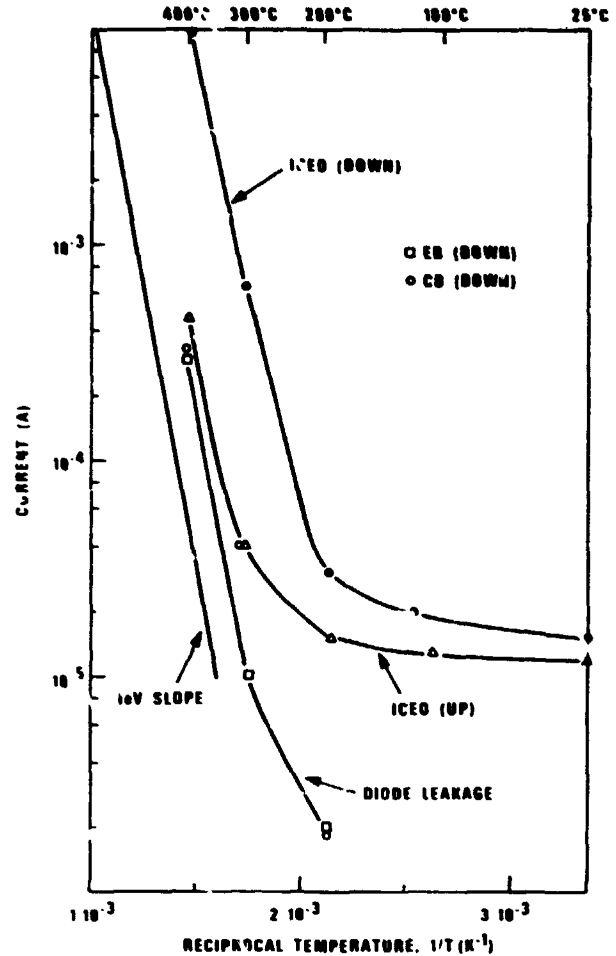

Fig. 11 Diode leakage currents and I_{CEO} as a function of the reciprocal temperature

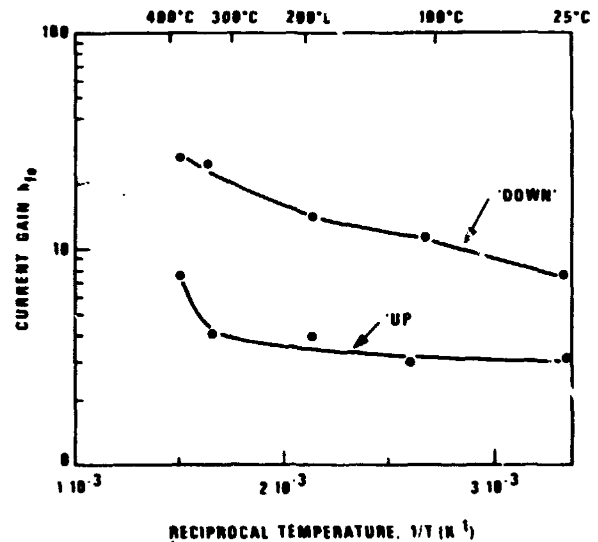

Fig. 12 Current gain as a function of the reciprocal temperature