

**SEMICUSTOM INTEGRATED CIRCUITS AND THE STANDARD
TRANSISTOR ARRAY RADIX (STAR)**

by

**Teddy M. Edge
Electronics Development Division
Electronics and Control Laboratory**

**George C. Marshall Space Flight Center
Marshall Space Flight Center, Alabama 35812**

SUMMARY

This paper describes the development, application, pros and cons of the semicustom and custom approach to the integration of circuits. Integrating with custom and semicustom is considered in terms of cost, reliability, secrecy, power, and size reduction. Sources of commercial semicustom integrated circuits are included with circuit types and costs.

The development of a Standard Transistor Array Radix (STAR) at the NASA-Marshall Space Flight Center is also described. STAR is a semicustom approach to digital integrated circuits that offers the advantages of both custom and semicustom approaches to integration.

INTRODUCTION

The development and utilization of integrated circuits has certainly been a significant technical accomplishment. The application of large scale integration to items that affect us directly are becoming evident in the form of pocket calculators, digital watches, home appliances, automobiles, and other electronic hardware. As still the technology is changing so rapidly that it is impossible to stay abreast of the new products introduced daily which employ integrated circuits. This technology like so many others was spawned and utilized by the space program and its benefits are now spreading.

The area of integrated circuits is a highly complex technology and its understanding and application by those who are directly involved in it can be difficult. Such choices as which integrated technology to use, selecting off-the-shelf chips, employing a microprocessor, or developing a custom integrated circuit are things with which electronic designers are confronted. This paper and presentation describe the development, application, pros and cons of the semicustom and custom integrated circuits, and the development of STAR and the NASA-Marshall Space Flight Center.

Most electronic designers never consider the use of a custom or semicustom integrated circuit when converting logic to hardware. The designer realizes there are usually enough standard chips available that have been produced by integrated circuit manufacturers to do the job. These standard parts have evolved over a period of years based on demand and the ability of the integrated circuits manufacturer to produce large volumes cheaply. The

designer realizes that it would be advantageous if all the chips could be included in one chip; but complexity, cost, and turnaround have prevented most designers from attempting to integrate their designs. However, with repeatable processing, newly added technologies, new sources, a demand for faster turnaround, secrecy of design, and the willingness on the part of some large processing facilities to process for the low volume semicustom sources, a semicustom integrated circuit may be the best design solution. The large processing facilities accept this arrangement because the summation of the semicustom sources work amounts to volume.

Semicustom or standard integrated circuit patterns have existed for quite a few years. It was realized early that if you could develop a standard array that contained transistors, diodes, and resistors, and use only one unique mask (the metal interconnect mask), most of the production steps would be eliminated and a semicustom integrated circuit would result. This was first applied to the bipolar technology and has been used successfully in linear applications. The semicustom approach also works for digital circuitry with replicated gates, logic cells, and input/output buffers. In each case the wafers are processed up to the metallization layer. The unique metal mask which converts the standard patterns to a semicustom integrated circuit is only defined upon need, and in many cases the metal mask layout can be done by the designer. Figures 1 and 2 show commercially available semicustom linear and digital integrated circuit.

The true custom integrated circuit (unique from diffusions to metallization) has always been viable. It has been developed in all technologies, implemented with manual and design automation techniques and is the best approach for the large volume user. However, the low volume user has been left out of the custom approach due to high initial cost and the large part orders/year required. Figure 3 is an example of a true custom integrated circuit implemented using design automation techniques employing standard logic cells.

In the digital area the microprocessor has shown strength in its applications with a number of microprocessors attempting to solve the designers need for custom hardware. The designers are suddenly faced with becoming microprogrammers as well as hardware specialists. This also puts a burden on the microprocessor, since it must do every general task, its use may become more complex, costly, and prolonged than if the custom or semicustom hardware equivalent had been used. Figure 4 is a microprocessor board with its supporting chips.

It becomes evident that custom hardware is here to stay along with standard parts and microprocessors. There is a need for enhancement of the semicustom approach with emphasis on ease of integration, high packing density,

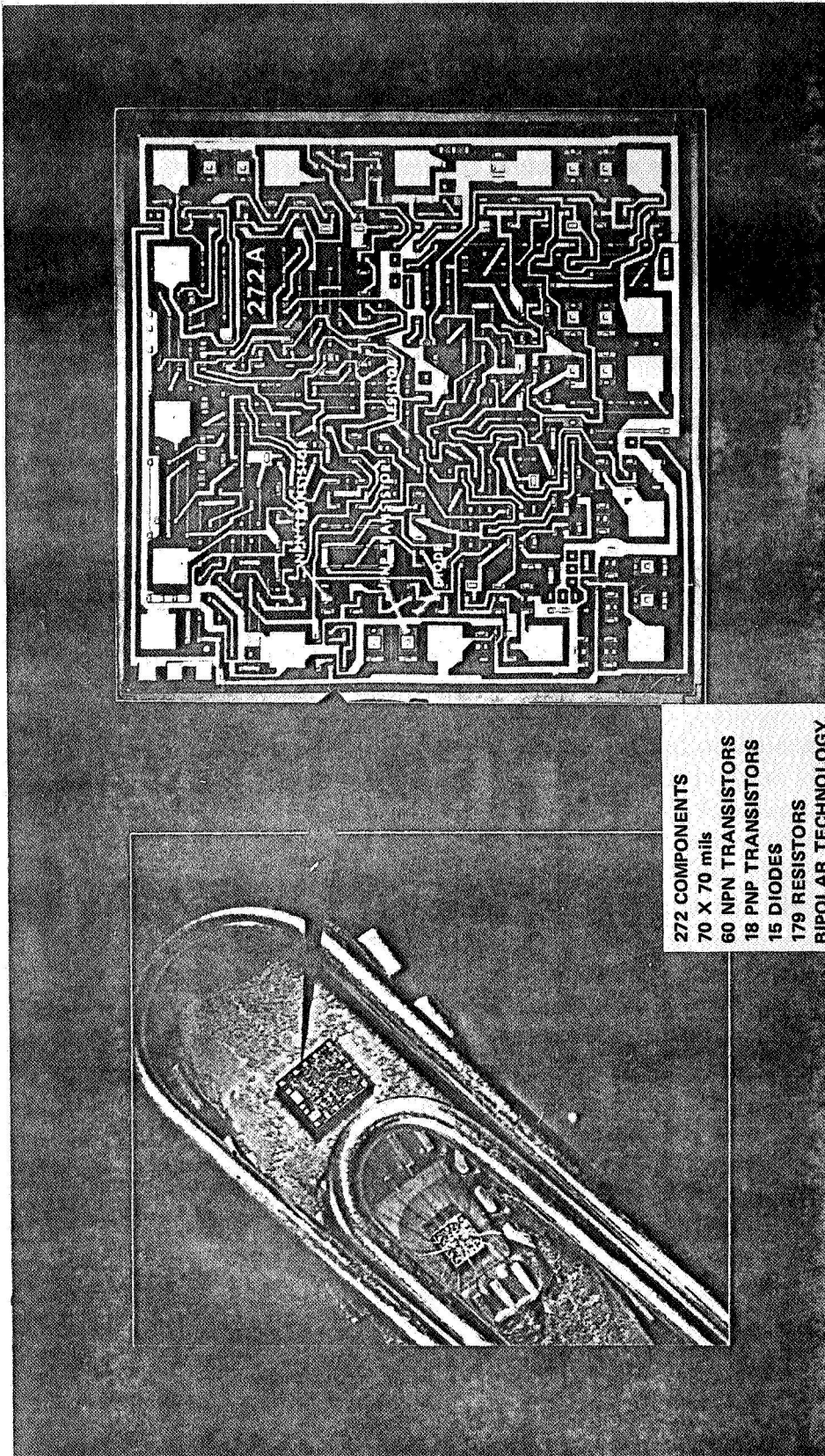


Figure 1. Semicustom linear integrated circuit.

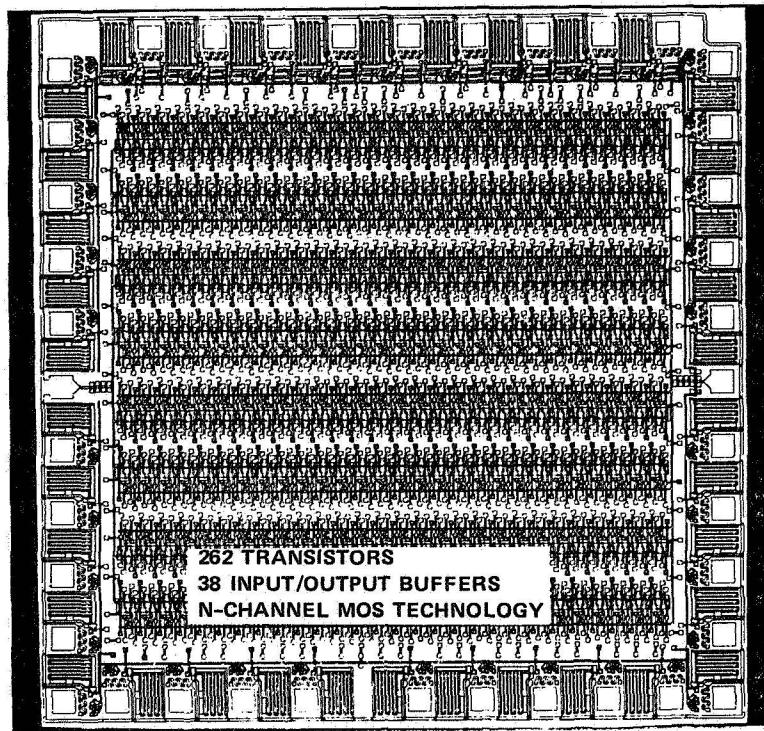


Figure 2. Semicustom digital integrated circuit.

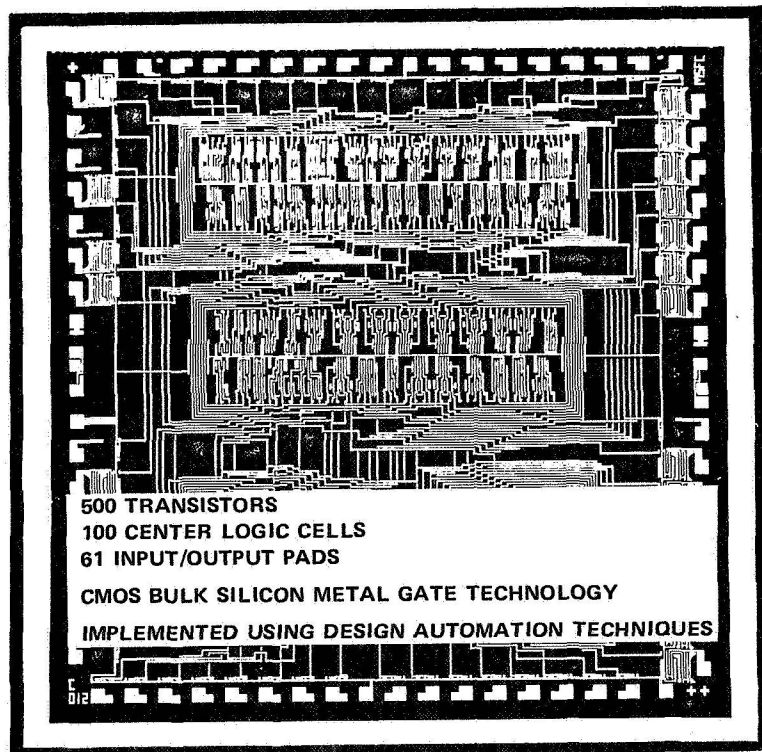


Figure 3. A custom digital integrated circuit.

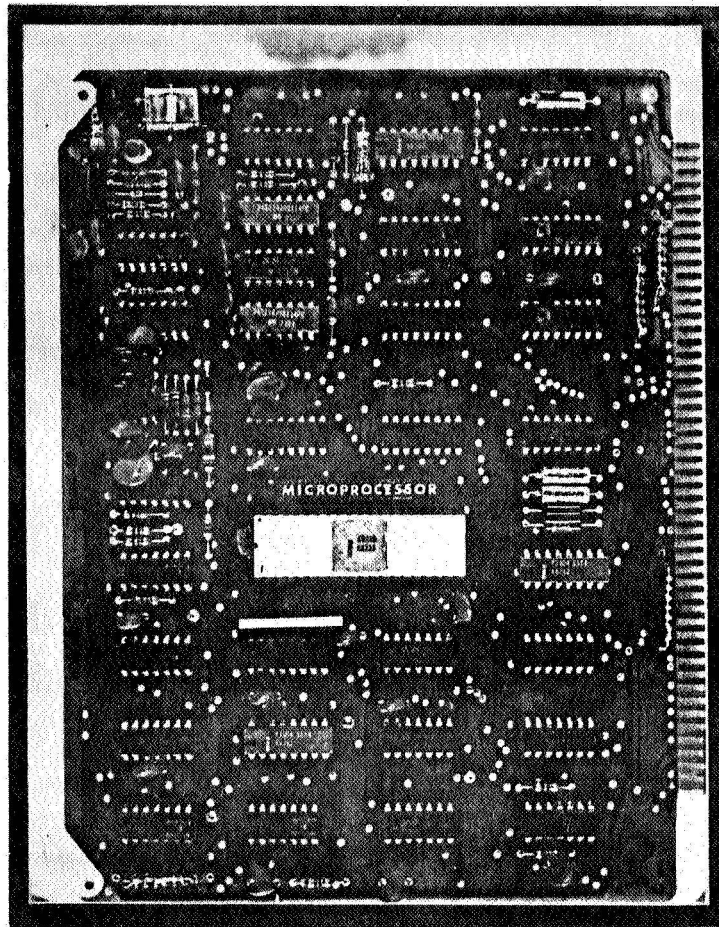


Figure 4. The microprocessor.

and flexibility with technologies while gaining the benefits of lower cost, high reliability, secrecy of design, lower power dissipation, and servicing ease. Figure 5 represents a brief look at the reasons for integrating, and a discussion of these points in terms of custom and semicustom integrated circuits follows.

- COST
- RELIABILITY
- SECRECY
- POWER
- SIZE
- SERVICING

Figure 5. Semicustom versus custom.

COST

Cost reduction is a significant reason for integration. It is not uncommon to integrate a logic board with 30 standard parts costing \$50 to \$100 into a single chip costing \$10 to \$30. There are also other indirect cost reductions due to reduction of interconnects and reduced power needs. Semicustom integration costs range typically between \$1800 to \$10 000 which yields initially 25 to 70 prototype parts in three to eight weeks. Some designs are practical for as few as 100 circuits; but most are in the 1000 to 100 000 quantity range. The price range is determined by a choice of development plans that range from total designer layout to complete semicustom source responsibility. Additional packaged parts typically cost \$0.80 to \$8.00 each with the cost determined by the quantity required. True custom integration costs are significantly higher, typically \$50 000 to \$100 000 required initially and a minimum order of 100 000 parts/year with six months to a year turnaround. Designs requiring above 100 000 parts tend to be vehicles for true custom integration with the price per part negotiated.

RELIABILITY

Another reason for integration is reliability. Interconnections are the weakest link in a system. If thirty packages are integrated into one a substantial number of interconnections have been eliminated. The reliability of semicustom and custom integrated circuits will be equal if designed (same design guidelines), processed, and packaged equally.

SECRECY

Secrecy of design is becoming of great importance, especially in the high risk commercial markets. This is a main selling point for the semicustom sources. Custom integrated circuits would be even more difficult to copy.

POWER REDUCTION

The integration of thirty separate chips into one will yield a power reduction in any technology with custom or semicustom integration. Power requirements are very application and technology dependent. Semicustom sources provide most of the established technologies that are repeatable by different processing facilities. Custom circuits provide these technologies and the newer ones.

SIZE REDUCTION

Integration always brings about a size reduction whether done in semicustom or custom. In terms of actual silicon used it is generally true that the commercial semicustom circuit will use more silicon than an equivalent custom circuit because only 80 percent of the patterns are normally utilized.

A list of the major sources of commercial semicustom integrated circuits is given in Table 1. Included are their trade names, available technologies, circuit types, basic cost, and turnaround times. Each source will supply upon request information explaining their integration procedures. Some sources provide a design kit (\$25 to \$90) which includes layout manuals, subsystem parts, and detailed information for layout of the interconnecting data.

THE STANDARD TRANSISTOR ARRAY RADIX (STAR)

This material describes a digital semicustom approach to integrated circuits. Our interest in semicustom integrated circuits in the Electronics and Control Laboratory, MSFC, has developed from our experience with custom integrated circuits. At MSFC we have an established custom integrated circuits program that is primarily research and development but provides support for in-house programs in low volume. The system incorporates state-of-the-art design automation software. This includes automatic layout programs, logic simulators, mask analysis, interactive graphics, test pattern generation, and artwork generation software. Mask making, device processing, and packaging capabilities are also available.

TABLE 1. SEMICUSTOM INTEGRATED CIRCUITS SOURCES

Sources	Trade Name	Technology Circuit Types	Linear Components/Digital Gates	Base Cost	Prototypes/ Turnaround
Exar Integrated Systems Sunnyvale, CA	XR-Chips	I ² L Linear-Digital	125/256 up to 88/864	\$1500	50 Prototypes/4 to 6 weeks
Interdesign Inc. Sunnyvale, CA	Monochip	Bipolar and NMOS Linear Digital	110/-- up to 300/-- 262	\$1800	50 Prototypes/3 weeks
International Mircircuits Inc. Santa Clara, CA	Mastermos	CMOS Digital	--/50 up to --/800	\$2800	50 Prototypes/3 to 6 weeks
Microcircuit Technology Santa Clara, CA	Masterchips	NMOS Digital	--/120 up to --/640	\$2650	70 Prototypes/5 weeks
Stewart-Warner Microcircuits Sunnyvale, CA	Swap	I ² L Linear	208/--up to 408/--	\$5000	25 Prototypes/4 to 8 weeks
				\$1800	25 Prototypes/4 weeks

The development of the STAR stems from an attempt to mix the best of both custom and semicustom approaches to integration. Figure 6 is a flow chart of the development. The main objectives were ease of use (system establishment and operations), high packing densities, and flexibility with changing technologies.

Ease of use was a primary point because of our awareness of the difficulties in establishing and supporting a design automation software system. Many potential users do not have large computers, interactive graphics system, large staffs, or financial backing to support a complex design automation system. The STAR approach provides for manual or printed interactive graphics and design automation. A predefined array of transistors that the user need not design, and a column-row layout that can be implemented on a relatively inexpensive computer. The cell concept is used but the actual devices are not involved in the cell design, only a double metal interconnect of the devices are routed to achieve the logic function.

Achieving high packing densities equal to or better than automatic layout was another aim and is achieved through an MSFC double metal process.

As technologies change there is a need for the design system to follow the technology but without a major overhaul of the software. The STAR is flexible because only the array understructure need be redefined. The new masks are generated and the STAR processed in the new technology. The cell placement and interconnect data that are defined for a design in one technology are transferable to another technology because only the array understructure changes. Wiring channels, gate locations, and source-drain contacts are maintained at fixed locations.

A double metal MOS process was defined by the device processing facility. This MSFC sputtered double metal process has been employed in small scale integration with double metal interconnect over the active and inactive regions of the chip. Continued testing with large numbers of interconnects and VIA's confirmed the process to be viable. Figures 7 and 8 show the double metal cross section and an example of its implementation.

The transistor array consists of alternating rows of P and N devices with ground and V+ supply. The transistors are sized for logic loads and are paralleled when driving large off-chip loads. The array is surrounded by multiple use input/output pad cells. Conversion from input to output to power pad is accomplished by placing metal lines that bypass series resistors. The first array is in CMOS bulk silicon technology with the array defined in CMOS silicon

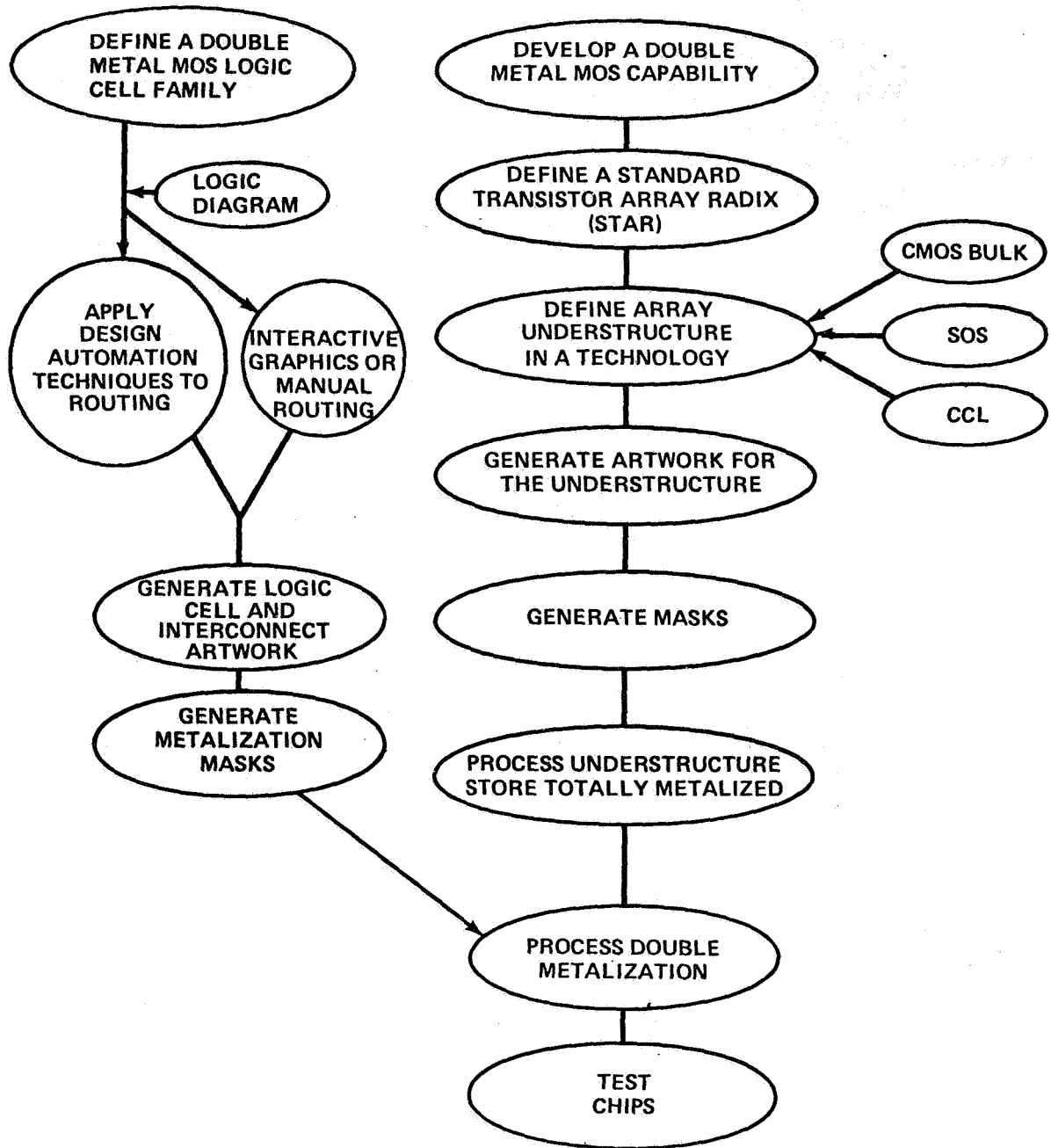


Figure 6. STAR semicustom approach.

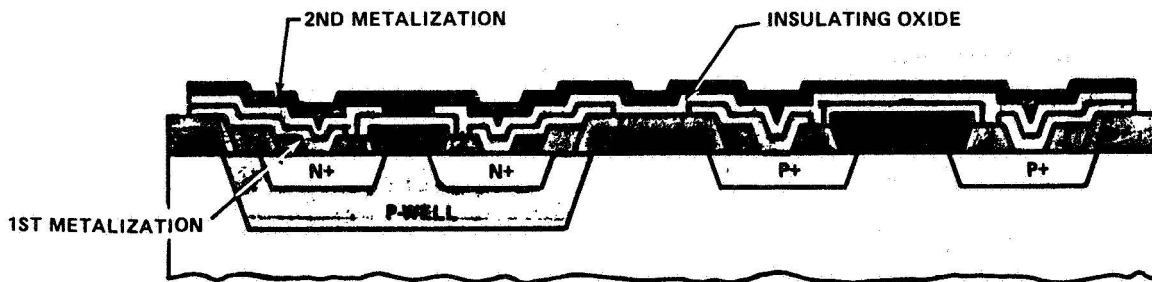


Figure 7. Double metal CMOS bulk metal gate technology cross section.

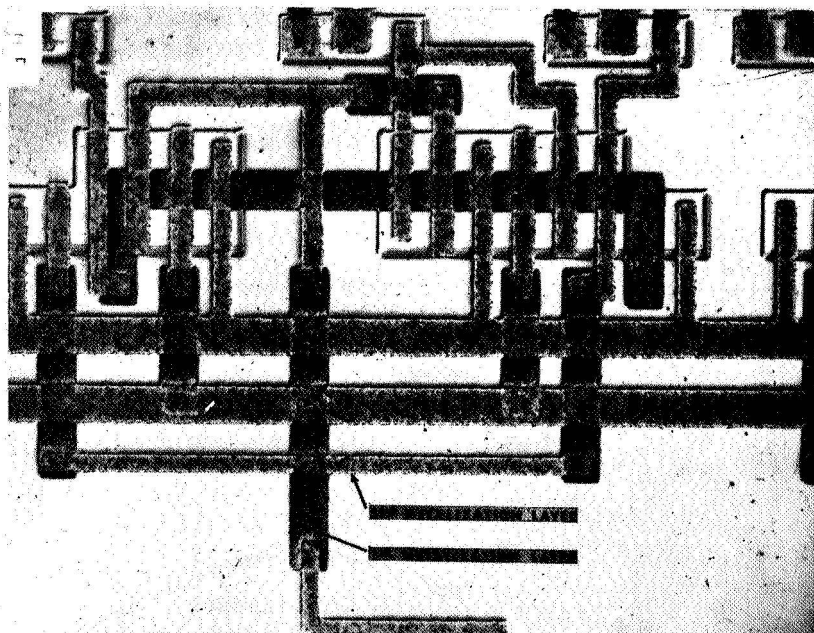


Figure 8. MSFC double metal MOS technology implemented.

gate, CMOS-SOS, and in closed contour logic (CMOS bulk and CMOS-SOS). The artwork for the array was generated with design automation software and the masks fabricated. The first five masks were used to process the array up to total metallization. The basic array will be produced in three sizes ranging from 384 transistors to 5264, and these sizes are shown in Figures 9 and 10.

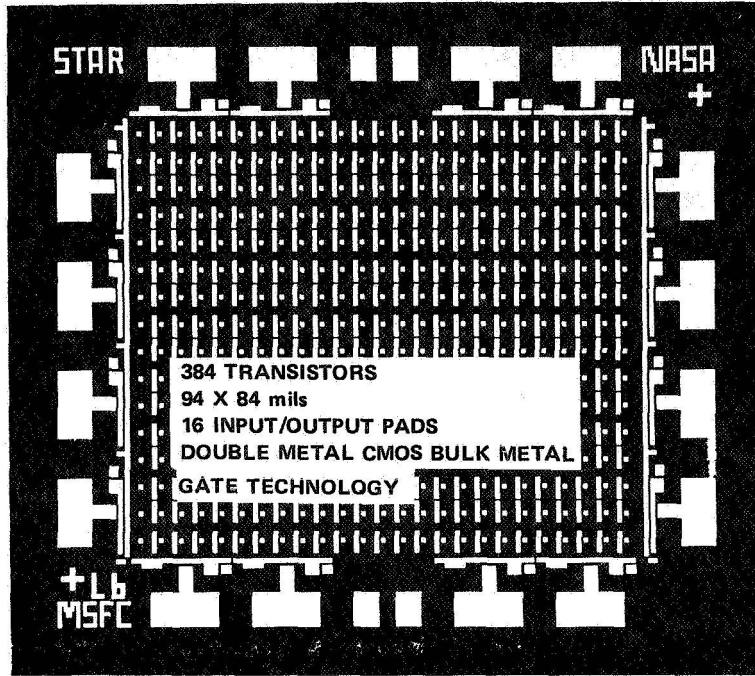


Figure 9. 384 transistor STAR structure.

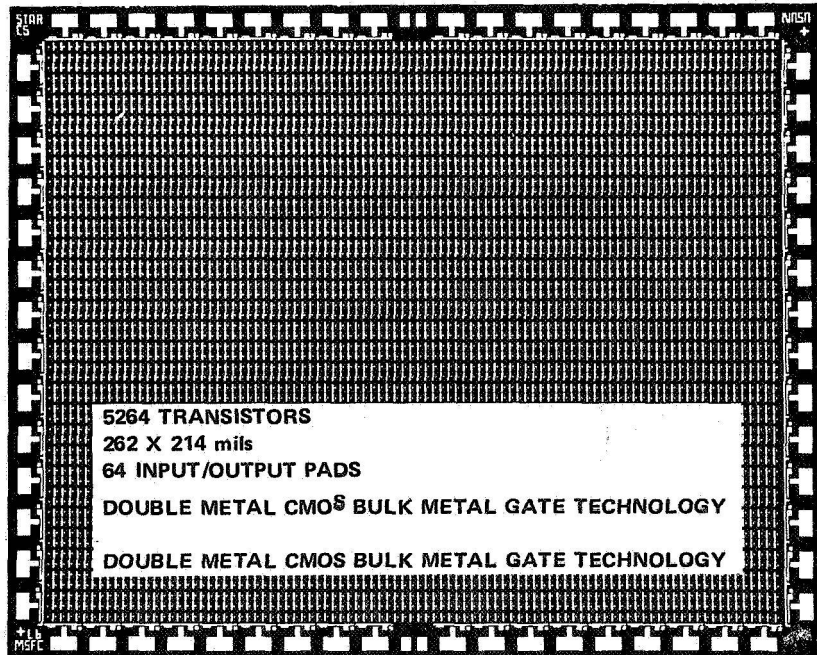


Figure 10. 5264 transistor STAR structure.

A double metal logic cell family was defined which contains the normal building blocks for logic design. A cell is designed by defining the double metal interconnect to the transistors.

Figure 11 shows the array layout and the STAR logic cell design. All cell placements and routes are restricted to an 0.8 mil grid. The first level of metal is 0.5 mil; VIA's through the insulating oxide are 0.3 mil, and the second level of metal is 0.4 mil. Vertical routine is normally done in first level metal and horizontal routing in second level metal. Each cell design starts with a source-drain tied off to ground and V+. The three routing channels between the P and N transistors are normally used for cell design. The wiring channel stubs surrounding the cell in Figure 11 show the routing channels available in double metal to supply signals and to interconnect the cells. Figure 12 is an example of a large STAR cell layout.

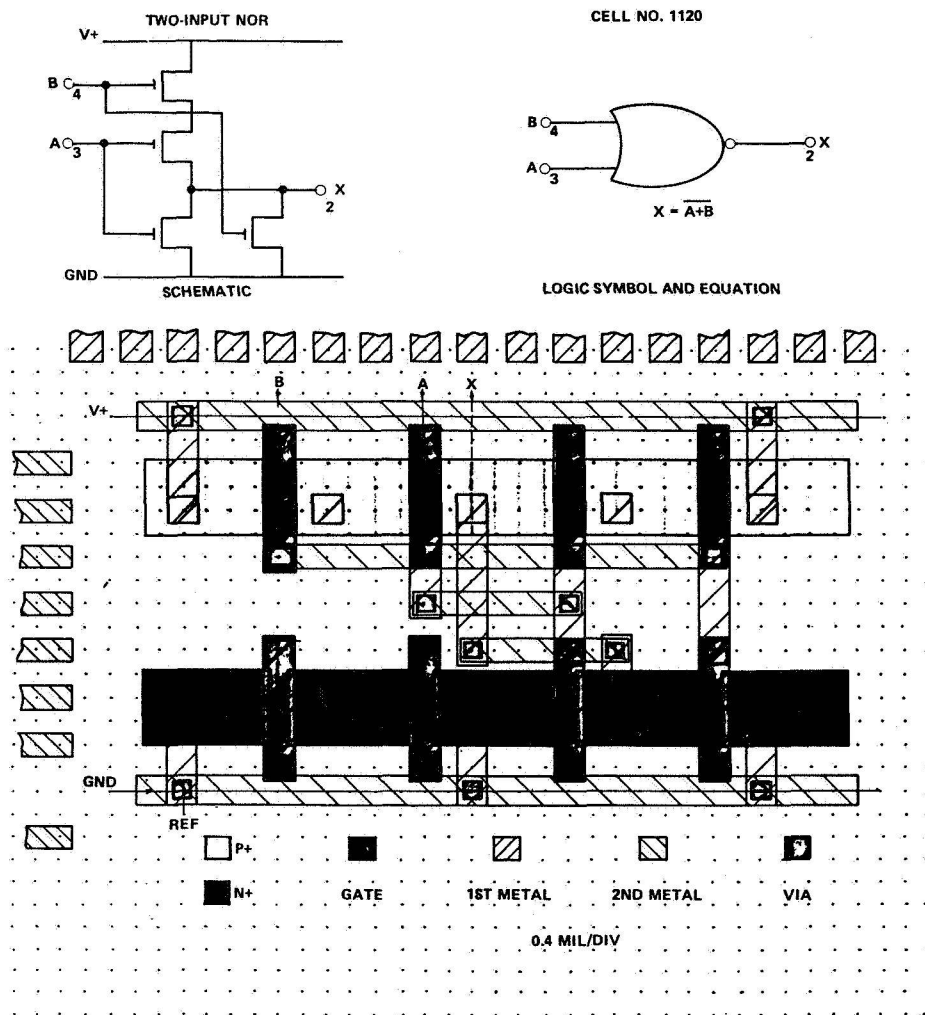


Figure 11. STAR logic cell.

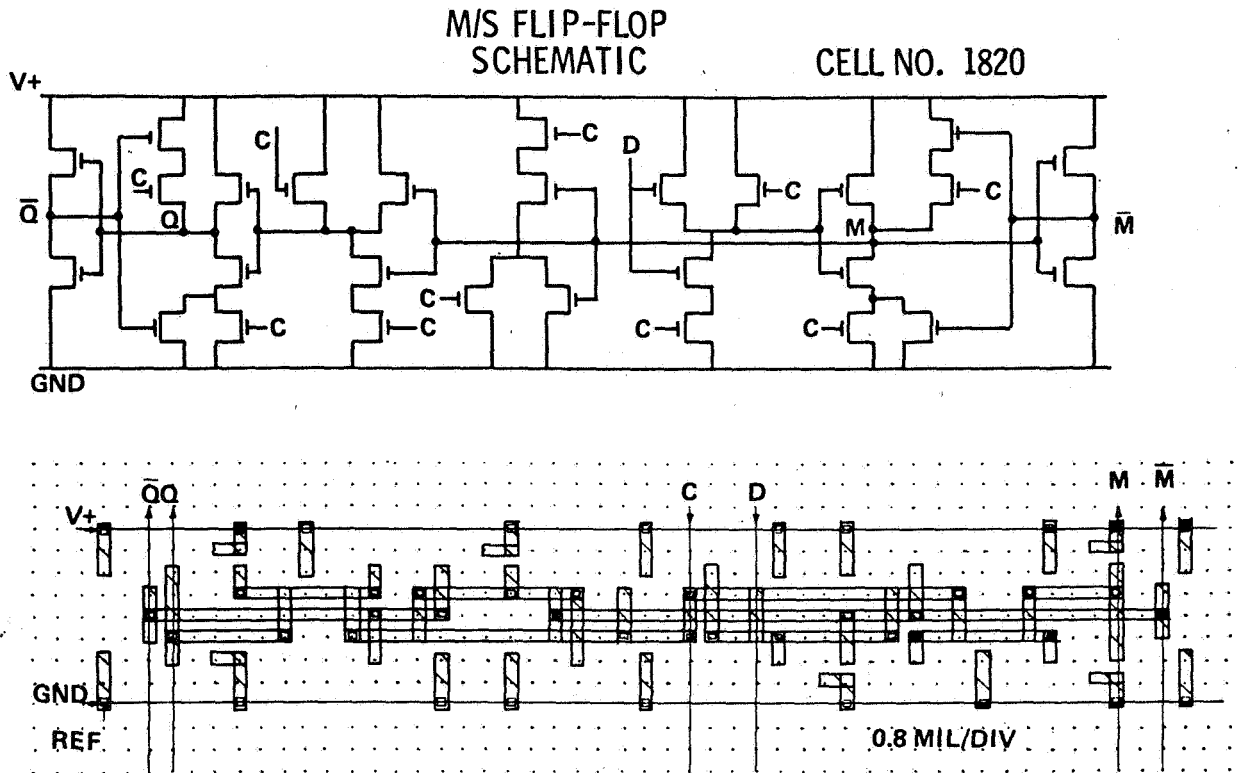


Figure 12. STAR logic cell layout.

Actual placement and routing of the logic cells to complete a logic design can be done on graph paper, a PCB layout system, interactive graphics, or with design automation techniques. This flexibility is due to the 0.8 mil grid system to which all cell placements and routes are restricted. Figure 13 is a portion of a design with logic cell placed and interconnected. The transistor understructure is not shown since only the interconnect levels were being defined and the input/output cells are only used as a backdrop for routing into them. For manual layout a printed backdrop of the array understructure with the input/output cells will be used and the cell placements and routing would be done on a transparent oversheet. Design automation techniques are currently being applied to the STAR which will form the routing data from an input connectivity list. The cell placement and routing data in the form of cards or other computer input is merged by an artwork generation program to generate the double metal interconnect mask data. The masks are used to convert the already processed array understructure into a semicustom integrated circuit as described and shown in Figures 14 and 15.

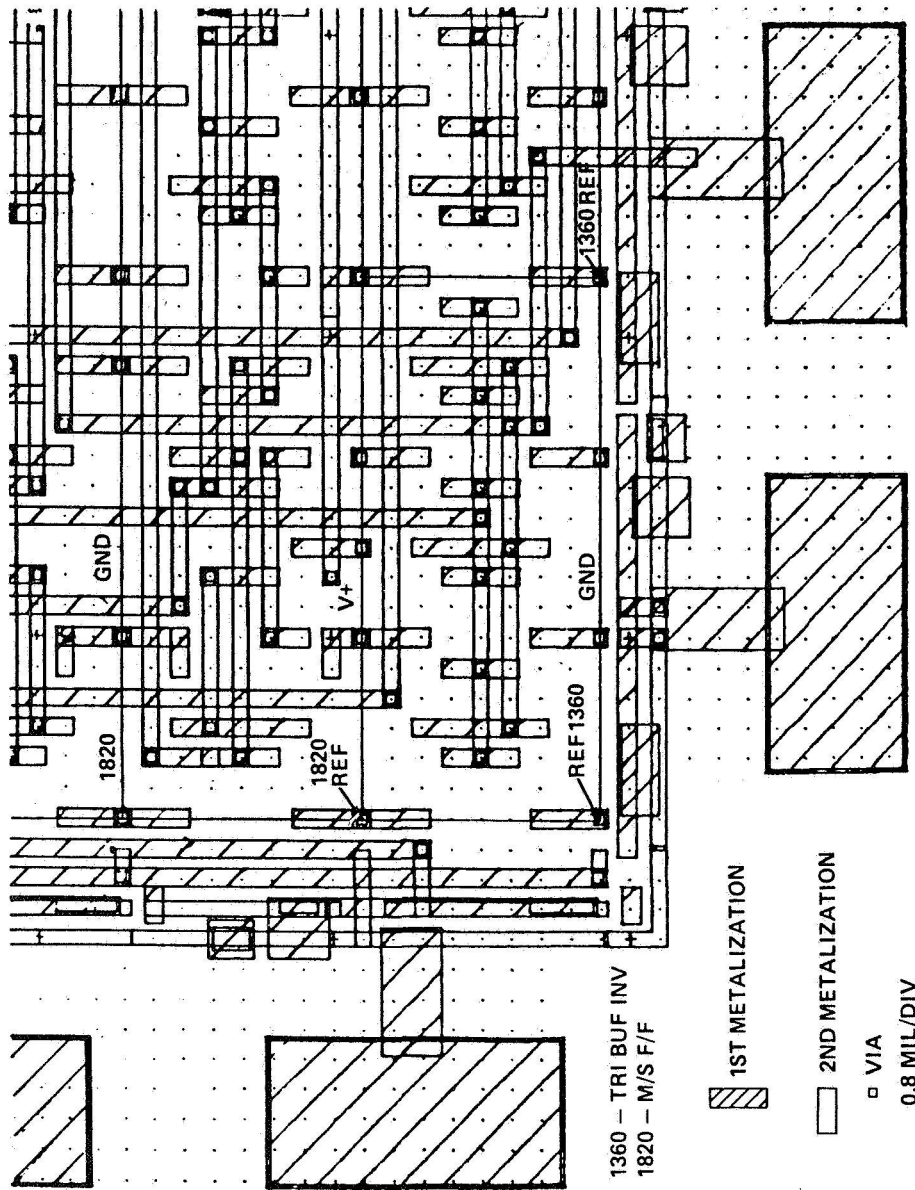


Figure 13. STAR cell placement and interconnection.

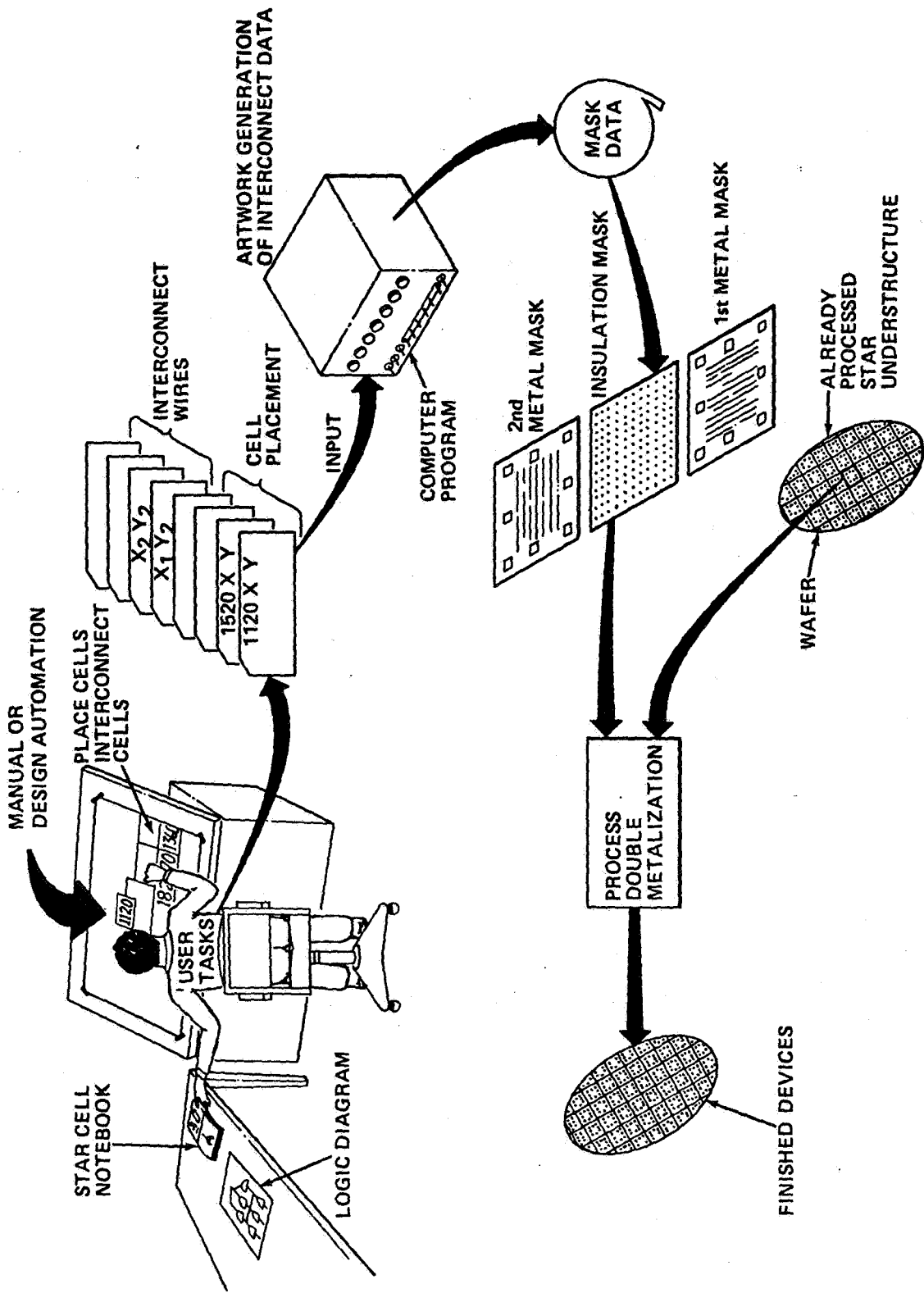


Figure 14. STAR operations.

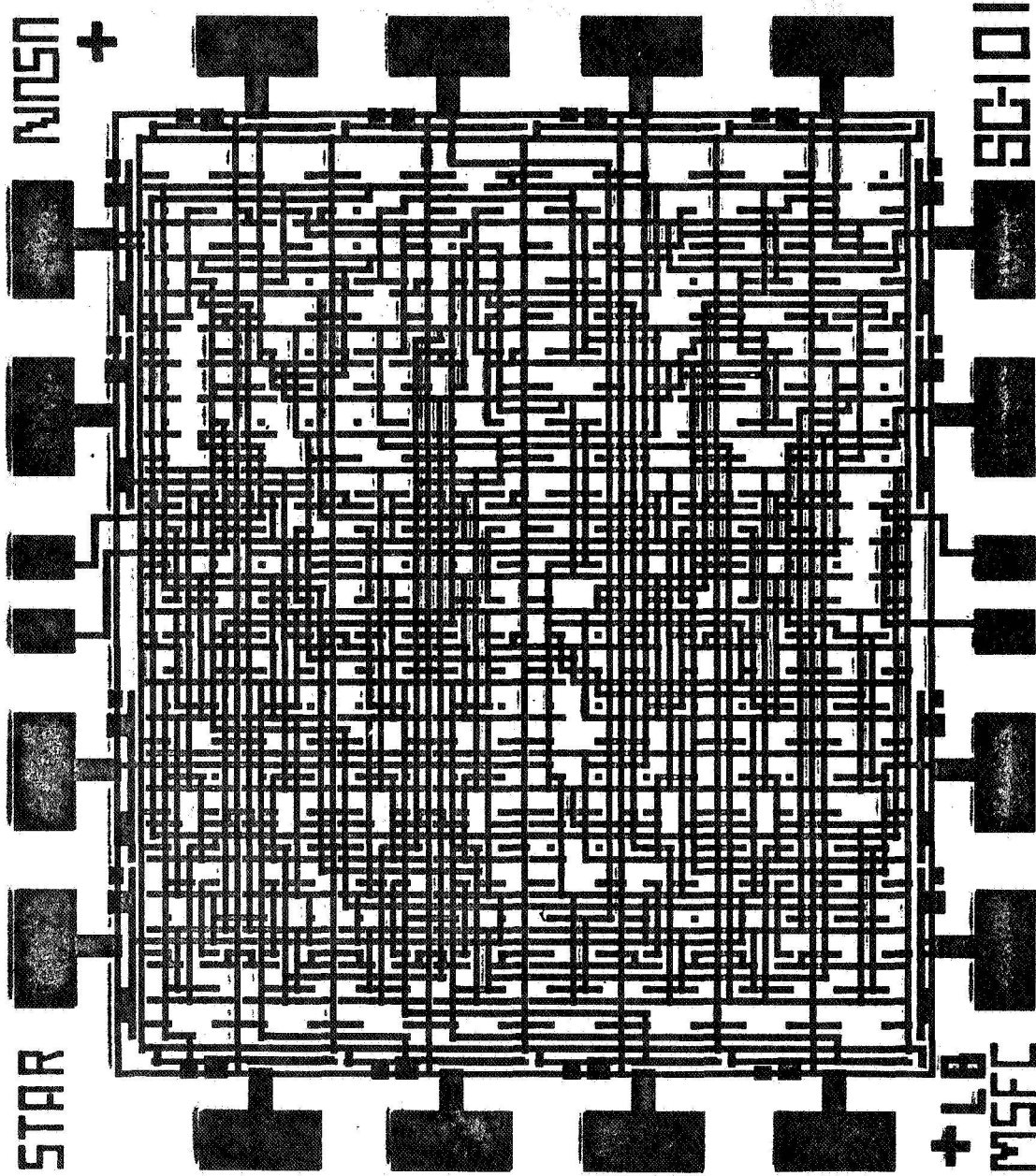


Figure 15. First and second metallization of layers of an MSFC heat source controller circuit.

CONCLUSION

The semicustom approach to integration is a commercially available option for the low volume user providing reduced cost, improved reliability, power reduction, secrecy, size reduction, and servicing ease.

The STAR approach to semicustom digital integrated circuits is intended to mix the best of both custom and semicustom. Emphasis is on ease of use, high device density, and flexibility with changing technologies. It is intended for those who feel the implementation and support of a complex custom design automation system is beyond their scope but have need for a semicustom integrating capability.