NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
WASHINGTON, D.C. 20546

MAR 14 1975

REPLY TO ATTN OF: GP

TO: KSI/Scientific & Technical Information Division
Attn: Miss Winnie M. Morgan

FROM: GP/Office of Assistant General Counsel for Patent Matters

SUBJECT: Announcement of NASA-Owned U.S. Patents in STAR

In accordance with the procedures agreed upon by Code GP and Code KSI, the attached NASA-owned U.S. Patent is being forwarded for abstracting and announcement in NASA STAR.

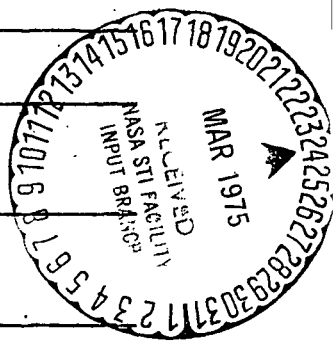
The following information is provided:

U.S. Patent No. : 3,866,022

Government or Corporate Employee : CalTech/JPL

Supplementary Corporate Source (if applicable) : Pasadena, CA

NASA Patent Case No. : NPO-13,125-1



NOTE - If this patent covers an invention made by a corporate employee of a NASA Contractor, the following is applicable:

YES [X] NO [ ]

Pursuant to Section 305(a) of the National Aeronautics and Space Act, the name of the Administrator of NASA appears on the first page of the patent; however, the name of the actual inventor (author) appears at the heading of column No. 1 of the Specification, following the words "...with respect to an invention of ..."

Bonnie L. Woerner

Bonnie L. Woerner
Enclosure

United States Patent [19]

Fletcher et al.

[11] **3,866,022**

[45] **Feb. 11, 1975**

[54] **SYSTEM FOR GENERATING TIMING AND CONTROL SIGNALS**

[76] Inventors: **James C. Fletcher**, Administrator of the National Aeronautics & Space Administration in respect to an invention by; **Marvin Perlman**, Granada Hills; **William J. Rousey**, Tujunga; **Alan Messner**, Monrovia, all of Calif.

[22] Filed: **Dec. 26, 1972**

[21] Appl. No.: **319,150**

[52] **U.S. Cl.** ..... **235/92 DM**, 235/92 R, 235/92 LG, 235/92 VA, 235/92 T

[51] **Int. Cl.** **H03k 21/36**

[58] **Field of Search** ..... 235/92 CC, 92 LG, 92 CP, 235/92 DM, 92 VA, 92 MC, 92 GT

[56] **References Cited**

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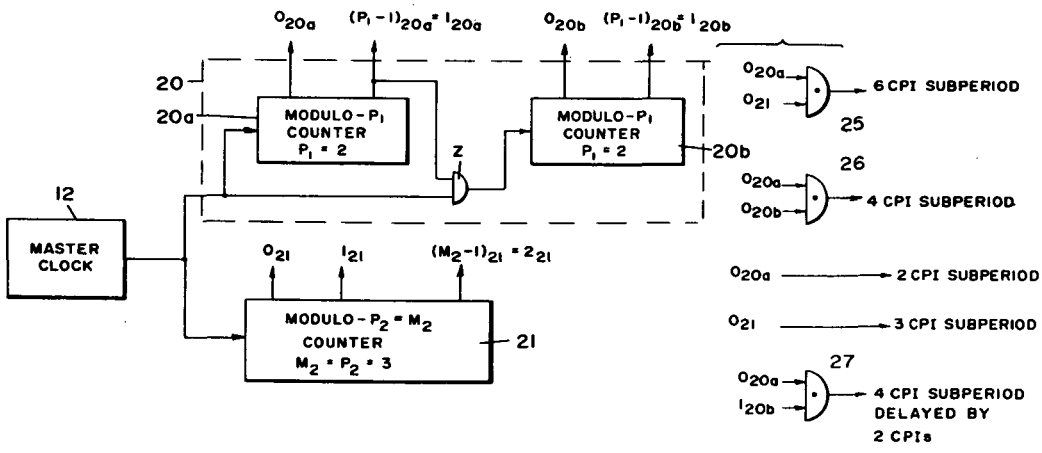
Primary Examiner—Gareth D. Shaw
Assistant Examiner—Robert F. Gnuse
Attorney, Agent, or Firm—Monte F. Mott; Paul F. McCaul; John R. Manning

[57] **ABSTRACT**

A system capable of generating every possible data frame subperiod and delayed subperiod of a data frame of length of M clock pulse intervals (CPIs) comprises parallel modulo-m_i counters. Each m_i is a prime power divisor of M. Each m_i is a cascade of α_i identical modulo-p_i counters, where $m_i = p_i^{\alpha_i}$. The modulo-p_i counters are feedback shift registers which cycle through p_i distinct states. By this organization, every possible nontrivial data frame subperiod (in terms of clock pulse intervals) and delayed subperiod may be derived. Also, a specific CPI in the data frame may be detected. The number of clock pulses required to bring every (or a subset of all) modulo-p_i counter to a respective designated state or count is determined by The Chinese Remainder Theorem. This corresponds to the solution of simultaneous congruences over relatively prime moduli.

9 Claims, 18 Drawing Figures



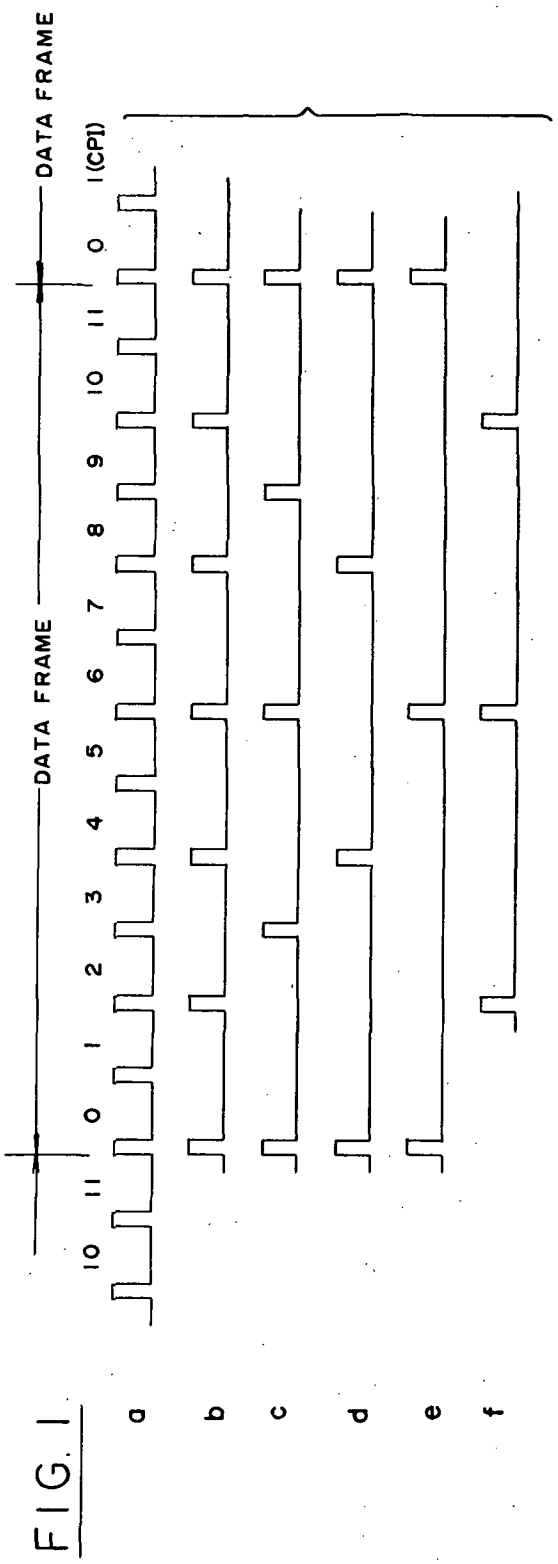


FIG. 1

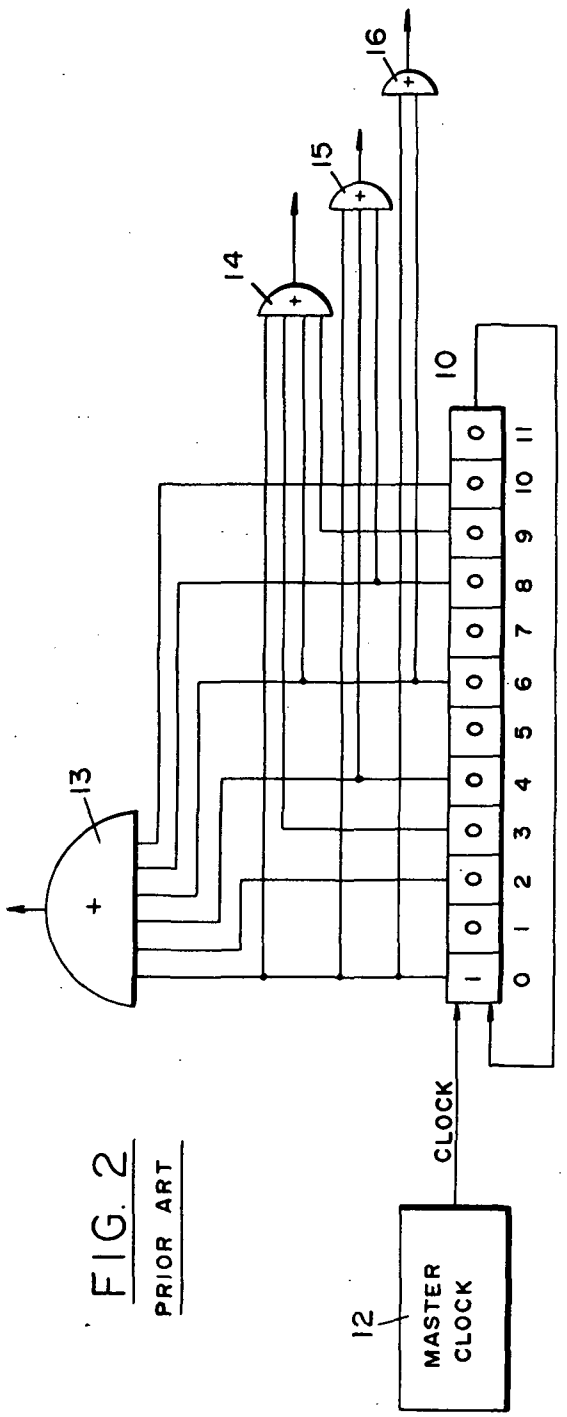


FIG. 2
PRIOR ART

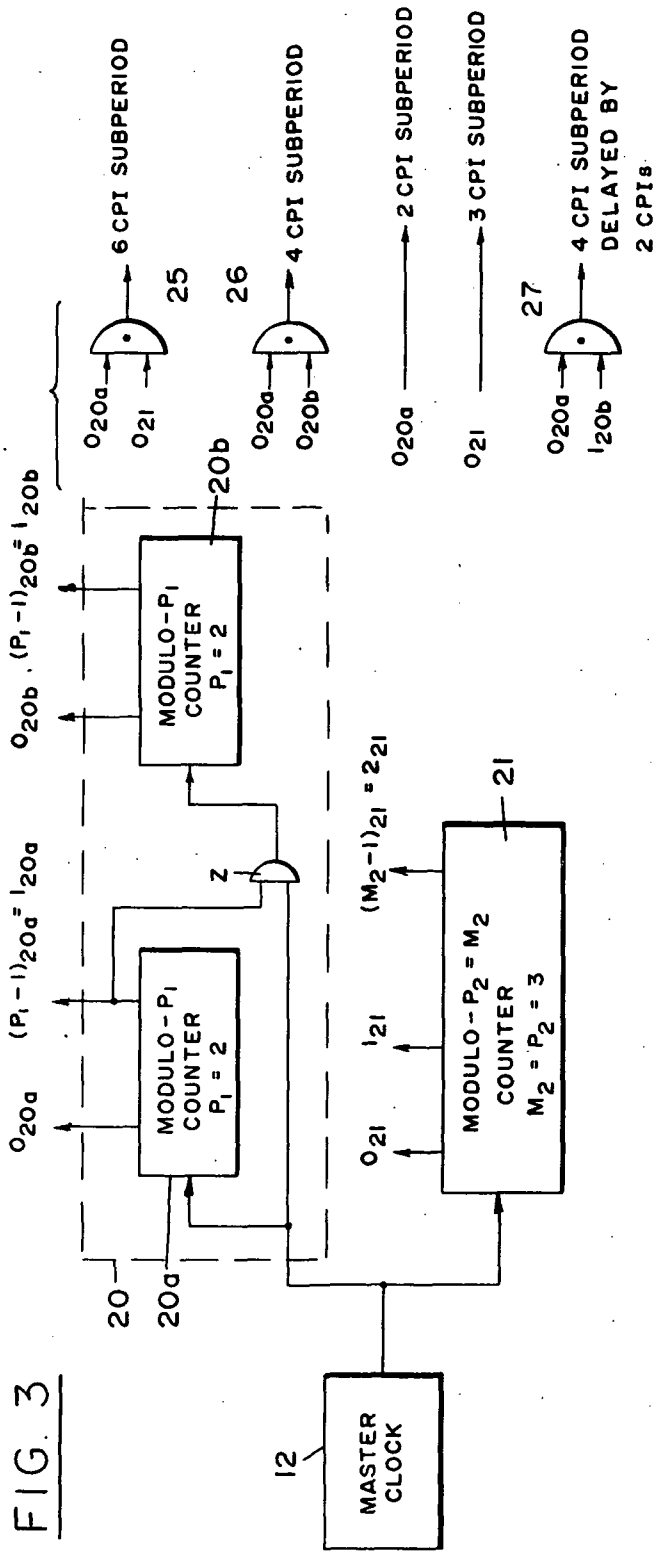

MASTER CLOCK
12
MODULO-P1 COUNTER P1 = 2
MODULO-P1 COUNTER P1 = 2
MODULO-P2 = M2 COUNTER M2 = P2 = 3
20
20a
20b
21
Z
6 CPI SUBPERIOD
4 CPI SUBPERIOD
2 CPI SUBPERIOD
3 CPI SUBPERIOD
4 CPI SUBPERIOD DELAYED BY 2 CPIs
25
26
27

FIG. 3

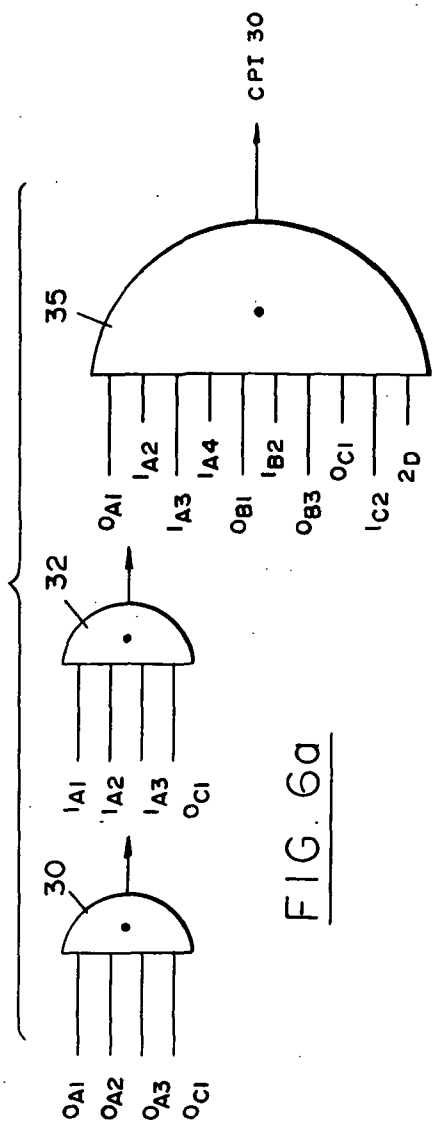

CPI 30
35
32
30

FIG. 6a

FIG. 4

CPI	STATE OF COUNTERS			
n	20a	20b	20	21
0	0	0	0	0
1	1	0	1	1
2	0	1	2	2
3	1	1	3	0
4	0	0	0	1
5	1	0	1	2
6	0	1	2	0
7	1	1	3	1
8	0	0	0	2
9	1	0	1	0
10	0	1	2	1
11	1	1	3	2
0	0	0	0	0
1	1	0	1	1

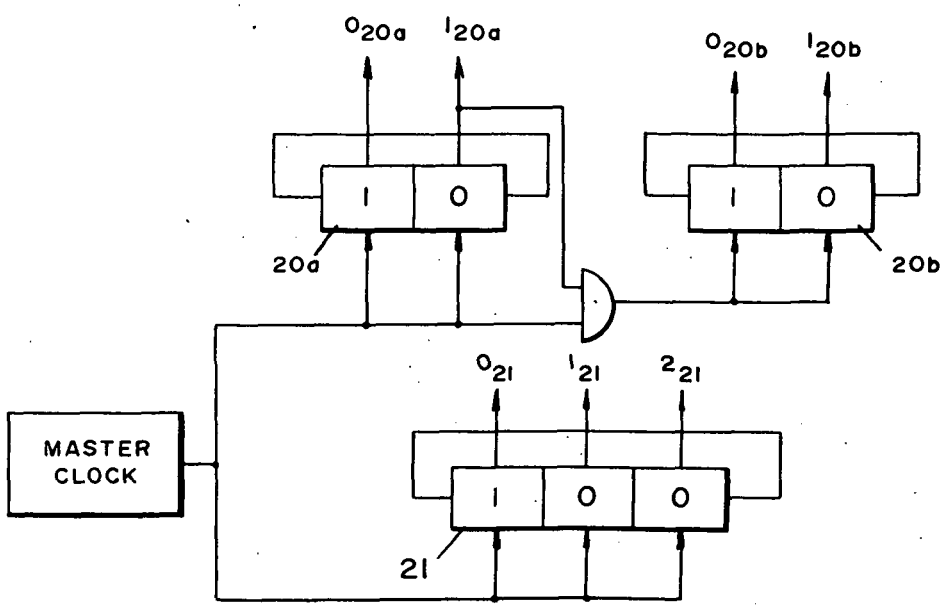


FIG. 5

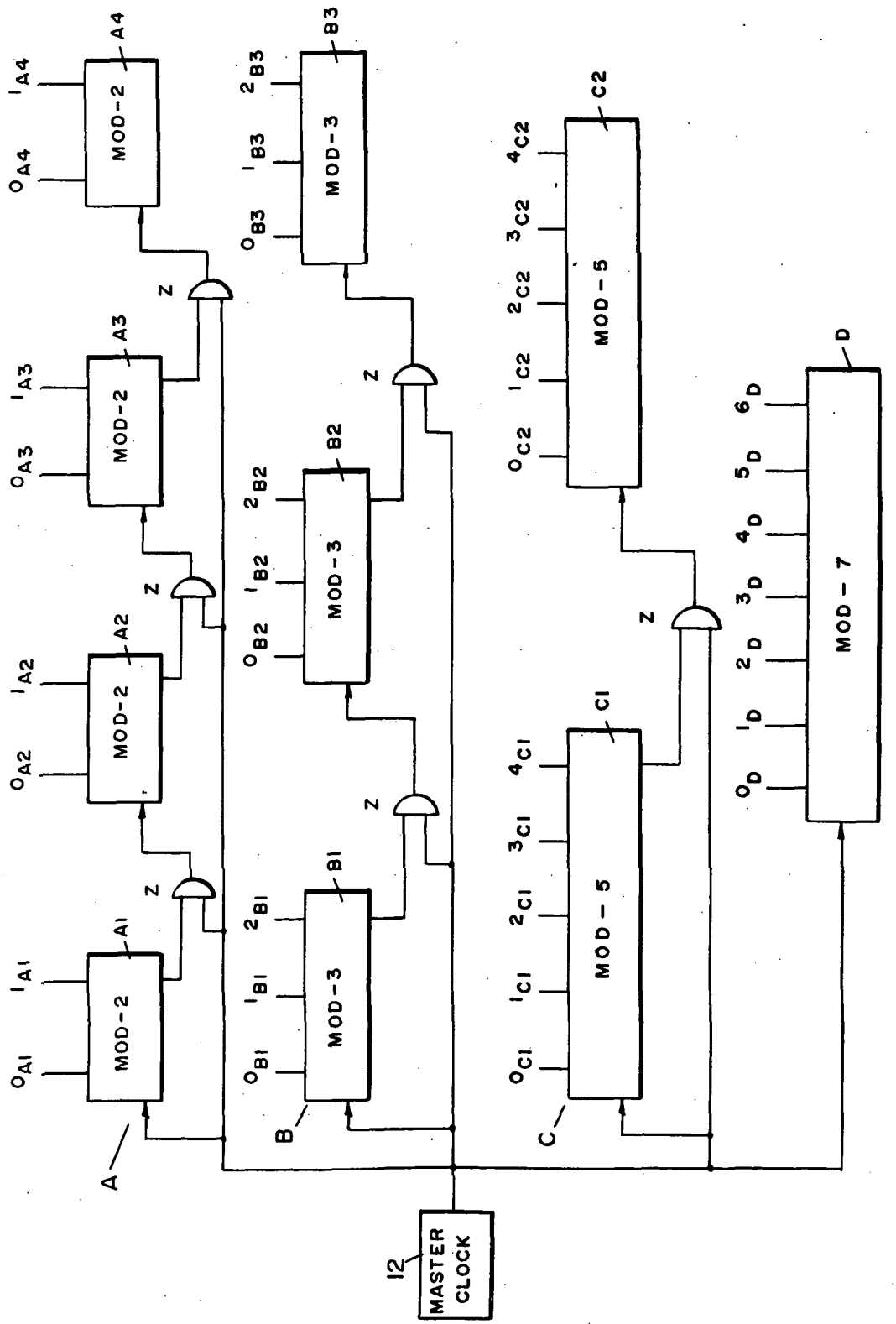


FIG.6

FIG. 7

CPI	A				B			C		D	MOD-4	MOD-8	MOD-16	MOD-9	MOD-27	MOD-25
n	A1	A2	A3	A4	B1	B2	B3	C1	C2	D	A1·A2	A1·A2·A3	A1·A2·A3·A4	B1·B2	B1·B2·B3	C1·C2
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	1	0	0	1	0	1	1	1	1	1	1	1
2	0	1	0	0	2	0	0	2	0	2	2	2	2	2	2	2
3	1	1	0	0	0	1	0	3	0	3	3	3	3	3	3	3
4	0	0	1	0	1	1	0	4	0	4	0	4	4	4	4	4
5	1	0	1	0	2	1	0	0	1	5	1	5	5	5	5	5
6	0	1	1	0	0	2	0	1	1	6	2	6	6	6	6	6
7	1	1	1	0	1	2	0	2	1	0	3	7	7	7	7	7
8	0	0	0	1	2	2	0	3	1	1	0	0	8	8	8	8
9	1	0	0	1	0	0	1	4	1	2	1	1	9	0	9	9
10	0	1	0	1	1	0	1	0	2	3	2	2	10	1	10	10
11	1	1	0	1	2	0	1	1	2	4	3	3	11	2	11	11
12	0	0	1	1	0	1	1	2	2	5	0	4	12	3	12	12
13	1	0	1	1	1	1	1	3	2	6	1	5	13	4	13	13
14	0	1	1	1	2	1	1	4	2	0	2	6	14	5	14	14
15	1	1	1	1	0	2	1	0	3	1	3	7	15	6	15	15
16	0	0	0	0	1	2	1	1	3	2	0	0	0	7	16	16
17	1	0	0	0	2	2	1	2	3	3	1	1	1	8	17	17
18	0	1	0	0	0	0	2	3	3	4	2	2	2	0	18	18
19	1	1	0	0	1	0	2	4	3	5	3	3	3	1	19	19
20	0	0	1	0	2	0	2	0	4	6	0	4	4	2	20	20
21	1	0	1	0	0	1	2	1	4	0	1	5	5	3	21	21
22	0	1	1	0	1	1	2	2	4	1	2	6	6	4	22	22
23	1	1	1	0	2	1	2	3	4	2	3	7	7	5	23	23
24	0	0	0	1	0	2	2	4	4	3	0	0	8	6	24	24
25	1	0	0	1	1	2	2	0	0	4	1	1	9	7	25	0
26	0	1	0	1	2	2	2	1	0	5	2	2	10	8	26	1
27	1	1	0	1	0	0	0	2	0	6	3	3	11	0	0	2
28	0	0	1	1	1	0	0	3	0	0	0	4	12	1	1	3
29	1	0	1	1	2	0	0	4	0	1	1	5	13	2	2	4
30	0	1	1	1	0	1	0	0	1	2	2	6	14	3	3	5
31	1	1	1	1	1	1	0	1	1	3	3	7	15	4	4	6
32	0	0	0	0	2	1	0	2	1	4	0	0	0	5	5	7
33	1	0	0	0	0	2	0	3	1	5	1	1	1	6	6	8

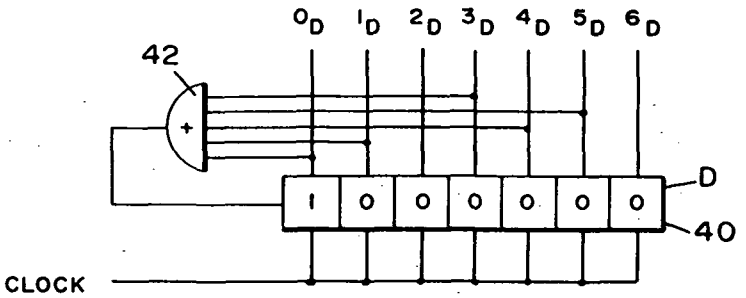


FIG. 8

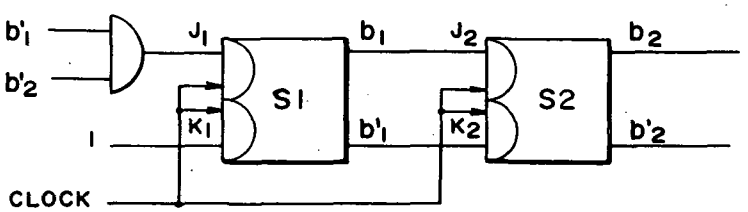


FIG. 9a

FIG. 9b

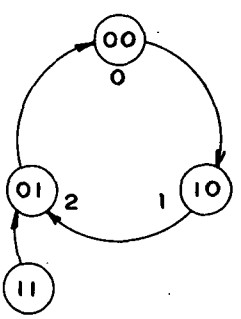


FIG. 9c

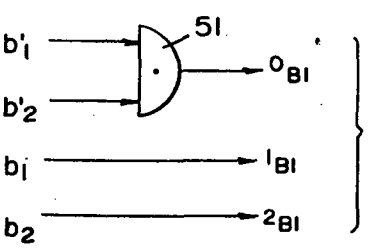


FIG. 10a

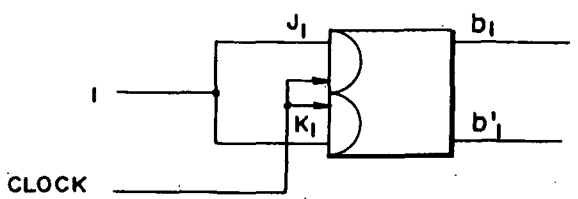


FIG. 10b

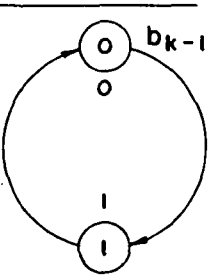
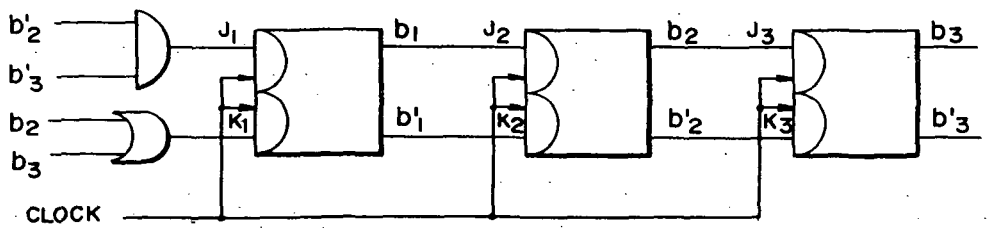


FIG. 11a



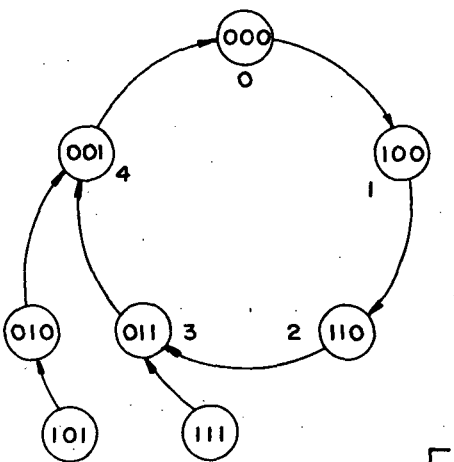
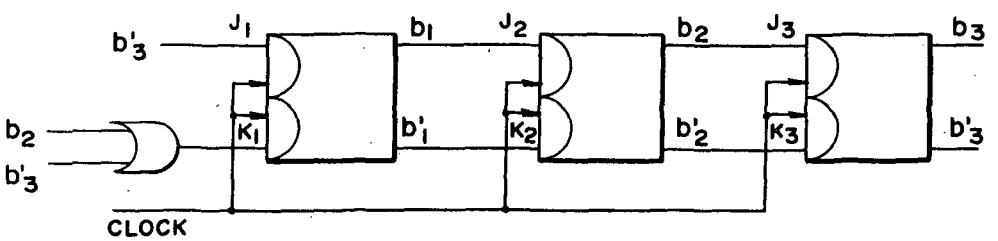


FIG. 11b

FIG. 12a



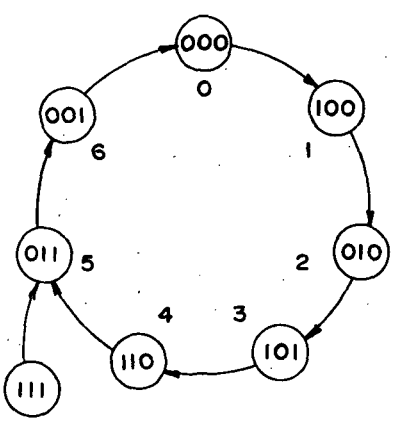


FIG. 12b

SYSTEM FOR GENERATING TIMING AND CONTROL SIGNALS

ORIGIN OF INVENTION

The invention described herein was made in the performance of work under a NASA contract and is subject to the provisions of Section 305 of the National Aeronautics and Space Act of 1958, Public Law 85-568 (72 Stat. 435; 42 USC 2457).

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention is generally related to a system for generating timing and control signals and, more particularly, to a system for generating timing and control signals during each fixed length serial data frame which is repetitive.

2. Description of the Prior Art

There are many applications in which it is necessary to provide different timing and control signals for controlling different experiments or operations, yet insure that all of the signals are synchronized to a master clock. Assuming that all the experiments occur at different subperiods of a master data frame of length which is equal to a fixed number of intervals, defined as M, of clock pulses from the master clock in theory a modulo-M counter which is clocked by the master clock can be used. As the counter is sequenced through its M states, selected ones of the states may be used to produce specific timing signals from the start of the frame as well as define specific subperiods of the frame. However, if M is very large and the clocking frequency is high, severe propagation delays and ripple problems are encountered. These can only be overcome by a large amount of logic circuits which greatly increases the complexity and cost of the system. Thus, a need exists for a new system to generate timing or control signals which define subperiods or delayed subperiods of a master data frame of clock pulse length M.

OBJECTS AND SUMMARY OF THE INVENTION

It is a primary object of the present invention to provide a new system for generating synchronized timing and control signals.

Another object of the invention is to provide a new system for generating selected subperiods and/or delayed subperiods of a master data frame of a fixed number of clock pulses.

A further object of the invention is to provide a system of minimum complexity which is capable of providing all subperiods and delayed subperiods of a relatively long fixed-length data frame.

These and other objects of the invention are achieved for a data frame of length M by providing a plurality of modulo-m_i counters which are clocked in parallel by a master clock. Each m_i is a prime power divisor of M, other than 1 and M. Each modulo-m_i counter is a cascade of α_i identical modulo-p_i counters where $m_i = p_i^{\alpha_i}$. Each p_i is a distinct prime of M, and each α_i is an integer not less than 1. Each of the modulo-P_i counter cycles through p_i distinct states. By detecting selected states of the p_i counters of the various m_i counters every non-trivial data frame subperiod and delayed subperiod may be determined with a minimum of logic and complexity.

The novel features of the invention are set forth with particularity in the appended claims.

The invention will best be understood from the following description when read in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a multiline clock pulse waveform diagram;

FIG. **2** is a block diagram of a prior art arrangement;

FIG. **3** is a block diagram useful in explaining one example of an embodiment of the present invention;

FIG. **4** is a state table of the counters shown in FIG. **3**;

FIG. **5** is a diagram of the embodiment shown in FIG. **3** and implemented with ring counters;

FIGS. **6** and **6***a* are diagrams useful in explaining another embodiment of the invention;

FIG. **7** is a state table of the counters shown in FIG. **6**;

FIG. **8** is a diagram of counter D shown in FIG. **6** as a ring counter;

FIGS. **9***a*, **9***b* and **9***c* are diagrams of a 2-stage modulo-3 FSR, its state cycle and decision logic;

FIGS. **10***a* and **10***b* are diagrams of a 1-stage modulo-2 FSR and its state cycle;

FIGS. **11***a* and **11***b* are diagrams of a 3-stage modulo-5 FSR and its state cycle; and

FIGS. **12***a* and **12***b* are diagrams of a 3-stage modulo-7 FSR and its state cycle.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention may best be described in connection with two specific examples and thereafter generalized for the most general cases.

Attention is first directed to FIG. **1** wherein in line *a*, a succession of clock pulses each of a fixed clock pulse interval (CPI) is diagrammed. Let it be assumed that the period of a data frame is defined by M CPIs, which in line *a* is assumed to be 12. The 12 CPIs are designated 0–11. Let it further be assumed that during the data frame various experiments are conducted which require control signals at different subperiods of the data frame, such as subperiods of 2, 3, 4 and 6 CPIs in length. Such subperiods are diagrammed in lines *b* through *e*, respectively.

It is clear to those familiar with the art that such subperiods may be defined by a modulo-M counter where M=12 which is clocked by the master clock and which advances through 12 states, 0–11. With the addition of decision logic, the subperiod of 2 CPIs can be defined by generating a pulse when the counter is in states 0, 2, 4, 6, 8, 10, 0 etc., while the subperiod of 3 CPIs can be generated by producing a pulse each time the counter is in states 0, 3, 6, 9, 0 etc.

One way of generating such subperiods is to employ a 12-stage ring counter, in which all stages store a binary 0 except one stage which stores a binary 1, so that as the counter is clocked the binary 1 shifts from one stage to the next. By connecting stages 0, 2, 4, 6, 8 and 10 to one OR gate, this gate would provide a true output which represents a pulse each time any of these stages stores the binary 1 thereby defining the start of each subperiod of 2 CPIs (line *b*). Similarly, the other subperiods can be defined in a similar way. Such an arrangement is shown in FIG. **2** wherein the 12-stage ring counter is designated by numeral 10, the master clock

by numeral 12 and the four gates which produce output pulses which define subperiods of 2, 3, 4 and 6 CPIs by numerals 13–16, respectively. The ring counter is shown in state 0.

It should be obvious that even in this simple example 12 memory stages or units of counter **10** are needed. Clearly as M increases, which in many practical applications may be equal to several millions, an extremely large number of memory units is needed. This greatly increases the cost and complexity of the system needed to generate the subperiods. The number of memory units may be reduced by replacing the ring counter with a minimum stage feedback shift register (FSR) at the cost of increased decision complexity. For example, a 4-stage FSR may be used and operated to cycle only through 12 states rather than through $2^4 = 16$ states. However, decision logic would be required to define each of the 12 states in terms of the binary states of the 4 stages.

The present invention provides a completely new approach to generating such subperiods and delayed subperiods as will be described hereafter. In accordance with the present invention, any modulo-M counter of clock pulses is decomposed into parallel modulo-m_i counters, where each m_i is a prime power divisor (or factor) of M. Each m_i counter is implementable as a cascade of α_i identical modulo-p_i counters, where $m_i = p_i^{\alpha_i}$, p_i is one of the distinct primes of M, and α_i is an integer at least equal to one. Each modulo-p_i counter cycles through p_i distinct states. The combination of the states of the α_i identical modulo-p_i counters cycle through m_i states. In a system, comprising such an organization, every possible non-trivial data frame subperiod in terms of CPIs and delayed subperiods may be derived.

The principles of the invention will now be described assuming $M = 12$. Unique factorization except for order gives:

$$M = 2^2 \cdot 3^1$$

Let

$$M = m_1 m_2$$

where

$$m_1 = 2^2 = 4$$

$$m_2 = 3^1 = 3$$

The arrangement of m_i factors is arbitrary as long as pair-wise relative primeness holds. This is guaranteed by the unique factorization into products of powers of distinct primes, where each distinct prime power corresponds to an m_i. Furthermore, prime power factorization enables one to enumerate all divisors of M. It is clear that $m_1 = 4$ and $m_2 = 3$ are the prime power factors of $M = 12$ and that 2 and 3 are the two distinct primes of $M = 12$.

Let

$$p_1 = 2 \text{ and } p_2 = 3$$

The following polynomial factors, when multipled, yield terms which correspond to every divisor of M.

$(1 + p_1 + p_1^2)(1 + p_2)$ The number of terms in the resulting polynomial is

$$(2 + 1)(1 + 1) = 6$$

Thus, there are six divisors of M, four of which are proper, with 1 and M being the improper divisors. It is clear that the four proper divisors of $M = 12$ are 2, 3, 4 and 6.

In accordance with the present invention for $M = 12$, two parallel modulo-m_i counters are provided. One counter is a modulo-m_1 counter and the other is a modulo-m_2 counter. Since $m_1 = 4$ and $m_2 = 3$, the counters area of modulo-4 and modulo-3. Such an arrangement is shown in FIG. **3** in which the two counters are designated by numerals **20** and **21**, respectively.

As previously pointed out, each m_i counter is decomposed into α_i modulo-p_i counters, where $m_i = p_i^{\alpha_i}$. In the case of m_1, since $m_1 = p_1^2 = 2^2$, it is decomposed into 2 modulo-$p_i = 2$ counters, which in FIG. **3** are designated as **20***a* and **20***b*. However, since $m_2 = p_2^1 = 3^1$ it is represented by a single modulo-3 counter **21**.

Each counter is shown with a plurality of output lines each of which is assumed to be true or high hereafter also referred to as being at a 1 level when the counter is at the state corresponding to the line designation. It is obvious that each of counters **20***a* and **20***b* being a modulo-2 counter, cycles through 2 states 0 and 1, while counter **21** being a modulo-3 counter cycles through 3 states 0, 1 and 2. The counters **20** and **21** are synchronously clocked by master clock **12**. In counter **20**, the leftmost counter **20***a* is clocked directly from clock **12**. However, the next counter **20***b* is clocked only when counter **20***a* changes from its highest state which is 1 to its lowest state which is 0. This is achieved by incorporating a logic element represented by gate Z. Basically, it permits counter **20***b* to be clocked by a clock pulse from master clock **12** only when line 1_{20a} changes from high to low which occurs only when counter **20***a* changes from state 1 to state 0. Assuming that all the counters are at state 0 at the first CPI of the data frame which is designated as $n = 0$, the states of the counters at the other 11 CPIs is as shown in the state table of FIG. **4**.

In accordance with the present invention, any subperiod of $M = 12$ can be derived from these three counters. For example, to obtain a subperiod of 6, since $6 = 2 \cdot 3$, the start of each subperiod is provided by detecting the instance when both counters **20***a*, which is a mod-2 counter and counter **21** which is a mod-3 counter are at the 0 state. This can easily be accomplished by means of an AND gate **25** which is connected to lines 0_{20a} and 0_{21}, as shown in FIG. **3**. It is clear from FIG. **4** that both of these counters are at state 0 only at $n = 0$ and $n = 6$. To obtain a subperiod of 3, all that is necessary is to detect a high level at line 0_{21} which occurs only every third CPI. To obtain a subperiod of 4 CPIs, since modulo-4 counter **20** is decomposed into 2 counters **20***a* and **20***b*, the outputs of both of these counters need be detected. This is easily achieved by ANDing the output lines 0_{20a} and 0_{20b} in an AND gate **26**.

As seen from FIG. **4**, even though each of counters **20***a* and **20***b* cycles through only states 0 and 1, their combined outputs **00, 10, 01** and **11** represent the four states 0, 1, 2 and 3 respectively, of counter **20**, as shown in the second column from the right in FIG. **4**. It is thus seen that the arrangement shown in FIG. **3** is capable of providing any subperiod of $M = 12$.

Defining the subperiod by M' any subperiod may be delayed from the start of the frame by up through $M' - 1$ CPIs. For example, let it be assumed that it is desired to provide a subperiod of 4 CPIs which starts 2 CPIs

after the start of the data frame, i.e., at $n = 2$ as diagrammed in line *f* of FIG. **1.**

$$2 \equiv 2 \bmod 4$$

Consequently, state 2 of the mod-4 counter has to be detected. This state is represented by the combined states of 0 and 1 counters **20***a* and **20***b*, respectively. Thus, by ANDing lines 0_{20a} and 1_{20b} by gate **27**, as shown in FIG. **3**, a pulse is produced at $n = 2$ which indicates the start of the first 4-CPI subperiod and thereafter every 4 CPIs such as at $n = 6$ and $n = 10$. This is shown in FIG. **4**.

Assuming that a subperiod of 6 CPIs is desired which is delayed by 4 CPIs, since

$$6 = 2 \cdot 3$$

$$4 \equiv 0 \bmod 2$$

$$4 \equiv 1 \bmod 3$$

Thus, by ANDing output lines 0_{20a} of modulo-2 counter **20***a* which is high at state 0 with line 1_{21} which is high at state 1 of mod-3 counter **21** a first pulse is produced at $n = 4$, and thereafter every 6th CPI such as at $n = 10$.

It is thus seen that with the present system any delayed subperiod may be generated. As will be pointed out hereafter, the system may be used to detect a particular CPI in the data frame. However, this point may better be highlighted later with an example in which M is very large and the system includes a large number of parallel modulo-m_i counters.

FIG. **5** to which reference is now made is a block diagram of the arrangement of FIG. **3** implemented with simple ring counters all of which are shown in state 0. As seen, counter **21** which is a mod-3 counter, is implemented by a three-stage ring counter, while each of counters **20***a* and **20***b* is implemented by a two-stage ring counter. It is thus seen that only $3 + 2 + 2 = 7$ memory stages are required for $M = 12$ as compared with the requirement of a 12-stage ring counter as shown in FIG. **2**.

The advantages of the invention becomes more apparent when M is large. Let

$M = 75{,}600$

Unique factorization except for order gives

$M = 2^4\ 3^3\ 5^2\ 7^1$

Let

$M = m_1\ m_2\ m_3\ m_4$

where

$m_1 = 2^4 = 16$

$m_2 = 3^3 = 27$

$m_3 = 5^2 = 25$

$m_4 = 7^1 = 7$

Also, let $p_1 = 2$, $p_2 = 3$, $p_3 = 5$ and $p_4 = 7$, thus

$m_1 = p_1^4$

$m_2 = p_2^3$

$m_3 = p_3$

$m_4 = p_4^1$ It is obvious that $p_1 - p_4$ are the distinct primes and $m_1 - m_4$ are the prime power factors of M. It can be shown that the number of proper divisors of M is

$$(1+p_1+p_1^2p_1^3+p_1^4)(1+p_2+p_2^2+p_2^3)(1+p_3+p_3^2)(1+\mathbf{p}_1)$$

The number of terms in the resulting polynomial is

$$(1+4)(1+3)(1+2)(1+1) = 120$$

Thus, the total number of divisors is 120, 118 of which are proper.

To obtain all possible 118 subperiods of M four modulo-m_i counters are clocked in parallel. One counter is of modulo-m_1 = modulo-16. Another counter is of modulo-m_2 = modulo-27. The third counter is of modulo-m_3 = modulo-25 and the fourth counter is of modulo-m_4 = modulo-7. Since $m_1 = p_1^4 = 2^4$, the modulo-m_1 counter is decomposed into a cascade of 4 modulo-2 counters. Likewise, since $m_2 = p_2^3 = 3^3$, the modulo-m_2 counter is decomposed into a cascade of 3 modulo-3 counters. Following the same process since $m_3 = p_3^2 = 5^2$, the modulo-m_3 counter is decomposed into a cascade of 2 modulo-5 counters. As to the last counter since $m_4 = p_4^1 = 7^1$, it is represented by a single modulo-7 counter. Such an arrangement is shown in FIG. **6** wherein the four counters are designated as A, B, C and D. Counter A, which is the modulo-m_i counter is shown comprising of four counters A1–A4 each of modulo-2, counter B which is the modulo-m_2 counter is shown comprising 3 counters B1–B3 each of modulo-3 and counter C which is the modulo-m_3 counter is shown comprising 2 counters C1 and C2, each of modulo-5.

It is apparent to those familiar with the art that counters of modulo-2, modulo-3, modulo-5 and modulo-7, cycle through 2, 3, 5 and 7 states hereafter designated **01, 012, 0, 1, 2, 3, 4** and **0, 1, 2, 3, 4, 5** and **6** respectively. As in the arrangement shown in FIG. **3**, the leftmost counter of each of counters A–D in FIG. **6**, is closed in synchronism, thereby changing state by each clock pulse. However, each succeeding counter in a chain, such as counter A2 of counter A or counter B2 of counter B is clocked only when the preceding counter in the chain, such as A1 or B1 changes from its highest state such as 1 or 2 to its lowest state 0. This is achieved by the inclusion of gates Z.

In operation, all the counters are reset to their 0 states when the first CPI of the frame, i.e., CPI $n = 0$ is received. It is obvious that different means may be used to reset all counters to their 0 state. Thereafter the counters cycle through their different states as they are clocked by the master clock **12**. Their states during CPI $n = 0$ through $n = 33$ are listed in FIG. **7**. It is clear that the combined states of A1 and A2 form a 4-state sequence, the combined states of A1, A2 and A3 form a 8-state sequence and the combined states of A1, A2, A3 and A4 form the 16-state sequence of counter A. Also, the combined states of B1 and B2 form a 9-state sequence and they together with B3 form the 27-state sequence of counter B. Likewise, the states of counters C1 and C2 form the 25-state sequence of counter C. These sequences are also listed in FIG. **7**.

Several of the following examples will indicate that any of the 118 subperiods of M may be obtained by the arrangement of FIG. **6**.

EXAMPLE 1

Let it be assumed that CPI$x = 0 + k40$ for $k = 0, 1 \ldots$, is to be generated. That is, *M* is to be divided into equal subframes of length **40**. Let the subperiod of **40** be designated by *M'*. *Thus*

$$M' = 40 = 2^3 \cdot 5^1$$

Thus, the outputs of a mod-2^3 counter and a mod-5 counter need be combined. In the present invention, a mod-2^3 counter is represented by combining the outputs of the leftmost 3 counter A1–A3 of counter A. The single mod-5 counter is represented by the leftmost counter C1 of counter C. Thus, when all of these counters are at the 0 state, a pulse should be produced.

This can be easily achieved by ANDing the output lines 0_{A1}, 0_{A2}, 0_{A3} and 0_{C1} in an AND gate **30** shown in FIG. **6***a*. This gate will provide a true output representing a pulse for every 40 pulses of the master clock.

The first output pulse of a subperiod of **40** may be delayed by up to $40 - 1 = 39$ pulses. Assume that the first pulse is to be delayed by 15 CPIs.

$$15 \equiv 7 \bmod 2^3 \equiv 7 \bmod 8 \equiv 0 \bmod 5$$

As seen from FIG. **7** at $n = 15$ state **7** of the mod-8 counter is represented by an all **1** state in each of counters **A1**, **A2** and **A3** while the mod-5 counter represented by counter **C1** is at state 0. Thus, to delay the subperiod of **40** by 15 CPIs, output lines 1_{A1}, 1_{A2}, 1_{A3}, and 0_{C1} are ANDed by an AND gate **32** (see FIG. **6***a*). It would provide the first pulse at $n = 15$ and thereafter every 40 CPIs.

In the above expression let the states of 7 and 0 in the mod-8 and mod-5 counter be designated by $\hat{a}_1$ and $\hat{a}_2$ respectively. It can generally be stated that the subperiod M' can be delayed by up to $M' - 1$ CPIs by detecting a particular nonzero combination of $\hat{a}_1$ $\hat{a}_2$ in the modulo-8 and modulo-5 counters, respectively. In the above example, it is 7, 0. However, other combinations of nonzero states will be present for different delays of the subperiod of **40**. The maximum delay is $40 - 1 = 39$ CPIs.

EXAMPLE 2

Assuming that the states of the mod-8 and the mod-5 counters are 4 and 2, respectively, the delay in terms of CPIs designated X can be determined by the Chinese Remainder Theorem.

$X \equiv 4 \bmod 8$, where $\hat{a}_1 = 4$
$\equiv 2 \bmod 5$, where $\hat{a}_2 = 2$
$M_1 = 40/8 = 5$
$M_2 = 40/5 = 8$
$5y_1 \equiv 1 \bmod 8$
$8y_2 \equiv 1 \bmod 5$

Unique solutions of y_1 and y_2 are 5 and 2, respectively.

$X \equiv (a_1 y_1 M_1 + a_2 y_2 M_2) \bmod 40$
$\equiv (4 \cdot 5 \cdot 5 + 2 \cdot 2 \cdot 8) \bmod 40$
$\equiv 132 \bmod 40$
$\equiv 12 \bmod 40$

Check

$12 \equiv 4 \bmod 8$

and

$12 \equiv 2 \bmod 5$

Thus, the first time that the states 4 and 2 will appear in the mod-2^3 and mod-5 counters is $n = 12$. That this indeed is the case in the present invention is apparent from FIG. **7**. As seen at $n = 12$, the states of **A1**, **A2**, **A3** are **001** which represent state 4 in the mod-2^3 counter and the mod-5 counter **C1** at $n = 12$ is at state 2.

EXAMPLE 3

Let it be assumed that CPI **30** must be identified as $M = 75{,}600$. Since $M = 2^4\ 3^3\ 5^2\ 7^1 = 16 \cdot 27 \cdot 25 \cdot 7$

$30 \equiv 14 \bmod 16$
$\equiv 3 \bmod 27$
$\equiv 5 \bmod 25$
$\equiv 2 \bmod 7$

Thus, CPI **30** occurs when counters A, B, C, and D are in states 14, 3, 5 and 2, respectively. That this is indeed the case is seen from FIG. **7**. At $n = 30$, state 14 of counter A is represented by **0111** of counters **A1** –**A4**. State **3** of counter B is represented by states **010** of counters **B1** – **B3**, and state **5** of counter C is represented by states **01** of counters **C1** and **C2**. Counter D is at state **2**. Thus, by ANDing output lines 0_{A1}, 1_{A2}, 1_{A3}, 1_{A4}, 0_{B1}, 1_{B2}, 0_{B3}, 0_{C1}, 1_{C2} and 2_D in gate **35** as shown in FIG **6***a*, this gate will provide a true output only at $n =$ 30 of each frame.

EXAMPLE 4

Assume that CPI 2000 of $M = 75{,}600$ is to be identified. Since $M = 16 \cdot 27 \cdot 25 \cdot 7$

$2000 \equiv 0 \bmod 16$
$\equiv 2 \bmod 27$
$\equiv 0 \bmod 25$
$\equiv 5 \bmod 7$

Thus, CPI 2000 occurs when counters A, B, C and D are at states 0, 2, 0 and 5 respectively. These states are represented by state 0000 of **A1** – **A4**, state 200 of **B1** – **B3**, state 00 of **C1** and **C2** and state 5 of D. Thus, CPI can be detected by ANDing lines 0_{A1}, 0_{A2}, 0_{A3}, 0_{A4}, 2_{B1}, 0_{B2}, 0_{B3}, 0_{C1}, 0_{C2} and 5_D in an appropriate AND gate (not shown).

From the foregoing, it is thus seen that the arrangement of FIG. **6** for $M = 75{,}600$ is capable of providing any of **118** subperiods of M as well as any delayed subperiod. It is further capable of being used to identify any particular CPI in the frame. Furthermore, based on the states of the counters A, B, C and D, the CPI at which such states occur can be determined by the Chinese Remainder Theorem. It should be apparent that any of the counters A – D can be implemented with ring counters. Counter A requires 4 2-stage ring counters, counter B requires 3 3-stage ring counters and counter C requires 2 5-stage ring counters. Counter D is a single 7-stage ring counter. Thus, a total of 34 stages are needed. This compares with 75,600 stages that would be required in the prior art if it were implemented by a 75,600-stage ring counter. Also, with the present invention, a minimum amount of decision logic is needed. The largest AND gate necessary is one with 10 inputs. In the prior art, to obtain a subperiod of 2 CPIs from a ring counter of 75,600 stages, a gate with 37,800 inputs is needed.

It should be apparent that any of the counters shown in FIG. **6** may be implemented as a multistage ring counter. For example, counter D may be implemented by a 7-stage ring counter, designated by numeral **40** in FIG. **8**. It is shown in state 0 since a binary 1 is shown stored in the leftmost stage and all the other stages store binary 0's. As the counter is clocked, the 1 advances from stage to stage thereby cycling the counter through its states.

Conventionally, the output of the last stage is fed back to the first stage. Preferably, however, the assertion outputs of all the stages except the last are connected to a NOR gate **42**, whose output is connected to the input of the first stage. This insures proper setting of the counter after not more than one complete cycle. As long as any of the first five stages holds a 1, a 0 is stored in the first stage. Only when all the first five stages store 0's is a 1 stored in the first stage at the next clock period.

In the present invention, when the system is turned on, all the ring counters are reset to their 0 states by storing 1's in the first stages of the various counters. Thereafter, the shifting of the 1's in the counter is accomplished by clocking the counters with the pulses

from the master clocks. If during turn on, any stage except the first stage is inadvertently set to binary 1 state, the error will be eliminated after the first complete cycle by means of NOR gate **42**. If the negation outputs of all the stages, except the last, are used, NOR gate **42** is replaced by a AND gate.

As previously pointed out, the modulo-p_i counters shown in FIG. **6** need not be limited to ring counters. They may be implemented by minimum stage feedback shift registers (FSRs). This may result in fewer memory cells at the price of more complex decision logic. For example, each of the counters **B1**, **B2** and **B3** which is a modulo-3 counter may be implemented by a 2-stage FSR, interconnected to cycle through 3 states. The unused state is always driven into the desired cycle of states.

FIG. **9***a* is a block diagram of a 2-stage FSR which cycles through **3** states, as shown in FIG. **9***b*. It is assumed to represent counter **B1**. The two stages of the FSR are designated by **S1** and **S2**. Each is a 1-enable JK flip flop whose characteristic equation is $Q = J_q' + K'_q$ where J and K are 1-enable inputs, q and Q are the present and next state, respectively and the ' designates complementation.

As seen from FIG. **9***b*, the combined states of **S1** and **S2** of **00**, **10** and **01** represent states 0, 1 and 2 of the FSR acting as a modulo-3 counter. The combined state of **11** for **S1** and **S2** is inhibited from occurring. It is generally referred to as an unused state. It is clear that to derive these states, decision logic is necessary. This is represented by the logic circuitry shown in FIG. **9***c*. The inputs of AND gate **51** are connected to the negation outputs b_1' and b_2' of **S1** and **S2**, respectively. Its output is directly connected to counter output terminal $\mathbf{0}_{B1}$. Only when both **S1** and **S2** are in the 0 state is a true output provided by the gate **51**, thereby indicating that the counter is in state 0. The assertion output b_1 of **S1** is connected to counter output terminal $\mathbf{1}_{B1}$. It is true only when **S1** is at a 1 state, indicating that the counter is in state 1. Similarly, the assertion output of **S2** is connected to counter output terminal $\mathbf{2}_{B1}$. It is true only when **S1** is in state 1, indicating that the counter is in state 2.

It is thus seen that the modulo-3 counter, **B1**, can be implemented by either a 3-stage ring counter or a 2-stage FSR. The ring counter of **3** memory stages does not require decision logic such as gates **51–53**, to determine the state of the counter. However, the 2-stage FSR, which requires one memory stage less than the ring counter, requires such logic. Thus, the trade off is between less memory stages at the price of more decision logic.

In order to complete the description of the implementation of the counters shown in FIG. **6** with minimum stage FSRs, FIGS. **10***a*, **11***a* and **12***a* are included herewith. They represent diagrams of FSRs which cycle through 2, 5 and 7 states, respectively, as shown in FIG. **10***b*, **11***b* and **11***c*. Thus, the FSR of FIG. **10***a* can be used for each of the modulo-2 counters of counter A. It does not require decision logic since its outputs b_1 and b' respectively, represent the 0 and 1 states of its single stage **S1**. The FSR shown in FIG. **11***a* can be used together with decision logic (not shown) as any of the counters forming counter C, and the FSR shown in FIG. **12***a* can be used together with decision logic as counter D.

As previously pointed out, the implementation of the system shown in FIG. **6** with ring counters requires **34** storage stages. When implemented with FSRs, such as those shown in FIGS. **9***a*–**12***a*, it requires only 3+3+3+2+2+2+1+1+1+1=19 storage stages. However, the reduction of 15 storage stages is achieved at the price of decision logic, which is needed to decode the combined states of the stages of the FSRs into the discrete states of the counters. Thus, the present invention may be implemented with either ring counters or FSRs, depending on the designer's choice. Indeed the present invention may be implemented with any circuit design technique which provides modulo-p_i counters where p_i is any distinct prime of a number, M.

Summarizing the foregoing description in accordance with the present invention, any nontrivial subperiod or delayed subperiod of a data frame whose length is equal to M clock pulse intervals can be derived by providing parallel modulo-m_i counters, where each m_i is a prime power factor (or divisor) of M. In the last described example, $i = 1, 2, 3$ and 4 where $m_1 = 2^4$, $m_2 = 3^3$, $m_3 = 5^2$ and $m_4 = 7$. Thus, four parallel counters are provided of moduli numbers of $2^4 = 16$, $3^3 = 27$, $5^2 = 25$, and $7^1 = 7$. Each modulo-m_i counter is decomposed into a cascade of α_i identical modulo-p_i counters, where $m_i = p_i^{\alpha_i}$. The term p_i is a distinct prime of M and α_i is the power to which p_i is raised to equal m_i. Thus, the modulo-2^4 counter (counter A) is decomposed into a cascade of 4 modulo-2 counters, (**A1**–**A4**), the modulo-3^3 counter (counter B) is decomposed into 3 modulo-3 counters (**B1**–**B3**), and the modulo-5^2 counter (counter C) is decomposed into 2 modulo-5 counters (**C1** and **C2**). The modulo-7^1 counter (counter D) is a cascade of a single modulo-7 counter. All the modulo-m_i counters are clocked synchronously by the clock pulses from a master clock. However, as pointed out herebefore in each cascaded modulo-m_i counter each of its modulo-p_i counters except for the first is clocked only when the preceding modulo-p_i counter in the cascade changes from its highest state of a cycle to the first state in the cycle. Thus, for example, in counter A, counter **A2** is clocked only when counter **A1** changes from state 1 to state 0. Similarly, counter **B2** of counter B is clocked only when counter **B1** changes from state 2 to a state 0.

It should be appreciated that the present invention is not limited to the values of M herebefore used as examples. As is known, the Fundamental Theorem of Arithmetic states that every number can be factored as a product of powers of primes, unique except for order. Therefore, as long as M is not a prime, any number M can be factored and implemented as herebefore described. Thus, a modulo-M counter can be decomposed as taught herein. For example, for M = 14,817,600 since

$$M = 2^6\,3^3\,5^2\,7^3$$

it can be decomposed by an arrangement just like that shown in FIG. **6** except that counter A would consist of a cascade of 6, rather than 4, modulo-2 counters and counter D would consist of a cascade of 3 modulo-7 counters rather than the single modulo-7 counter shown in FIG. **6**.

Herebefore reference was made to the Chinese Remainder Theorem which was used in one example to determine the number of CPIs from the start of the data frame needed to produce a particular combination of

states of the various counters. This theorem is well known by mathematicians. One reference to it is made in Topics in Number Theory, Volume 1 by W. J. LeVeque, published in 1956 by Addison-Wesley Publishing Company, Reading, Mass. However, for purposes of completeness, the theorem will be discussed herein.

The Chinese Remainder Theorem guarantees a unique solution for simultaneous congruences over moduli which are relatively prime by pairs. The theorem may be stated as follows:

Every system of linear congruences in which the moduli are relatively prime in pairs is solvable, the solution being unique modulo, the product of the moduli. Given the simultaneous congruences

$$\begin{aligned} x &\equiv a_1 \bmod m_1 \\ x &\equiv a_2 \bmod m_2 \\ &\vdots \\ x &\equiv a_n \bmod m_n \end{aligned}$$

where $(m_i, m_j) = 1$ for all i, j, where $i \neq j$ and $a_1, a_2, \ldots, a_n$ are any set of integers, let

$$M = m_1 m_2 \ldots m_n$$

and

$$M_i = M/m_i$$

Since $(M_i, m_i) = 1$, a unique solution exists for y_i in the linear congruence

$$M_i y_i \equiv 1 \bmod m_i \text{ for all } i$$

There is one and only one solution for x, which is determined as follows:

$$x \equiv \sum_{i=1}^{n} a_i y_i M_i \bmod M$$

Note that, as expressed in the above expression, x is a solution of each congruence in the expression $x \equiv a_n$ modulo m_n.

$a_i y_i M_i \equiv a_i \bmod m_i$

$\equiv 0 \bmod m_j$, where $j \neq i$

The latter results since m_j is a factor of M_i. The value of x is such that $0 \leq X < M$.

As an example let it be assumed that

$x \equiv 1 \bmod 3$ $a_1 = 1$ $m_1 = 3$

$x \equiv 2 \bmod 4$ $a_2 = 2$ $m_2 = 4$

$x \equiv 3 \bmod 5$ $a_3 = 3$ $m_3 = 5$

$M = 3 \cdot 4 \cdot 5 = 60$

$M_1 = 20$, $M_2 = 15$, $M_3 = 12$

$20y_1 \equiv 1 \bmod 3$

$15y_2 \equiv 1 \bmod 4$

$12y_3 \equiv 1 \bmod 5$

Unique solutions for y_1, y_2 and y_3 are 2, 3 and 3, respectively.

$x \equiv (40a_1 + 45a_2 + 36a_3) \bmod 60$

$x \equiv (40 \cdot 1 + 45 \cdot 2 + 36 \cdot 3) \bmod 60$

$x \equiv 58 \bmod 60$

Check

$58 \equiv 1 \bmod 3$

$58 \equiv 2 \bmod 4$

$58 = 3 \bmod 5$ A modulo-3, a modulo-4, and a modulo-5 counter would be in state 1 2 3 (i.e., $a_1 = 1$, $a_2 = 2$ and $a_3 = 3$) for $n = 58 + k60$ CPI, where $k = 0, 1, 2, \ldots$. State 1 2 3 repeats every 60 CPIs.

Although particular embodiments of the invention have been described and illustrated herein, it is recognized that modifications and variations may readily occur to those skilled in the art and consequently it is intended that the claims be interpreted to cover such modifications and equivalents.

What is claimed is:

1. A system comprising:

clock means for providing a succession of clock pulses of equal clock pulse intervals, each sequence of M clock pulse intervals defining a data frame, M being an integer other than a distinct prime and not less than one thousand;

a plurality of modulo-m_i multistage counters where each m_i is a different prime power divisor of M, each modulo-m_i counter comprising a different cascade of α modulo-p_i counters, where p_i in each cascade is the same and is a different distinct prime of M and α_i in each cascade is an integer not less than 1, with at least one α_i being greater than 1 and each $m_i = p_i^{\alpha_i}$;

means for coupling said counters to said clock means for clocking said modulo-m_i counters in parallel with said clock pulses, with the first counter in each cascade being clocked directly with each clock pulse and each succeeding counter in a cascade is clocked by a clock pulse only when the preceding counter in a cascade changes from a last state in its state cycle to a first state in its cycle whereby each modulo-p_i counter cycles through a cycle of p_i states and the combined states of the α_i counters forming each modulo-m_i counter represent different states of a state cycle of m_i states; and

logic means coupled to selected ones of said counters for providing a plurality of subperiods of said data frame as a function of the states of the counters to which it is coupled, each subperiod being a sequence of output pulses, each with an output pulse interval which is equal to the clock pulse interval times a different factor definable as X_i, where X_i is an integer and a factor of M and wherein the smallest value of X_i is equal to the smallest distinct prime of M, said subperiods including one delayed subperiod whose first output pulse is delayed by an interval from the start of said data frame, which is not less than one clock pulse interval and not greater than Y clock pulse intervals, where $Y \leq X_i - 1$.

2. A system as described in claim 1 wherein M includes at least two prime power divisors definable as m_1 and m_2 wherein $m_1 = p_1^{\alpha_1}$, p_1 being a distinct prime of M and α_1 is an integer greater than 1, and said plurality of counters includes a modulo-m_1 counter and a modulo-m_2 counter, said modulo-m_1 counter comprises a cascade of α_1 identical modulo-p_1 counters, each of said modulo-p_1 counters cycling through a cycle of p_1 states.

3. A system as described in claim 2 wherein $m_2 = p_2^{\alpha_2}$, where p_2 is a distinct prime of M other than p_1 and α_2 is an integer greater than 1, said modulo-2 counter comprises a cascade of α_2 modulo-p_2 counters each cycling through a cycle of p_2 states.

4. A system as described in claim 3 wherein said modulo-m_1 counter includes logic means for controlling each of said modulo-p_1 counters except for the first in said cascade of α_1 counters to be clocked only when

a clock pulse is received from said clock means and the preceding modulo-p_1 counter in the cascade changes from the highest state in its p_1-state cycle to the first state of the state cycle, and said modulo-m_2 counter includes logic means for controlling each of said modulo-p_2 counters except the first in said cascade of α_2 counters to be clocked only when a clock pulse is received from said clock means and the preceding modulo-p_2 counter in the cascade changes from the highest state in its p_2-state cycle to the first state of the state cycle.

5. A modulo-M counter, where M is an integer other than a distinct prime and is not less than one thousand, comprising:

a plurality of parallel modulo-m_i multistage counters, each m_i being a prime power divisor of M, i=1 through n where n is not less than two, each m_i counter including a cascade of α_i identical modulo-p_i counters where $m_i = p_i^{\alpha_i}$, where each p_i is a different distinct prime of M and is the same in each cascade and each α_i is an integer not less than 1, at least one α_i is not less than 2 with the total number of stages of all of said counters being not greater than the sum of $\alpha_i p_i$ of all the cascades, and is less than M;

means for clocking in parallel said plurality of modulo-m_i counters with each clock pulse in a sequence of clock pulses of equal intervals, with the first counter in each cascade being clocked directly by each clock pulse and each succeeding counter in a cascade being clocked by a clock pulse only when the preceding counter in the cascade changes from a last state in its cycle to a first state in its cycle, whereby each modulo-p_i counter cycles through a state cycle of p_i states and the combined states of α_i counters forming each modulo-m_i counter represent different states of a state cycle of m_i states; and

output means coupled to selected stages of selected counters of said plurality of counters for providing at least one output when said selected stages of said selected counters are in preselected states, said one output being a sequence of output pulses at an interval which is equal to the clock pulse interval times a factor X where X is a factor of M and the first output pulse occurring at a delay interval from a time when all of said counters are at their first states, said delay interval being equal to the clock pulse interval times a factor Y where $1 < Y < X-1$, both Y and X being integers.

6. A modulo-M counter as described in claim 5 wherein M is equal to the product of at least two prime power divisors, definable as m_1 and m_2, $m_1 = p_1^{\alpha_1}$, where p_1 is a distinct prime and α_1 is an integer greater than 1, and $m_2 = p_2^{\alpha_2}$, where p_2 is a distinct prime other than p_1 and α_2 is an integer not less than 1, said modulo-M counter including a first cascade of α_1 modulo-p_1 counters each modulo-p_1 counter cycling through a cycle of p_1 states, with the combined states of said α_1 modulo-p_1 counters representing a cycle of m_1 states, and a second cascade of α_2 modulo-p_2 counters, each modulo-p_2 counter cycling through a cycle of p_2 states, and logic means coupled to at least a plurality of the counters in the group including said modulo-p_1 and modulo-p_2 counters for providing an output for every M'th clock pulse where M' is less than M and is equal to $p_1^{\alpha_3} p_2^{\alpha_4}$, where α_3 is an integer not less than 1 and α_4 is an integer not less than 1.

7. A modulo-M counter as described in claim 6 wherein each of said modulo-p_1 counters is a p_1-stage ring counter.

8. A method for producing a selected output pulse related to a data frame represented by M clock pulse intervals of a succession of M equal interval clock pulses, M being an integer not less than one thousand and other than a distinct prime and is equal to the product of n prime power factors definable as m_1 through m_n, where n is at least equal to 2, the steps comprising:

providing a first cascade of α_1 modulo-p_1 counters where $m_1 = p_1^{\alpha_1}$, p_1 being a distinct prime and being the same in each counter of said first cascade and α_1 is an integer greater than 1;

providing at least a second cascade of α_2 modulo-p_2 counters where $m_2 = p_2^{\alpha_2}$, p_2 being a distinct prime different from p_1 and the same in each counter of said second cascade and α_2 is an integer greater than 1;

clocking said first and second cascades of counters with equal interval clock pulses, with the first counter in each cascade being clocked directly by each clock pulse and each preceding counter in a cascade being clocked by a clock pulse only when the preceding counter in the cascade changes from the last state in its state cycle to the first state in its cycle, whereby each modulo-p_1 counter cycles through a cycle of p_1 states, with the combined states of said α_1 modulo-p_1 counters representing a cycle of m_1 states, and each modulo-p_2 counter cycles through a cycle of p_2 states with the combined states of said α_2 modulo-p_2 counters representing a cycle of m_2 states; and

utilizing the states of selected stages of all of said counters to provide a selected output pulse during each data frame, at a time from the start of said data frame which is an integer multiple of said clock pulse interval.

9. A modulo-M counter, where M is an integer other than a distinct prime and is not less than one thousand, comprising:

a plurality of parallel modulo-m_i multistage counters, each m_i being a prime power divisor of M, i=1 through n where n is not less than two, each m_i counter including a cascade of α_i identical modulo-p_i counters, where $m_i = p_i^{\alpha_i}$, where each p_1 is a different distinct prime of M and is the same in each cascade and each α_i is an integer not less than 1, at least one α_i is not less than 2 with the total number of stages of all of said counters being not greater than the sum of $\alpha_i p_i$ of all the cascades, and is less than M;

means for clocking in parallel said plurality of modulo-m_i counters with each clock pulse in a sequence of clock pulses of equal intervals, with the first counter in each cascade being clocked directly by each clock pulse and each succeeding counter in a cascade being clocked by a clock pulse only when the preceding counter in the cascade changes from a last state in its cycle to a first state in its cycle, whereby each modulo-p_i counter cycles through a state cycle of p_i states and the combined states of the α_i counters forming each modulo-m_i counter represent different states of a state cycle of m_i states; and

output means coupled to a selected stage of each of said counters for providing a single output pulse

which is delayed by X clock pulse intervals from an interval when all of said counters are in their first state, X being an integer where

$$X = a_1 \text{ modulo } m_1 = a_2 \text{ modulo } m_2 \ldots = a_n \text{ modulo } m_n,$$

where a_1, a_2 through a_n represent states of the state cycles of said m_i counters, said output means including logic means for providing said single output pulse only when said m_1 through said m_n counters are respectively in states a_1 through a_n of their respective state cycles.

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