NASA TECH BRIEF

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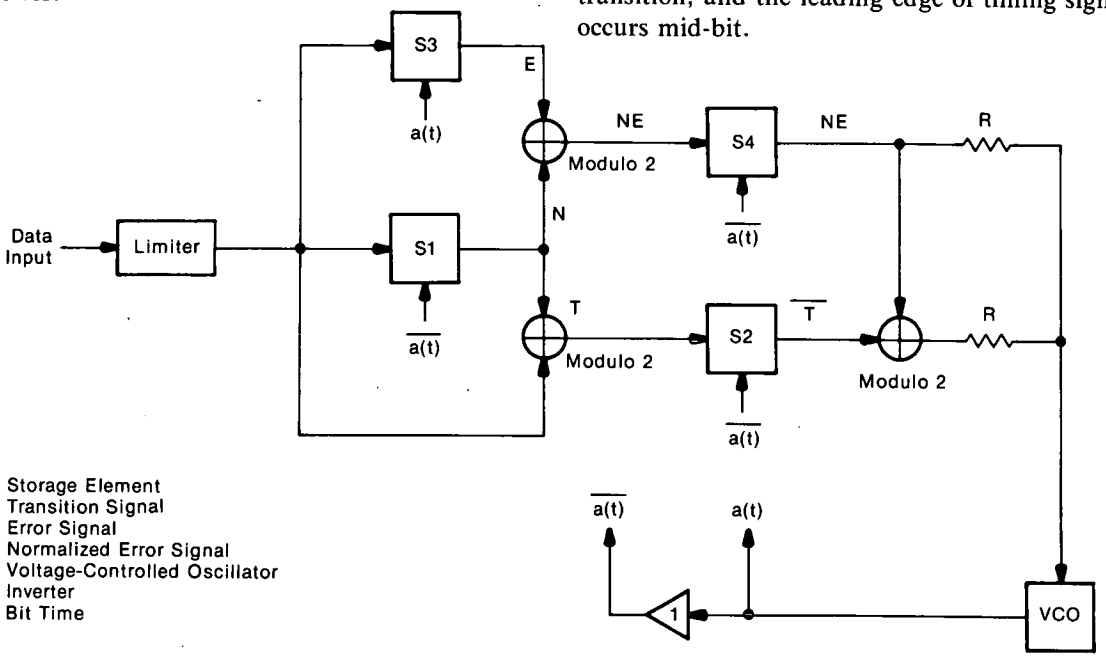
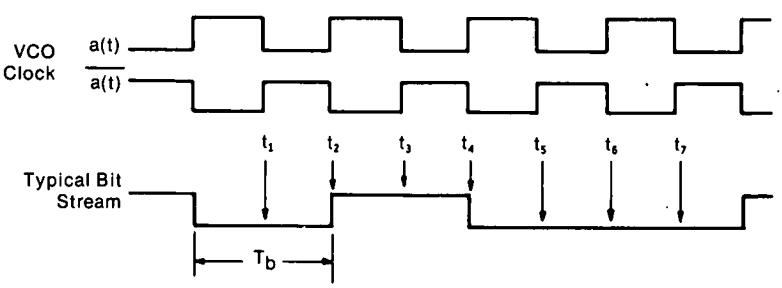
Synchronizer for Random Binary Data

A simplified binary-data transition detector, for the synchronization of relatively noise-free signals, can be used with radio or cable data-control links. It permits the reception of binary data in the absence of a clock signal or a self-clocking coder. The detector includes a phase-locked loop (PLL) and a voltage-controlled oscillator (VCO) to reconstruct the data clock rate at the receiver.

The detector loop, as shown in the block diagram, incorporates a VCO which generates a square-wave output at twice the frequency of the incoming bit rate. The true and complement outputs at a(t) and $\overline{a(t)}$ are the data transition sample pulse and the mid-bit sample pulse, respectively. When the PLL is in lock the leading edge of timing signal a(t) occurs at the bit transition, and the leading edge of timing signal $\overline{a(t)}$ occurs mid-bit.



Notes:
S = Storage Element
T = Transition Signal
E = Error Signal
NE = Normalized Error Signal
VCO = Voltage-Controlled Oscillator
I = Inverter
T_b = Bit Time



System Block Diagram and Sample Timing

(continued overleaf)

The leading edge of timing signal a(t) is used to sample the input data to determine the sign of the present phase error and to derive the error signal. The leading edge of timing signal $\overline{a(t)}$ is used to sample the input data to determine whether a transition occurred or not. If a transition occurred a binary-valued error voltage is applied to the VCO. If a transition did not occur a voltage that is midway between the two binary values is applied to the VCO. This provides an output frequency from the VCO, when there is no transition, that is approximately equal to the received data rate.

Storage is required as follows (see sample timing under the block diagram): Time t_1 is the point in time where the data is first sampled and then stored in storage element S1. At time t_3 the data stored is added modulo 2 to the present data and is stored in S2. The output from S2 then indicates whether a data transition occurred at time t_2. At time t_2 the data is sampled and stored in S3. The output from S3 is added modulo 2 to the output from S1 which serves as the normalizing term N.

This addition assures the independence of the sign of the error signal from the direction of the transition. At t_3 the normalized sign of the error signal NE is stored in S4. The output from S2, the transition detector, remains for one full bit time between t_3 and t_5. The output from S4, the sign of the error signal, remains for the same length of time. The data are eventually clocked into a serial-input shift register (not shown) for receiver processing.

Note:

Requests for further information may be directed to:

Technology Utilization Officer
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4800 Oak Grove Drive
Pasadena, California 91103
Reference: TSP75-10325

Patent status:

NASA has decided not to apply for a patent.

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(NPO-13286)