NASA TECH BRIEF

Marshall Space Flight Center

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Real-Time Video Correlator

The problem:

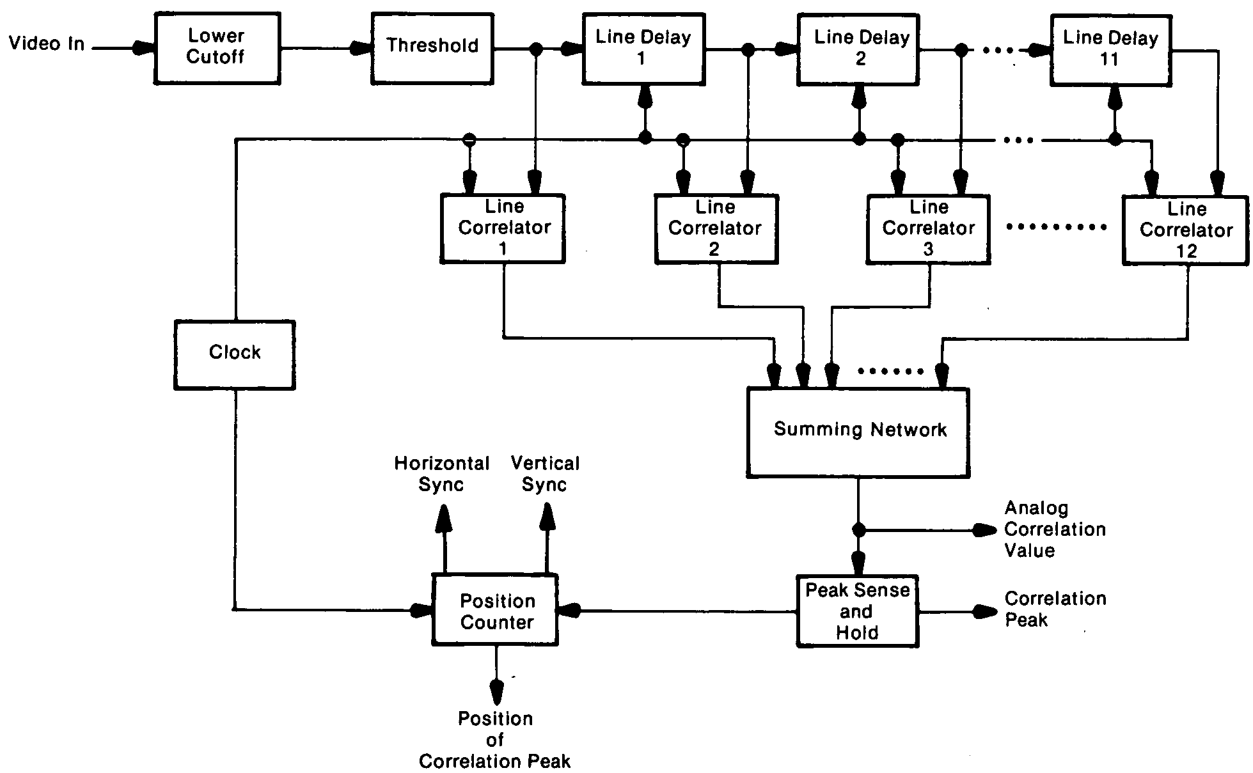
Two-dimensional correlation of video data is a complicated and slow procedure. Some of the standard methods include the use of optical sources, video disks, and sequential digital calculations. These methods are expensive; none operates in real time.

The solution:

A new real-time video correlator is fast and inexpensive.

How it's done:

The correlator as shown in the illustration includes 11 line delays and 12 line correlators. The real-time digitized video (TTL logic level) is fed into the line delays (MOS 64-bit shift registers) serially. At the same time, any information available at the input of each line correlator is clocked through. During the first line cycle, the first line of live video data is clocked through line correlator 1. During the second line cycle, the first line of live video data is clocked through line correlator 2, and the second line through correlator 1, etc.



Real-Time Video Correlator

(continued overleaf)

The input video entering a line correlator is available to a series of 12 paired shift registers. One side of the paired series is continuously clocked during the correlation. This permits the physical translation of a line of live data relative to a line of stationary reference data, namely, that stored in the remaining side of the paired series. The outputs of each of the 12 pairs of registers are put through EXCLUSIVE-OR gates and are summed. This corresponds to the output of the single line correlator, which is one-twelfth of the total input to the summing network.

Basically, the 11 line delays serve to translate the real-time image vertically (Y direction) with respect to the stored image, whereas each line correlator serves the function of horizontal translation (X direction). The stationary line of data (reference) is one of the 12 lines of the stored reference scene. If the operator desires to update or change the reference, the memory update clock is enabled, and the incoming video is fed through both sides of the paired series of registers in each line correlator but is frozen into one side only at the designated point. At that time the memory update clock is disabled.

The outputs of all 12 line correlators are summed with each clock pulse and are fed into a peak sense-and-hold module. At that point the operator can monitor the analog correlation values. The peak detector tracks the correlation value and holds the peak value per frame. A free-running synchronous position counter assigns a count (coordinate) to each successive value of the correlation output and also registers per frame the coordinate assigned to the maximum correlation value attained at that frame.

A prototype correlator has undergone rigorous testing and has been the subject of numerous demonstrations. Its operation has been extremely reliable, accurate (within present constraints on resolution and memory, which are easily removed), and quite predictable. Manual operation of the unit also has been made easy.

Note:

Requests for further information may be directed in writing to:

Technology Utilization Officer
Marshall Space Flight Center
Code AT01
Marshall Space Flight Center, Alabama 35812
Reference: B75-10265

Patent status:

Inquiries concerning rights for the commercial use of this invention should be addressed to:

Patent Counsel
Marshall Space Flight Center
Code CC01
Marshall Space Flight Center Alabama 35812

Source: P. E. Geise, Jr., M. Petcher, and D. F. Cornwell of Sperry Rand Corp.
(MFS-23200)

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