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Fast Fourier Transformation Computer Using Fast Counters

Special-purpose computing machines implementing the fast Fourier transform (FFT) algorithm have revolutionized the field of data processing. They make it possible to obtain the discrete Fourier transform (DFT) of a sequence of data points in a method which is both economical and fast.

When the speed of transformation obtainable through a serial application of the FFT algorithm is still not sufficiently high, one has to resort to seriesparallel implementations with their attendant cost increase. It is shown that for small batch sizes ($N \le 32$), a more cost-effective design can be based on transforming the basic DFT matrix into a Hankel (or Toeplitz) matrix. This leads to a realization in which the main hardware investment is in a large array of "full-adders" employed as elementary counters.

Two different designs have been developed, one applicable to N prime and one applicable to all N. For low N, both designs have a cost advantage over the equal-speed implementation of the FFT algorithm.

The limiting N value (32) mentioned above is a function of the ratio of the cost of memory to that of logic elements and will increase with this ratio.

Note:

Requests for further information may be directed to:

Technology Utilization Officer NASA Pasadena Office 4800 Oak Grove Drive Pasadena, California 91103 Reference: TSP75-10175

Patent status:

NASA has decided not to apply for a patent.

Source: Shalhav Zohar of Caltech/JPL under contract to NASA Pasadena Office (NPO-13110)

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