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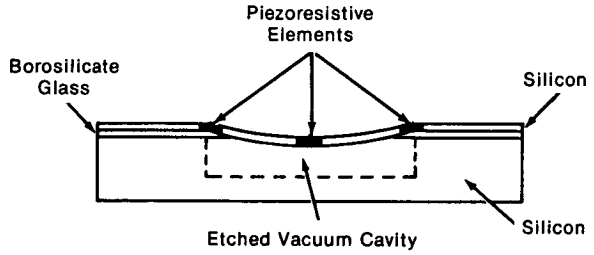
NASA TECH BRIEF

Langley Research Center

Low-Temperature Electrostatic Silicon-to-Silicon Seals Using Sputtered Borosilicate Glass

A new method for sealing two silicon surfaces together produces an all-silicon package. The package has advantages which are especially important for compensating the effects of temperature upon piezoresistive and piezojunction sensors. The silicon members are hermetically sealed to each other at a temperature $\gtrsim 500°$ C. The process produces no measurable deformation of the silicon surfaces and is compatible with package designs of tight tolerance.

The surfaces of the silicon members to be sealed are polished, cleaned, and stripped of any residual oxide. They are then coated with sputtered borosilicate glass to a minimum glass thickness of approximately 4 μm. Prior to sealing, each coated silicon substrate is annealed at 600° to 900° C. A slightly higher yield is obtained when this annealing is carried out in steam, but successful seals are formed after annealing in either nitrogen or oxygen.



Silicon-to-Silicon Electrostatic Seal Under Hermetic Test

To achieve the silicon-to-silicon electrostatic seal, a second polished silicon chip is alined in the desired orientation on top of the first silicon member, which is already coated with borosilicate glass. The combination is then heated and stabilized to a temperature of 450° to 550° C. A slowly-increasing dc voltage is then applied across the silicon-borosilicate glass-silicon sandwich, the uncoated silicon member being positively biased. After reaching a maximum voltage (50 V), the sandwich is left at the process temperature and the maximum voltage for 5 minutes. To complete the sealing operation, the substrate heater is removed, and the sandwich is returned to near room temperature before removing the voltage.

To test the hermeticity of such a seal, a number of silicon-to-silicon seals were prepared in which one silicon member of the silicon-borosilicate glass-silicon sandwich had a deep cavity etched part way through it. The second silicon member was then thinned to a total thickness of 0.025 to 0.1 mm (1 to 4 mils), and the sealing operation was carried out in a vacuum chamber at a pressure of approximately 10^{-5} torr. Upon completing the seal and removing the unit from the chamber, atmospheric loading on the thin top member produced a visible depression above the cavity, as shown in the illustration.

Such an evacuated cavity has been measured as essentially leak free by helium leak testing. Even after 63 thermal cycles between +100° and —40° C, the unit showed no loss of dimple or measurable leak rate.

(continued overleaf)

Notes:

1. Seals have been made with glass coatings in the 10-mm to 20-mm thickness range without any prior annealing of the coated silicon substrates. Higher maximum sealing voltages can be tolerated with the thicker glass coatings without the danger of breakdowns.
2. Requests for further information may be directed to:

   Technology Utilization Officer
   Langley Research Center
   Mail Stop 139-A
   Hampton, Virginia 23665
   Reference: B74-10263

Patent status:

NASA has decided not to apply for a patent.

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04 (Materials)
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