NASA TECH BRIEF

Ames Research Center

Decimal Digit Generator for Commutated Data — A Concept

The problem:

To replace ordinary analog-to-digital devices with similar, less expensive systems that can handle commutated data with little loss in resolution or dynamic range.

The solution:

First perform an analog-to-digital conversion on the input signal with a staircase circuit that has a 10-percent resolution and then convert the digital result to an analog voltage and subtract it from the original input signal; read out the feedback signal as the decimal digit representation during one clock phase and the servo-error difference between the input and the feedback as the analog portion during the following clock phase.

How it's done:

The input commutated analog signal pulse is converted into a pulse pair; the first determines the amplitude within 10-percent resolution and the second defines the data within the 10-percent range identified by the first pulse. The original analog data is converted from a decimal digit plus an analog pulse which is a ten-fold amplified version of the difference between the decimal digit and the original analog data.

Commutated data is added to a feedback signal in a summing amplifier during time phase $\overline{\phi_1}$ obtained from an oscillator. During phase ϕ_1, the feedback is disconnected and the input signal passes through an absolute value circuit which uses opposite polarity diodes to steer the current into the two inputs of an amplifier. The absolute value circuit output goes to a set of nine biased comparators. The comparators biased below the incoming signal level turn on, while those biased above the incoming signal stay off. The output of the comparators is summed to form an analog magnitude representing the number of comparators turned on. This analog signal has a staircase characteristic in which each step is 10 percent of full scale. A sample-and-hold circuit holds the decimal digit during ϕ_1 so that it is ready for feedback application during the following phase $\overline{\phi_1}$. The input minus feedback servo error signal is read out as the second member of the output pulse pair during time phase $\overline{\phi_1}$.

The staircase function is implemented through an absolute value circuit to avoid duplication of the comparator array for negative signals. A comparator sets the sign at the output, positive for positive input and negative for negative input.

The decimal digit generator circuit increases the accuracy of commutated data at least by a factor of 10 with essentially no loss of resolution or dynamic range and very little reduction in frequency response.

Note:

Requests for further information may be directed to:

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Reference: TSP 74-10120

Patent status:

NASA has decided not to apply for a patent.

Source: Stanley J. Rusk of
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Category 01