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NASA TECH BRIEF

Langley Research Center

Logical-Function Generator

An apparatus and technique for generating logical functions and circuits have been developed (see Figure 1). They provide an aid in designing and constructing hardware to generate logic circuits, by defining the circuit connections required to generate these functions.

With this method, it is possible quickly and automatically to design logic, while eliminating involved and time-consuming mathematical manipulations. This method also eliminates lengthy and difficult computer programming, as well as the use of expensive and large general-purpose computing facilities for logic design. It provides a method for finding directly minimal circuits for NAND-NOR logic (although no known direct mathematical method exists), a means for mapping quickly functions to circuits, and a tool for use in conducting research on minimal NAND-NOR form.

This method provides for switching to permute a number of input literals and recursive inputs into a number of logical connective elements. The outputs from these connective elements provide the set of all functions possible from these connective elements and input literals. Monitoring the switching states provides the set of all logical circuit connections, associated with the set of all generated functions, with a one-to-many mapping existing between functions and circuits.

The input generator generates all possible input combinations of the literals $a_o - a_i$ which are applied to the circuit generator on $(i + 1)$ lines. The switching generator generates steering signals $x_o - x_j$ on $(j + 1)$ lines as inputs to the circuit generator. These steering signals gate the input literals $(a_o + a_i)$, along with some connective element outputs, into $(k + 1)$ logical connective elements (C_k) having outputs $f_o - f_k$. One set of steering signals is generated for each input cycle, which provides for the generation of a different circuit for each input cycle and continues until all circuits have been produced. The circuit generator supplies the logic required to generate different circuit connections as a function of the $x_o - x_j$ switching signals. The control provides timing and logical control for the system, as required. The input generator must produce and continue to regenerate input cycles.

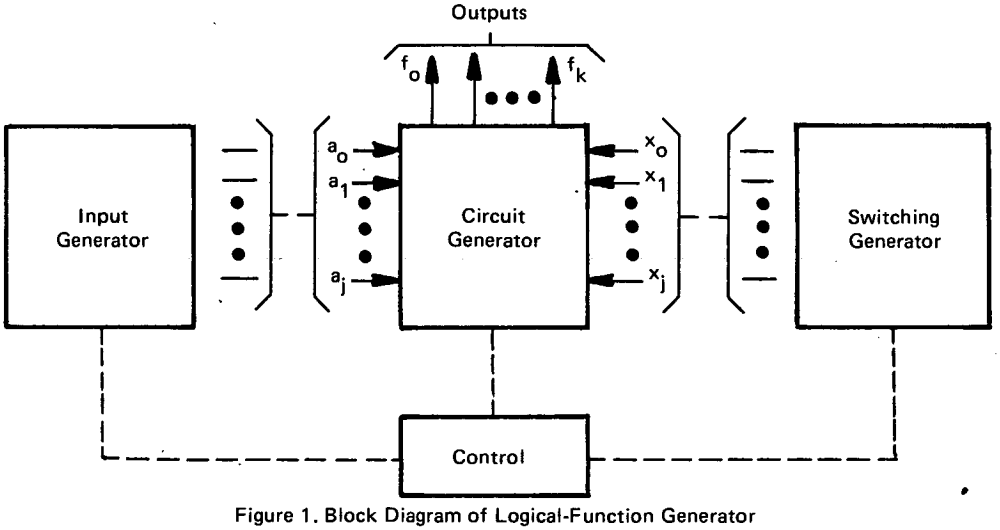

Figure 1. Block Diagram of Logical-Function Generator

(continued overleaf)

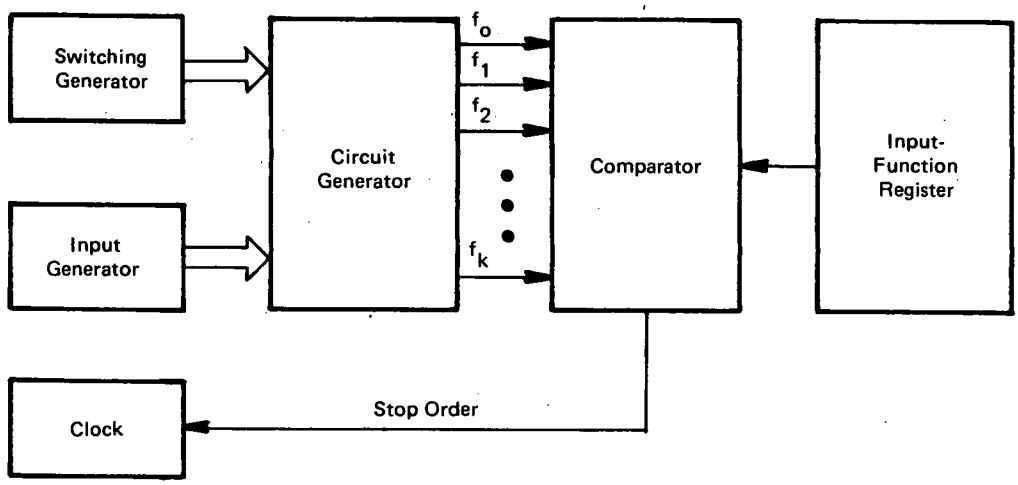

Figure 2. Circuit-Selection Diagram

Figure 2 illustrates the system in use. To design a circuit that generates the function g with the least amount of hardware, set the value g in the input function register and input this function to the comparator. Start the logic-function circuit generators. When one output function f is generated so that f_o or f_1 or . . . f_k equals g, the comparator generates a stop order that will stop further circuit generation. This can be accomplished by having the stop order stop the clock. The output from the switching generator structures and defines the connections necessary to design a circuit for generating g. This procedure is repeated until the output of the switching generator has generated all possible combinations of the switching signals, for which the circuit generator generates an f that is equal to g. The circuit that requires the least hardware can then be selected.

Note:

Requests for further information may be directed to:

Technology Utilization Officer
Langley Research Center
Mail Stop 139-A
Hampton, Virginia 23665
Reference: B73-10360

Patent status:

This invention has been patented by NASA (U.S. Patent No. 3,700,868). Inquiries concerning nonexclusive or exclusive license for its commercial development should be addressed to:

Patent Counsel
Langley Research Center
Code 456
Hampton, Virginia 23665

Source: Wilford E. Sivertson, Jr.
Langley Research Center
(XLA-5099)