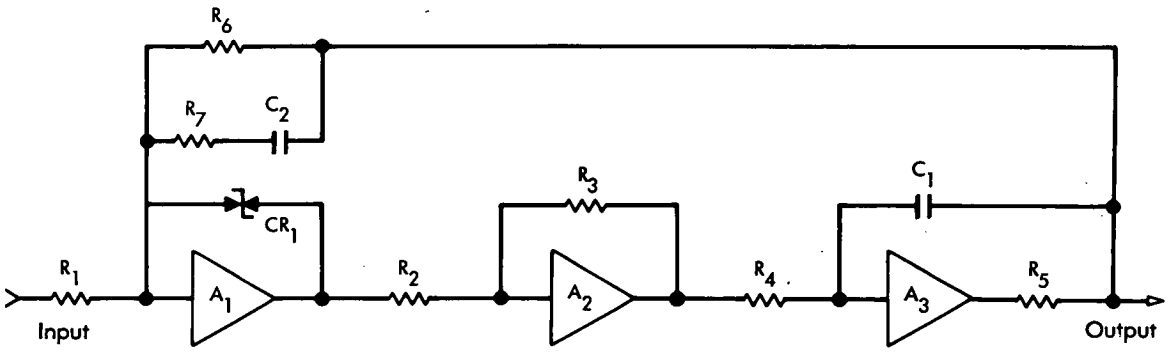
NASA TECH BRIEF

NASA Pasadena Office

Operational Slope-Limiting Circuit



The problem:

To limit the slope of an arbitrary waveform in order to avoid exceeding the rate limit of a subsequent amplifier, or to form a trapezoidal wave with adjustable rise and fall rates from a square wave of arbitrary frequency.

The solution:

A circuit consisting of an amplifier, an inverter, and an integrator; the integrator provides the delay needed to develop the output waveform. DC coupling is used to preserve the original DC offset.

How it's done:

The circuit is shown in the diagram; the output of the first of three general-purpose operational amplifiers is bridged to its input by a double-anode zener or two closely-matched back-to-back zeners (CR_1) with breakdown voltages within the excursion capability of the amplifier (say, 8 volts). The amplification of the second amplifier (an inverter) is set approximately at unity by resistors of the order of 10 kilohms (± 5%). The input resistor to the last amplifier is set at a few kilohms to 100 kilohms or more, and the integrating capacitor can be from 100 pf or less to 1 mfd or more in order to set the slope limit. For adjustable slope operation, the input resistor to the last stage may be variable and the capacitor value is altered by switching. The output resistor in the last stage is optional but, if used, it determines the circuit output impedance, and permits use of large capacitances which otherwise must be limited to about 0.05 mfd by the choice of the operational amplifier. The main feedback resistor, R_6, and the input resistor, R_1, determine the overall gain of the circuit; generally, they will be a closely-matched pair (say, 10 kilohms each). The series resistor-capacitor combination, R_7 and C_2, across R_6 compensates the loop gain which, for a small signal, is the product of the gains of the first and third amplifiers (typically about 200 dB); the RC combination also stabilizes the gain. The optimum value of the RC combination is determined empirically, and will be governed by the characteristics of the operational amplifiers, but if the integrating capacitor, C_1, is switched, then the RC compensating combination must also be switched.

(continued overleaf)

When the input signal changes rapidly, the output is prevented from following it by the delay in the integrator; consequently, a large error exists in the loop and the output of the first amplifier rises until it is clamped by CR_1. A constant voltage is applied to the inverter, causing the integrator to slew at a uniform rate until the output very nearly equals the input.

When the change of input signal is sufficiently slow to allow the integrator to keep up with it, the circuit operates linearly, exactly reproducing the input waveform. (Note that the output signal is inverted in polarity with respect to the input).

Note:

Requests for further information may be directed to:

Technology Utilization Officer
NASA Pasadena Office
4800 Oak Grove Drive
Pasadena, California 91103
Reference: TSP 73-10346

Patent status:

NASA has decided not to apply for a patent.

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