July 1973 B73-10292

NASA TECH BRIEF

NASA Pasadena Office

Minimal Hardware, Binary Sequence Pseudonoise Generator and Detector

The problem:

To provide a binary sequence generator for determining the mathematical properties of polynomials such as divisibility, the period, the order of the roots, and other parameters that affect the desirability of various sequences for specific applications; for example, irreducible polynomials which characterize sequences with randomness properties.

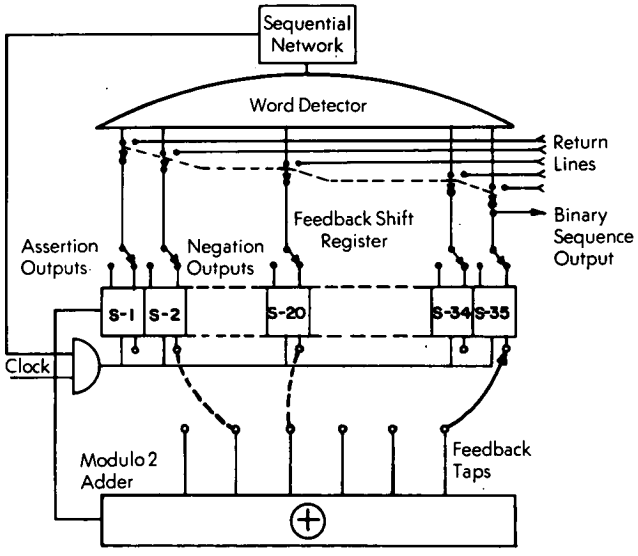
The solution:

A general purpose sequence generator and detector which includes a 35-stage field shift register constructed to operate at a clock frequency of 1 MHz.

How it's done:

The field shift register (FSR) is constructed in such a way that the length can be altered, any predetermined initial state can be inserted, and the modulo-2 sum (exclusive OR) or the complement of the modulo-2 sum of the content of the stages i, j, and r where $i<j<r$ can be inserted. A word detector (effectively an r-input gate) is used to sense and "remember" the initial state. By means of control logic, the initial state is inserted, the word detector primed, the clock initiated, and the clock terminated when the FSR is returned to its initial state. The foregoing sequence yields a count of the number of pulses required for the FSR to return to its initial state. The count is equivalent to the length of the cycle containing the initial state. Any desired FSR sequence is initiated by referring to tables of irreducible polynomials.

The basic elements of the sequence generator and detector are shown in the diagram. The FSR consists of 35 stages of flip-flops connected as a shift register. Indicator lamps on the assertion outputs of each of these indicate when that stage is high (1 state). The effective length of the shift register can be adjusted to any number of stages between 1 and 35. Generally,



in working with pseudonoise (PN) sequences, no fewer than 20 stages are used, and as many as 15 more stages can be annexed. The assertion or negation output of each flip-flop can be connected to the word detector by switches. In this function, the word detector samples the initial state of the FSR and transfers this binary information to the sequential network which memorizes the initial state of the FSR. The sequential network provides a logic state which enables the clock to strobe the FSR until the initial state is repeated by the FSR. In application as a

(continued overleaf)

general purpose sequence generator, the output is taken from the assertion output of the last flip flop (or any other desirable stage). A power driver stage may be added for some applications where large fan-out is desired, but the flip-flop has sufficient drive for most general purpose applications. Provision is made for up to six feedback taps, thereby making it possible to generate sequences corresponding to polynomials with 7 terms (6 taps) or fewer. Such polynomials are sometimes desirable in generating codes for error-correction coding/decoding systems.

For linear feedback, used for cycles of maximal length primarily for PN generation, a three-input modulo-2 adder is used with $r+1$ or $r+2$ stages and its output is fed back to the first stage of the FSR. This is done when an rth degree primitive trinomial does not exist and a length 2^r-1 pseudonoise sequence cannot be generated with a two-tap FSR with r stages. The i, j, and r taps shown in the diagram correspond to stage numbers; in every case, a tap is connected to the last or highest numbered stage. After sampling the initial state of the FSR, the word detector may be switched to receive inputs from logic circuits under test to stop the test automatically upon completion of a sequence.

Reference:

Perlman, M.: Pseudonoise Sequence Generation with Three-Tap Linear Feedback Shift Registers. JPL Technical Report 32-1432, November 15, 1969 (N70-13354).

Notes:

1. In order to truncate a maximal length cycle for a particular sequence of states, a *nonlinear* feedback function term can be added by inserting an AND gate which recognizes a particular state in the register and causes a jump to a new state which is not its normal successor. An inversion results when a 1 output of the AND gate is modulo-2 summed with other feedback terms and causes the FSR to jump to the next state.
2. Requests for further information may be directed to:

   Technology Utilization Officer
   NASA Pasadena Office
   4800 Oak Grove Drive
   Pasadena, California 91103
   Reference: TSP 73-10292

Patent status:

This invention has been patented by NASA (U.S. Patent No. 3,700,869). Inquiries concerning nonexclusive or exclusive license for its commercial development should be addressed to:

NASA Patent Counsel
Mail Code 1
NASA Pasadena Office
4800 Oak Grove Drive
Pasadena, California 91103

Source: Marvin Perlman of
Caltech/JPL
under contract to
NASA Pasadena Office
(NPO-11406)