# NASA TECH BRIEF <br> John F. Kennedy Space Center 


#### Abstract

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## High Speed Direct-Binary to Binary-Coded-Decimal Converter and Scaler

## The problem:

A telemetry (pulse code modulated) digital system, as a general rule, sends binary numbers representing some parameter that is not the value of the binary number. The received binary number must be scaled and converted to binary coded decimal to operate a readout device to display the true value. This conversion is usually accomplished by use of a digital clock and counter chain. The speed of the conversion has been limited by the speed of the clock pulses as well as the speed of operation of the counter and the associated hardware. The dependence of conversion on all these factors slows the entire data processing operation.

## The solution:

The clock and counter chain can be eliminated by a group of adders which speed up the binary number conversion and scaling in one operation.

## How it's done:

The group of adders that are used for this conversion are shown in Figure 1. The group shown is decade connected for producing units readout. Similar decades are provided for the 10 's and 100 's readout, etc. Each of the adders has three inputs, sum outputs (S's), and carry outputs (CA's). The four adders in the bottom row have their carry output connected to an input of the


Figure 1. Units Readout Connected Adder Group

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| $\begin{array}{c}\text { Ref. } \\ \text { Char. }\end{array}$ | Decimal Number |  |  |
| :---: | :---: | :---: | :---: | :---: | \(\left.\begin{array}{l}Binary <br>

Number\end{array}\right]\)

Figure 2. Conversion Sequence
next adder on the left. The carry output of adder $\mathrm{A}_{1}$ is connected to input of adder $\mathbf{A}_{2}$. The sum of output adder $A_{1}$ is connected to an input of adder $A_{5}$ in the row directly above. Similar connections are between adders $A_{2}$ and $A_{6}, A_{3}$ and $A_{7}$, and $A_{4}$ and $A_{8}$, respectively. The sum outputs of adders $A_{6}, A_{7}$, and $\mathrm{A}_{8}$ are fed into a row of adders $\mathrm{A}_{10}, \mathrm{~A}_{11}$, and $\mathrm{A}_{12}$ which have their sum output connected to a readout driver. The driver is connected to a display tube which exhibits number " 0 " to " 9 ".

In the conversion sequence (see Figure 2) the binary number is illustrated on the right, the decimal number in the middle, and reference characters A through H on the left. The latter represent the signals being fed into the adders. For example, if the binary coded number is 00000001 , which is represented by character A , it will be fed into the readout tube and the numerical character 1 will be illuminated. However, if the binary character is 00010000 , which is equal to 16 , the character represented by E would be fed into adders $\mathrm{A}_{2}$
and $\mathrm{A}_{3}$. These adders would form the unit value 6 which is the units digit. The number 10 is carried into the next decade (not shown) and processed accordingly.

Scaling of the numbers is accomplished by the same circuit simultaneously with the conversion. Selection of the scaling factor is accomplished by use of different patchboard cards which are programmed for each specific factor. These patchboards may be automatically controlled by using punch buttons.

## Note:

Requests for further information may be directed to:
Technology Utilization Officer
Kennedy Space Center
Code AD-PAT
Kennedy Space Center, Florida 32899
Reference: TSP73-10281

## Patent status:

This invention has been patented by NASA (U.S. Patent No. $3,638,002$ ). Inquiries concerning nonexclusive or exclusive license for its commercial development should be addressed to:

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