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NASA TECH BRIEF

Marshall Space Flight Center

P-Channel Silicon Gate FET

The problem:

The conventional fabrication of P-channel Metal-Oxide-Semiconductor-Field-Effect-Transistor (MOSFET) devices involves a critical step in the alignment of the gate metalization mask. Because of this, fabrication of large arrays of nonredundant devices on single wafers has proven difficult. The problem is that a design tolerance must be built into the system to allow for a slight misalignment. This usually leads to an 8- to 10-μm gate overlap above the source and drain regions, increasing the gate capacitance which limits the speed of the MOSFET.

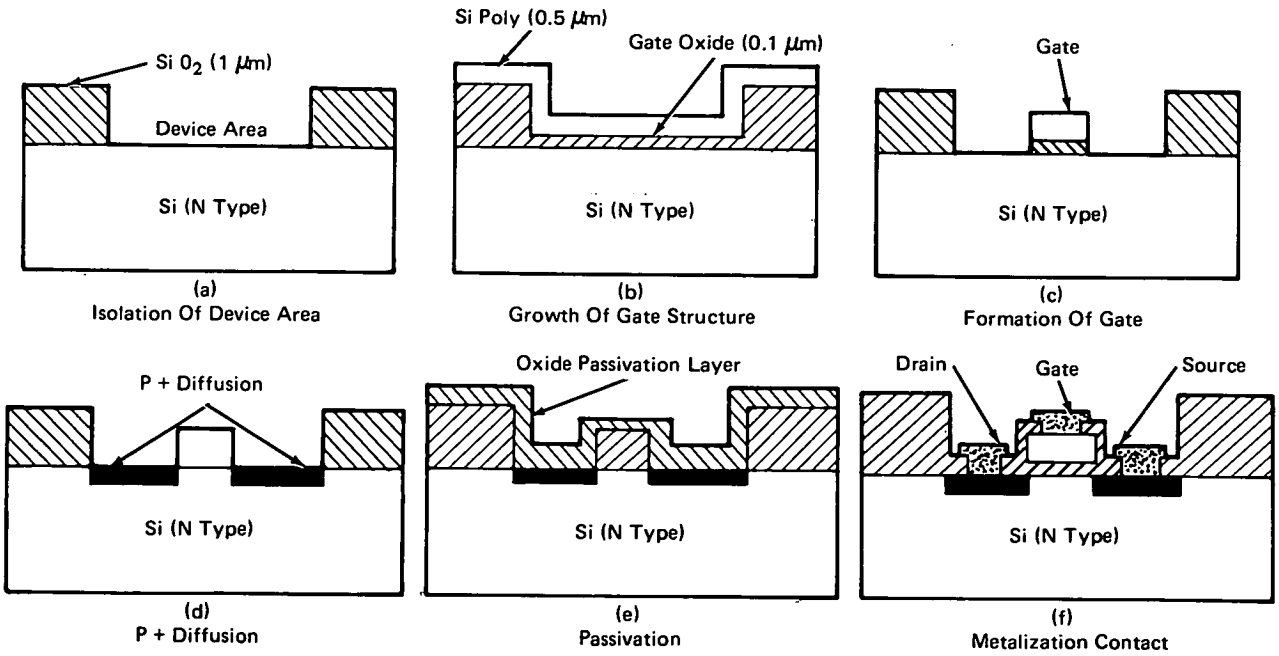
The solution:

A modified fabrication technique for the P-channel MOSFET devices eliminates the problems involving gate placement and gate overlap.

How it's done:

The entire process, as shown in the figure, involves six steps. First, the device area is isolated on the silicon N-type substrate (step a). Immediately after the clean gate oxide is grown, the layer is covered and protected by a polycrystalline silicon layer (step b). Next, the gate is formed (step c). The gate electrode and source and drain regions are then simultaneously diffused, and thus are geometrically well defined (step d). Further lateral diffusion of the P^+ doped regions is kept at a minimum by limiting the temperature in the remaining processing steps. The final steps (e) and (f) are deposition of the oxide passivation layer and formation of metalization contacts, respectively.

This technique provides a self-aligned gate, eliminating the complexity of mask aligning. The source and drain electrodes are formed exactly as required with a lateral diffusion equal to the depth of diffusion, 0.5 μm.



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Devices produced by this process are considerably faster than conventional MOSFET's because the parasitic capacitance has been reduced by at least a factor of 10. Since the work function of polycrystalline silicon is much closer to that of the single silicon substrate than any metalization, device threshold voltages are reduced by a minimum of 0.5 V, which makes it possible to use lower-voltage power supplies. Finally, the process increases the yield because the gate oxide photoresist step is not as critical as in the conventional process.

Note:

Requests for further information may be directed to:

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Patent status:

Inquiries concerning rights for the commercial use of this invention should be addressed to:

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