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# NASA TECH BRIEF

*Goddard Space Flight Center*



## Two Autowire Versions for CDC-3200 and IBM-360

Telemetry ground data processor equipment design and fabrication at Goddard Space Flight Center in the past was accomplished through the use of commercial logic cards or modules. Each design engineering group selected a manufacturer logic system which suited their particular requirements. Unfortunately, these logic systems were not compatible physically or electrically with each other, thus eliminating competition when additional purchases were made. As integrated circuits improved in performance and price, an opportunity for performance and size improvement motivated the Processor Development Branch of the Information Processing Division to investigate new methods of implementation of the integrated circuits.

A micro-electronics program was initiated to evaluate circuitry, packaging methods and fabrication approaches necessary to produce a competitively procured logic system.

Goals of this micro-electronic program are:

1. An integrated circuit evaluation, to evaluate circuit elements for their electrical performance, their availability from numerous sources, and the completeness of the logic line;
2. In special circuit development, to design and test additional circuitry unavailable in the form of integrated circuits, and to develop techniques that will allow competitive manufacture;
3. In hardware development, to design and develop modular rack-mountable hardware to house the integrated circuits;
4. In software development, to provide the designer with computer-generated design, fabrication, and drafting assistance to the designer to reduce cost and the incidence of human error;
5. In testing and documentation, to evaluate available test equipment and fixtures for use with the new logic system, and to provide a user's manual for the logic system and the program aids.

The NAS-PAK logic system emerged more from the integrated circuit dual in-line package than any other aspect of the logic system development. Circuit evaluation was performed without regard to package type. Hardware development, however, required consideration of each package type. The familiar printed circuit card was discarded due to connector pin number limitations. A socket panel with plug-in capacity for sixty 14-pin dual in-line packages was chosen. These panels contain 14 wire-wrap pins per socket. Six socket panels are mounted on an aluminum frame which in turn is mounted in a drawer assembly or a vertical page assembly.

A Gardner-Denver Automatic Wire-Wrap Machine was used which eliminated manual wiring errors and human deficiencies in the fabrication area but offered no improvement for design modifications or corrections after wiring. Computer programs were written to minimize errors introduced at the design phase. These programs reduce the modifications and corrections required by eliminating the most common design errors before wiring.

The block entry program reduces the input wire list card number by generating wire-list cards from a single descriptive statement. Large shift registers and counters may be entered with a statement such as "–32 SRS." The block entry program generates all interconnection wiring cards necessary to wire the shift register as determined by the block entry function library. Since the designer does not have a drawing of the function, a program was developed to show the designer how the computer implemented his input statement. The Auto-

(continued overleaf)

Draft program provides drive information to an x - y plotter to draw the logic symbols with module type, socket and pin information. The symbols are positioned on the paper by coding information provided by the designer or the computer on the wire-list cards. The interconnecting lines are not drawn by this program and must be drawn by hand to complete the drawing. Since the symbols and designation information consume 90% of hand drafting time, the Auto-Draft program offers considerable design assistance.

Notes:

1. This program is written in FORTRAN IV (98.8%) and COMPASS (1.2%) to be utilized on the CDC-3200 computer. In addition, the program is written in FORTRAN IV (98.8%) and ASSEMBLER (1.2%) for IBM-360 computer using OS/360.
2. Inquiries concerning this program should be directed to:

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   112 Barrow Hall
   University of Georgia
   Athens, Georgia 30601
   References: GSC-11539 for CDC-3200
   GSC-11526 for IBM-360

Source: J. B. Billingsley
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(GSC-11539, GSC-11526)