September 1972

B72-10391

NASA TECH BRIEF

NASA Headquarters

A Simplified, Compact Static Shift Register

The problem:

The large number of field-effect elements used in flip-flops employing the full master slave principle requires many components and results in a high packaging density.

The solution:

A static shift register stage has been developed which uses only one D Type flip-flop rather than the usual flip-flop pair in a master-slave arrangement. This new arrangement improves packaging density by approximately 25%.

How it's done:

The clock in the illustrated circuit is normally low. In this condition, the transmission gate (T1 and T2) is conductive and transmits the datum content of the previous stage through input D to the storage node, which is so labeled in the circuit diagram. With the clock low, the two inner series devices in the first inverter, T5 and T6, are nonconductive, disabling the first inverter which has the new data content ready on the two outer devices, T3 and T4. The second inverter (which is activated due to the inner devices, T9 and T10, being conductive) and the third inverter are connected back to back to form a flip-flop which is holding the previously stored datum; this information may be either a "1" or a "0".

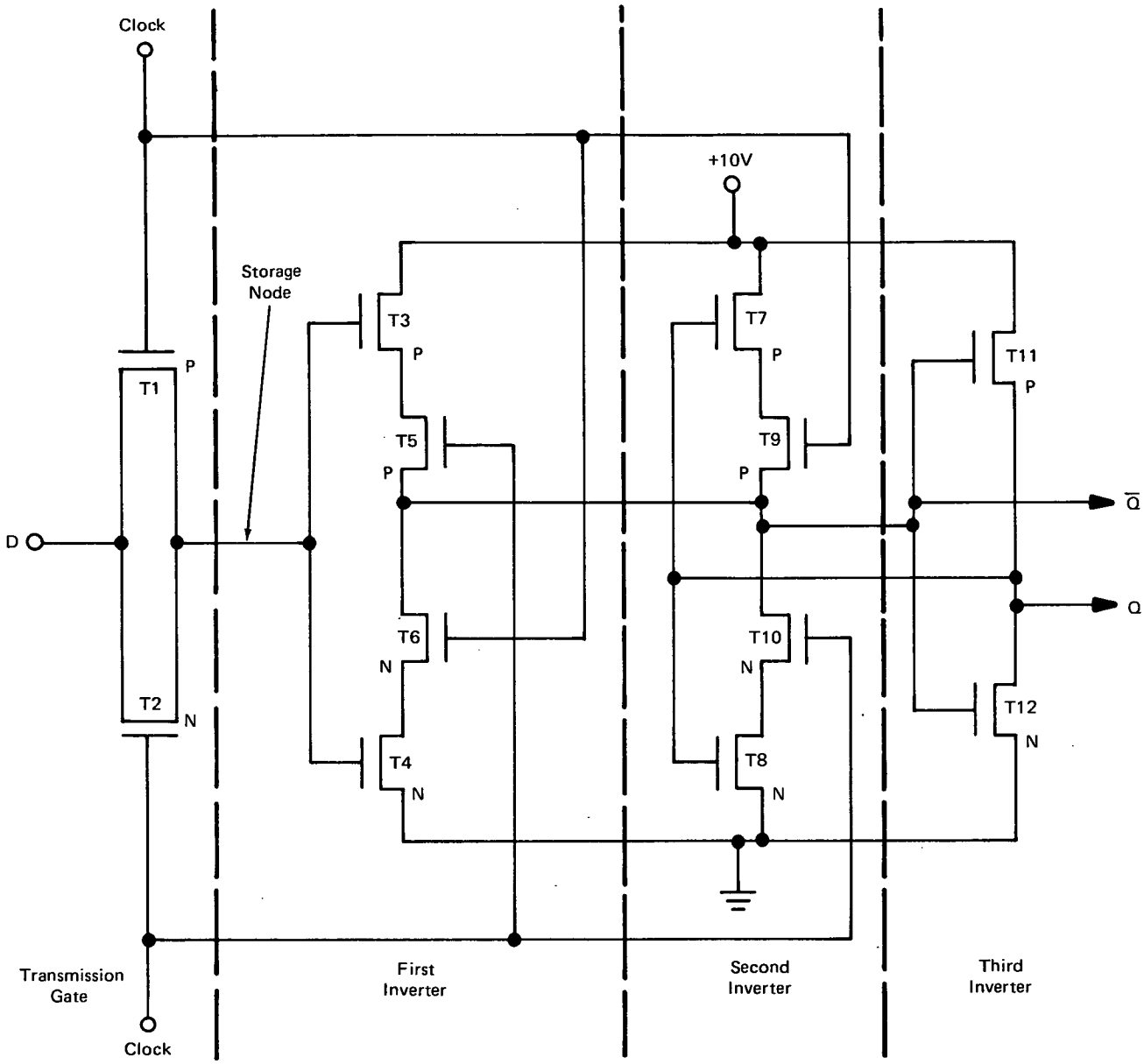
When the clock goes high, the transmission gate (T1 and T2) becomes nonconductive, preserving the datum at the time of clock rise at the storage node, which is now isolated from input D.

Simultaneously the second inverter is disconnected from the supply voltages by the transition to a nonconductive state of T9 and T10. Its output and the output of the first inverter are tied together, and the first inverter has now become operative through the transition to a conductive state of T5 and T6. The latchnig action of the flip-flop is no longer operative under these conditions. The new datum at the storage node has now replaced the old datum at the outputs. The inverse of the datum entered at D (supplied by the first inverter) now appears at $\overline{Q}$, and the direct datum (re-inverted by the third inverter) appears at Q.

When the clock returns to low, the proper logic level for the new datum is already controlling T7 and T8 in the second inverter, which is becoming activated again through the conductance of T9 and T10. With the latch reactivated, the datum which was entered when the clock became high is now stored. A new datum can once again enter the storage node which is once again isolated from the flip-flop.

In effect, this circuit is a compromise between a full master-slave arrangement with two complete static flip-flops and four double transmission gates and a dynamic shift register which cannot provide permanent storage. Thus, the advantages of each conventional circuit are utilized without the disadvantages. The only time dependent limitation is in the length of time that the clock can be held high during the entry of new data. The saving in component area over a full master-slave is considerable since there are only 12 transistors as opposed to 16.

(continued overleaf)



Note:

Requests for further information may be directed to:
Technology Utilization Officer
NASA Headquarters
Code KT
Washington, D. C. 20546
Reference: B72-10591

Patent status:

NASA has decided not to apply for a patent.

Source: Richard L. Pryor and Allan M. Smith of
RCA Corp.
under contract to
NASA Headquarters
(HQN-10723)