NASA TECH BRIEF
Manned Spacecraft Center

Dual Redundant Core Memory Systems
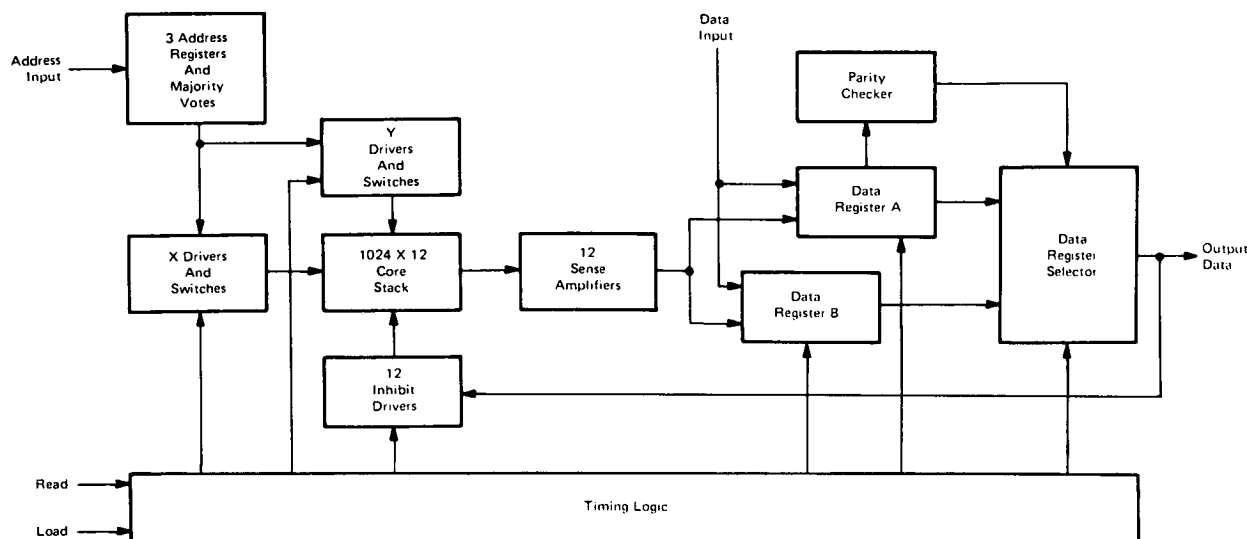
A dual redundant core memory system prevents loss of memory data when a single drive circuit failure occurs. The system requires two address locations and a parity bit for each word. It incorporates series redundant drive switch circuits, triple redundant majority voted memory timing functions, and two data registers to provide functional dual redundancy. The signal flow through these circuits is shown in the figure.

To load a word into the memory the initial storage address is transferred into three address registers. A 12-bit data word (11 data bits and one parity bit which generates odd parity) is transferred into the two data storage registers A and B. A load signal is then transmitted to the timing section. This causes the following sequence of events to take place in the memory system.

1. The data in register A are loaded into the core stack at the address location designated by the address registers (an address from 0 to 511).
2. The three address registers and the data register B are complemented.
3. The data in register B are loaded into the core stack at the address location designated by the address registers (an address from 512 to 1023).
4. The three address registers are again complemented and then incremented by one.

The x and y drivers are arranged so that none of the drive circuits that load data from register A into the core memory will be used to also load the corresponding data from register B. The data word now stored in the memory is contained at two different address locations; one address between 0 and 511 and a second address between 512 and 1023. The numerical value of the second address is the binary bit complement of the first. The data word, stored in the second address location, is equal in value to the bit complement of the data word located in the corresponding first address.

Because the inhibit drivers are series redundant and cannot be turned on inadvertently, the only error that can be caused by a single failure is to load a logic "1" instead of a logic "0" in that bit position. Should this occur in one of the inhibit drivers, one of the two related addresses now loaded will still contain the correct

data, the other will be incorrect by one bit (will have even parity). If an x or y driver or switch is open, one of the two words will still be correct and the other will have all "0's" (even parity). Additional words are loaded in a similar manner, except that a new initial address may not necessarily be transferred into the address registers. If not, loading is continued by loading sequential address locations.

To read data from the memory, the initial address from which data are to be read out of is transferred into the three address registers and a read signal is transmitted to the timing section. This causes the following sequence to take place in the memory system:

1. The data stored in the core stack at the address designated by the three address registers are read out into the data register A. They are then restored back into the same address location (an address between 0 and 511).

2. The three address registers are complemented.

3. The data stored in the stack at the address now designated by the three address registers are read out into data register B. They are then restored back into the same address location (an address between 512 and 1023).

4. Memory register B is complemented.

5. The parity bit, located in register A, is checked. If the parity is odd, the data selector transmits the data in register A to the output data lines. If the parity is even, the data selector transmits the data register B to the output data lines.

6. The three address registers are again complemented and incremented.

Additional words are read from the memory in a similar manner except that a new initial address may not necessarily be transferred into the address registers. If

not, reading continues by reading sequential address locations.

Failure modes in a sense amplifier will either give a logic "1" output or logic "0" output regardless of the sense inputs. When reading a redundantly stored word, as described above, the output bit from the failed sense amplifier will be correct in one of the two data registers, and the register receiving the wrong output will have even parity.

Thus, regardless of any single failure in the memory system the resultant output data will be correct. Also, because the address registers, timing, x and y drive, and inhibit-sense-data register sections are independent of one another for redundancy considerations, many multiple failure modes may be tolerated without the loss of stored data.

This system may be of use where extreme computer reliability is required.

Note:
No additional documentation is available. Specific questions, however, may be directed to:
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No patent action is contemplated by NASA.

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