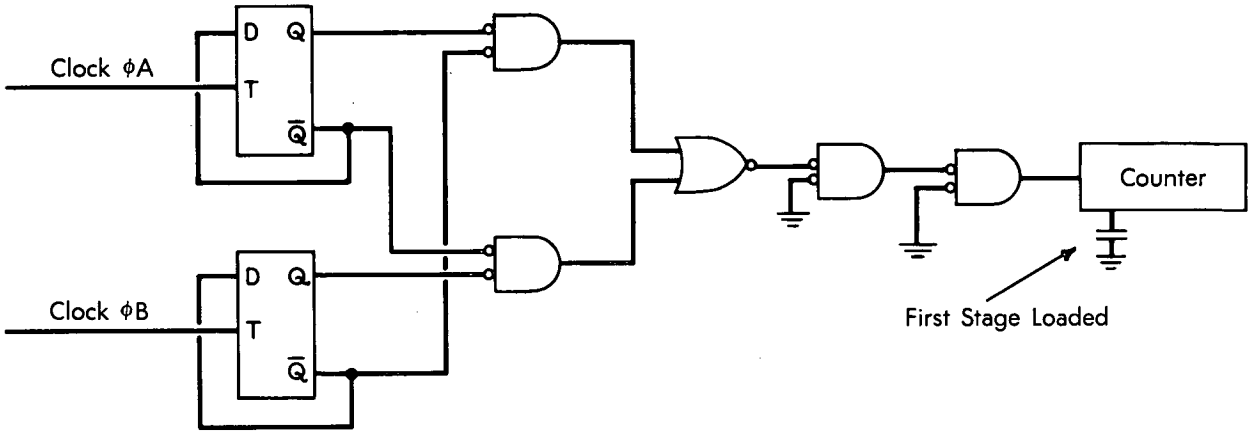
NASA TECH BRIEF

Ames Research Center

Speed Enhancement of Complementary MOS Devices

Space applications of solid-state digital circuits require low power dissipation and often are required to operate at high speeds. Frequently, high speed characteristics are sacrificed in order to limit power requirements — or power budgets are violated to ensure operation at desired speeds.



The "Sisyphus" experiment for a Pioneer probe required the operation of a binary counter at 4 MHz at low levels of power consumption, with bipolar TTL in the higher-speed portions of the circuits. Minimum weight requirements for the circuitry indicated the necessity of high-density packaging. As a result of high-density packaging, the logical gain-bandwith product of the devices used was significantly increased; this was attributed to short, low-capacity interconnections.

Since complementary MOS devices operate at higher speeds as power supply voltages are increased, and the speed of operation of high-impedance circuits is limited primarily by capacitive load, an investigation was made of the effects of combining a supply voltage higher than nominal with low reactance interconnections. It was found that speeds far in excess of the "typical" parameters suggested by manufacturers of MOS devices could be achieved, and that the speed required for the space experiment could be attained at supply voltages well within component limitations.

The circuit shown in the diagram is typical for the high-speed applications required for the experiment. It was tested for maximum speed of operation at room temperature for 22 samples of counter circuits, and at −45.6° and 65° C for two samples classed as "fastest" and "slowest". The tests were conducted with loads simulating the proposed application and with different values of supply voltage. (Flip-flop and gate samples were limited, but substitution of one sample in each location produced only

(continued overleaf)

minor changes in maximum speed.) The signals were "normalized" by a flip-flop and traversed four stages before triggering the counter.

The counter circuit used in the tests characteristically operates at 2.5 MHz at 10 V; 6.16 MHz were attainable at a power supply of 8 V, and 8.96 MHz at 12 V when used in high density packages.

Note:

No additional documentation is available. Specific questions, however, may be directed to:

Technology Utilization Officer
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Patent status:

No patent action is contemplated by NASA.

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