May 1972 B72-10149

NASA TECH BRIEF

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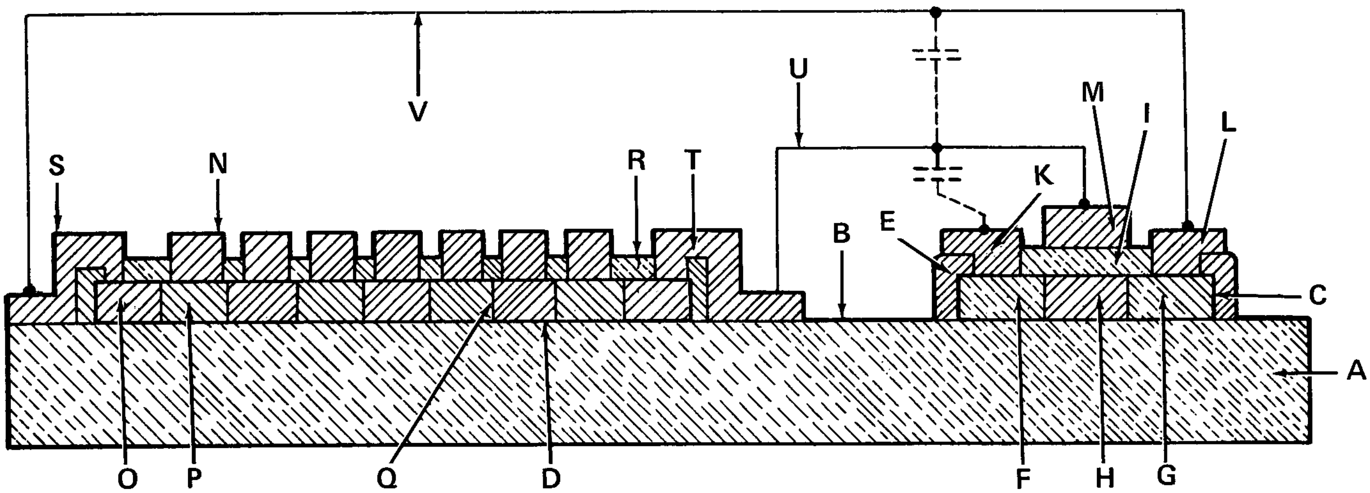
Gate Protective Device For Insulated Gate Field-Effect Transistors



Insulated gate field-effect transistors are well known and comprise source and drain regions of one type of conductivity semiconductor material separated by a channel region of the opposite type of conductivity material. Electrodes are provided in direct contact with each of the source and drain regions, and a gate electrode is provided overlying the channel region but separated by a relatively thin layer of a dielectric material. One problem associated with these devices is that frequently during handling a static electric voltage is developed between the gate electrode and the channel region causing voltage breakdown of the gate insulating layer and, consequently, damage to the device.

To protect the transistors from such damage, various circuit methods have been devised. Generally, these methods comprise low voltage breakdown devices connected between the gate electrode and the channel region of the transistor, whereby the static voltage is discharged through the device substrate along paths other than through the gate insulating layer.

One recently devised protective device is particularly useful for protection of insulated gate field-effect transistors formed in thin films of semiconductor material. A chain of diodes is formed in a back-to-back configuration as an integral part of the transistor structure. In the structure, the substrate (A) is composed of a crystalline insulating material such as sapphire or spinel. On one surface of the substrate, two thin films (C, D) of a semiconductor material, e.g. silicon, are disposed but are spaced apart. A field-effect transistor (E) is disposed within the film and comprises a source region (F) and a drain region (G), both of P conductivity, and a channel region (H) of N conductivity. A layer of a dielectric material, (I), e.g. silicon dioxide covers the surface (J) of the semiconductor material film (C). Source (K) and drain (L) electrodes are provided on the surface of the layer (I) and make contact with their respective regions through openings in the layer. A gate electrode (M) is located on the dielectric layer (I) overlying the channel region (H).

The protective device (N) for the transistor (E) is disposed within the film (D) and comprises a plurality of contiguous regions of semiconductor material of alternating conductivity. Thus, five regions (O) of N

(continued overleaf)

conductivity are provided, alternating with four regions (P) of P conductivity with each contiguous pair of regions having a PN junction (Q) between them and constituting a zener or avalanche diode. Due to the alternating of the type of conductivity of the contiguous regions (O) and (P), adjacent diodes are of opposite polarity and the row of diodes are connected in a back-to-back relationship.

A layer of protective material (R) e.g. silicon dioxide, is deposited over the film (D). The conductive terminals (S, T) contact the two end regions (O) of the device (N) through openings in the layer of protective material. One terminal (T) is electrically connected by means of a connector (U) to the gate electrode (M) of the transistor (E) and the other terminal (S) is connected electrically by means of connector (V) to either the source or drain electrode of the transistor. Reliability of the device is improved by using layers of a conductive material such as aluminum or tungsten on top of each alternating semiconductor material region. Separation of the layers is necessary to prevent shorting out the junctions between the alternating regions.

Notes:

1. Information concerning this innovation may be of interest to the designers and manufacturers of solid state circuits, devices, and systems.
2. Requests for further information may be directed to:

   Technology Utilization Officer
   Marshall Space Flight Center
   Code A & TS-TU
   Huntsville, Alabama 35812
   Reference:B72-10149

Patent status:

Inquiries about obtaining rights for the commercial use of this invention may be made to:

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