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# NASA TECH BRIEF

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## Topological Solution of Bilateral Switching Networks

The design of monolithic logic circuits utilizing metal oxide semiconductors (MOS) is usually preceded by a mathematical analysis which seeks to minimize component count. A topological method has been developed for synthesizing many bilateral switching networks without resorting to Karnaugh mapping or similar sophisticated methods that are often supplemented with a great deal of intuition.

The topological method uses the eye as a pattern detector to trace the path of transmission directly on a truth table. As a rule, such patterns are readily recognized since a truth table is an orderly and unambiguous statement of the problem. Unlike conventional mapping or algorithmic methods, selection of pathways is continually supervised by the logician, thus allowing him to seek a planar iterative solution desirable for the fabrication of monolithic circuits. A planar network does not contain wiring crossovers; this permits a single level of metallization on the substrate. An iterative network allows the use of the

“step-and-repeat” photography that is desirable for Large Scale Integration (L.S.I.). Achieving a planar iterative network may be more important in L.S.I. design than obtaining a minimum component count. For any event, the desired tradeoffs in design considerations may be more readily achieved by the topological method than by combinational logic methods because the eye observes the various bit patterns in the truth table and thus prompts selection of the network which meets desired objectives.

As an example, the truth table shown in figure 1 contains five allowable “truth” statements where only one of the five elements is true at one time, indicating that there are no shorts between elements. Figure 2 shows the topological solution super-imposed on the truth table; for simplicity, relay contacts are shown instead of MOS implementation, for MOS devices are solid-state analogs of conventional electromagnetic relays. For each variable a contact selects

A	B	C	D	E
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	1	0	0	0
1	0	0	0	0

Figure 1

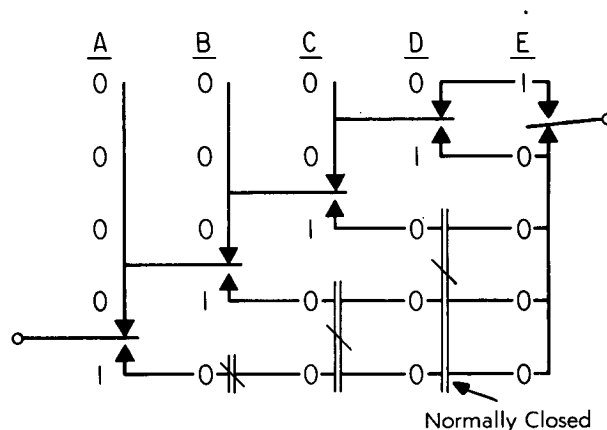


Figure 2

(continued overleaf)

between the "0" or "1" state; a normally-closed contact provides the "0" state and a normally-open contact provides the "1" state. Figure 3 shows the same solution in conventional form using relay contacts, and the solution is essentially identical when implemented with MOS devices. It is to be noted that an output is obtained when only one of the variables changes its state, and that there is no output

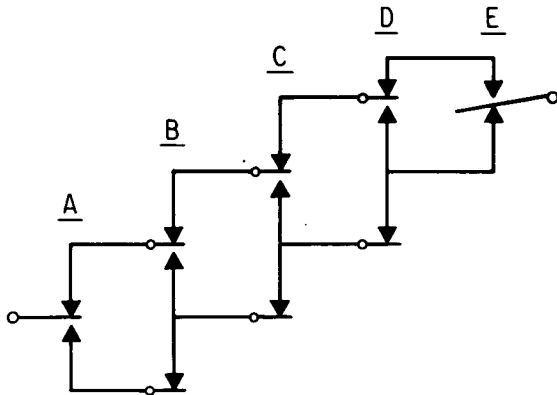


Figure 3

for any of the other possibilities (a short between two or more variables). Because of the apparent symmetry, the same solution can be used for a multiplicity of variables represented by a single output.

The topological method can be applied to synthesize networks for multiple output functions, parity generators, full adders, bit comparators, etc.

**Reference:**

Mazer, Louis: Topological Solution of Bilateral Switching Networks. IEEE Transactions on Computers, p. 234, February 1971.

**Note:**

No additional documentation is available. Specific questions, however, may be directed to:

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**Patent status:**

No patent action is contemplated by NASA.

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