SOLID STATE POWER CONTROLLERS

JACK C. BOYKIN
AND
WILLIAM C. STAGG

MANNED SPACECRAFT CENTER
HOUSTON, TEXAS

AND

DONALD E. WILLIAMS

MARSHALL SPACE FLIGHT CENTER
HUNTSVILLE, ALABAMA

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Jack C. Boykin

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William C. Stagg

NASA-Manned Spacecraft Center
Houston, Texas

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Donald E. Williams

NASA-Marshall Space Flight Center
Huntsville, Alabama

SUMMARY

A spacecraft PDC (power distribution and control) subsystem utilizing solid-state switching elements and capable of being computer controlled offers many potential advantages over systems using conventional electromechanical switching devices. These include higher reliability, longer life, a more rugged system, more flexibility, and an inherent compatibility with other advanced avionics subsystems. The trend in spacecraft design is toward larger, more sophisticated vehicles with correspondingly larger and more complex systems requiring electrical power. This trend has resulted in increasing numbers of power distribution paths and power-switching functions, in addition to requirements for cleaner (transient-free) electrical power to supply the complex avionics systems. This paper addresses one of the potential improvements in the PDC subsystem which is being strongly considered for these program and system interface requirements, the SSPC (solid-state power controller). The paper presents the basic functions of the SSPC, some of the basic design concepts thus far evolved for performing these functions, and some of the considerations involved in both the design and application of these devices. Spacecraft systems requirements as well as the potential results of applying SSPC's in an approach to meeting these requirements are presented. Finally, this paper presents the development status of SSPC's to date, along with the requirements for further development of the devices, systems, and concepts necessary to take full advantage of this technology.

INTRODUCTION

Spacecraft system designs and component applications have always drawn heavily on aircraft program experience. The Space Shuttle will be no exception, and may increase the dependence on aircraft experience due to its aircraft modes of flight. In the area of PDC (power distribution and control), relatively few improvements have been generated by aircraft systems in the last 20 years. However, as interfacing subsystems become more complex and payload delivery requirements increase, the PDC subsystem must be improved or it will become a significant burden on other systems.

POWER CONTROLLER FUNCTIONS

The SSPC will provide four basic functions or capabilities in an advanced PDC subsystem: (1) switch power ON and OFF to a load from a bus, (2) provide circuit overload protection, (3) provide remote control and monitoring of these functions, and (4) provide current limiting during overload conditions.

All of these functions except current limiting have been provided in the past by various combinations of toggle switches, circuit breakers, fuses, relays, and motor switches. In addition to the obvious advantages of replacing several types of devices with one single device to perform the many functions required by a system, the SSPC has the added advantage of reducing the total number of switching elements required since each load circuit of a conventional system normally employs a circuit breaker and one or more of the other switching devices in order to provide full functional capability. The current limiting function is not only advantageous from a safety hazard viewpoint, but also will offer great improvements to the entire electrical power system by reducing the transients normally generated during switching and fault conditions.

POWER CONTROLLER FUNCTIONS

- SWITCHES POWER ON AND OFF BETWEEN A BUS AND A LOAD
- PROVIDES CIRCUIT OVERLOAD PROTECTION
- REMOTE CONTROL CAPABILITY
- SHOULD PROVIDE CURRENT LIMITING DURING OVERLOAD CONDITIONS

BASIC SSPC DESIGN

The SSPC's envisioned for Shuttle application suffer from a problem common to programs implementing advanced technology; i.e., theory and breadboard knowledge far outweigh flight applicable hardware production. A major contributor to this condition is, of course, the lack of funds for manufacturers to pursue flight packaging development. This is a condition beyond the control of the power systems designer. Another major factor contributing to the situation is the lack of detailed system requirements presented to the SSPC designer to provide the real requirements on the SSPC. This problem is being studied by the power systems designers for the Shuttle; however, until sufficient details of the Shuttle system designs and requirements are generated, the limited availability of funds forces power systems designers to be hesitant in hardening detailed requirements. These circumstances have led to varying design concepts by manufacturers of a solid-state, current sensing switching device. The next portion of this paper will deal in more detail with several design approaches and the advantages and disadvantages of each.

To better understand the differences in the designs to be presented, a review of the basic design concepts pursued in early SSPC programs is in order. Figure 1 shows the basic building blocks of a d.c. SSPC. The power switching transistor must have sufficient voltage and power dissipation rating to be compatible with the system transients and the overload and circuit protection modes of operation. The regulator is used to provide a buffer effect so that the voltage to the internal circuitry is relatively independent of bus-voltage variations. The driver circuit must put the power transistor into deep saturation to provide low voltage drop and power dissipation. A d.c. to d.c. converter can be used to provide this drive power and at the same time provide the signal-to-load isolation required by computer control systems such as the Shuttle proposes. The overload circuit protection interfaces with the current sensing element and the drive circuitry to provide the circuit breaker function with the added improvement of an actual current limiting capability. A current fold-back is allowed for increased voltages to hold the power dissipation of the semiconductor within limits and help prevent the semiconductor junction from rising above its rated value during the worst case conditions of a high voltage transient on the input and a short circuit on the output. In order to protect the SSPC and optimize the PDC subsystem operation, a trip-out circuit is provided to turn off the power switch and indicate with a trip signal that the action has occurred. Reduced tripping times for higher voltages are designed to allow MIL-STD-704 transients without nuisance tripping and still allow the designer to give as much protection as possible to the semiconductor switch.

DC POWER CONTROLLER

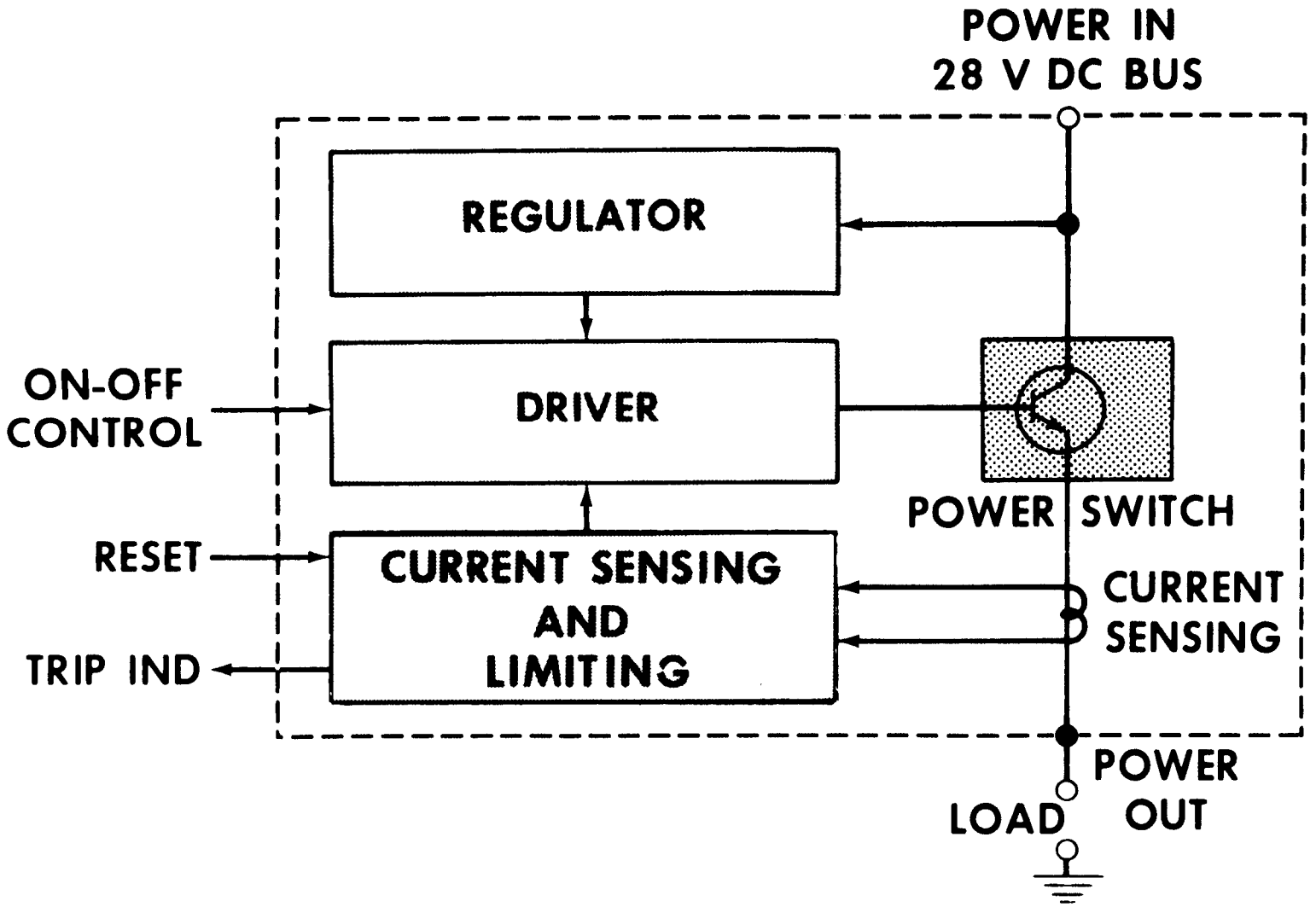


FIGURE 1

DESIGN CONSIDERATIONS

It should be evident from the previous discussion that SSPC's are not simple components such as the electromechanical components (relays, circuit breakers, etc.) used in conventional PDC subsystems. They are indeed very complex, multi-technology semiconductor devices employing not only power semiconductors, but also thin and thick film integrated circuits. This compexity, along with PDC subsystem requirements, leads the SSPC designer to consider five important points in his design and to attempt to optimize all of these.

a. Low Dissipation and Voltage Drop. Low dissipation in both the "ON" and current-limiting modes is important from the standpoint of obtaining maximum efficiency in the PDC system and from the standpoint of minimizing the thermal stresses to which the power semiconductor device is subjected. Designing for the lowest dissipation possible also has a profound effect on the maximum SSPC current rating achievable with current state-of-the-art power semiconductors. Low voltage drop across the SSPC is also very important both because it affects the dissipation in the device and because of the effect it has in minimizing the wire gauge required in order to maintain acceptable voltage limits at the load equipment.

b. High Current Capability. As discussed previously, the degree of success which the SSPC designer achieves in minimizing the power dissipation within the device plays a major role in determining the current rating of the device and consequently the maximum current rating obtainable with state-of-the-art semiconductors.

c. Current Limiting. Current limiting is a very desirable feature in SSPC's because of its effect in minimizing transients on the power bus due to overloads and faults. Various parameters, such as system voltage, power semiconductor ratings, and SSPC design techniques affect the degree of current limiting available with any particular SSPC design. In some cases, power dissipation in the current-limiting mode goes so high as to render that mode of operation impractical.

d. Control/Output Isolation. Isolation between the control input circuitry and the power handling output circuitry is important because of the possibility of inducing EMI from the power bus into the data bus control system and adversely affecting its operation. Because of the fact that the solid-state circuits, unlike their electromechanical counterparts, do not offer inherent isolation, special consideration must be given to this requirement. Two techniques commonly used to provide isolation are solid-state optically coupled devices and transformer coupling between the control input and the drive stage.

e. Low Leakage in the "OFF" State. This characteristic is important because of its effect on the overall efficiency of the PDC subsystem and generally restricts the designer to the use of silicon rather than germanium power semiconductors.

DESIGN CONSIDERATIONS

- LOW DISSIPATION AND VOLTAGE DROP
- HIGH CURRENT CAPABILITY
- CURRENT LIMITING
- CONTROL/OUTPUT ISOLATION
- LOW LEAKAGE IN 'OFF' STATE

DESIGN APPROACHES

Figures 2 to 5 present various design approaches which have been put forward thus far. Accompanying each figure is a brief discussion of the advantages and disadvantages of each approach. As will be seen, in some cases, optimization of one design consideration leads to compromises in other areas.

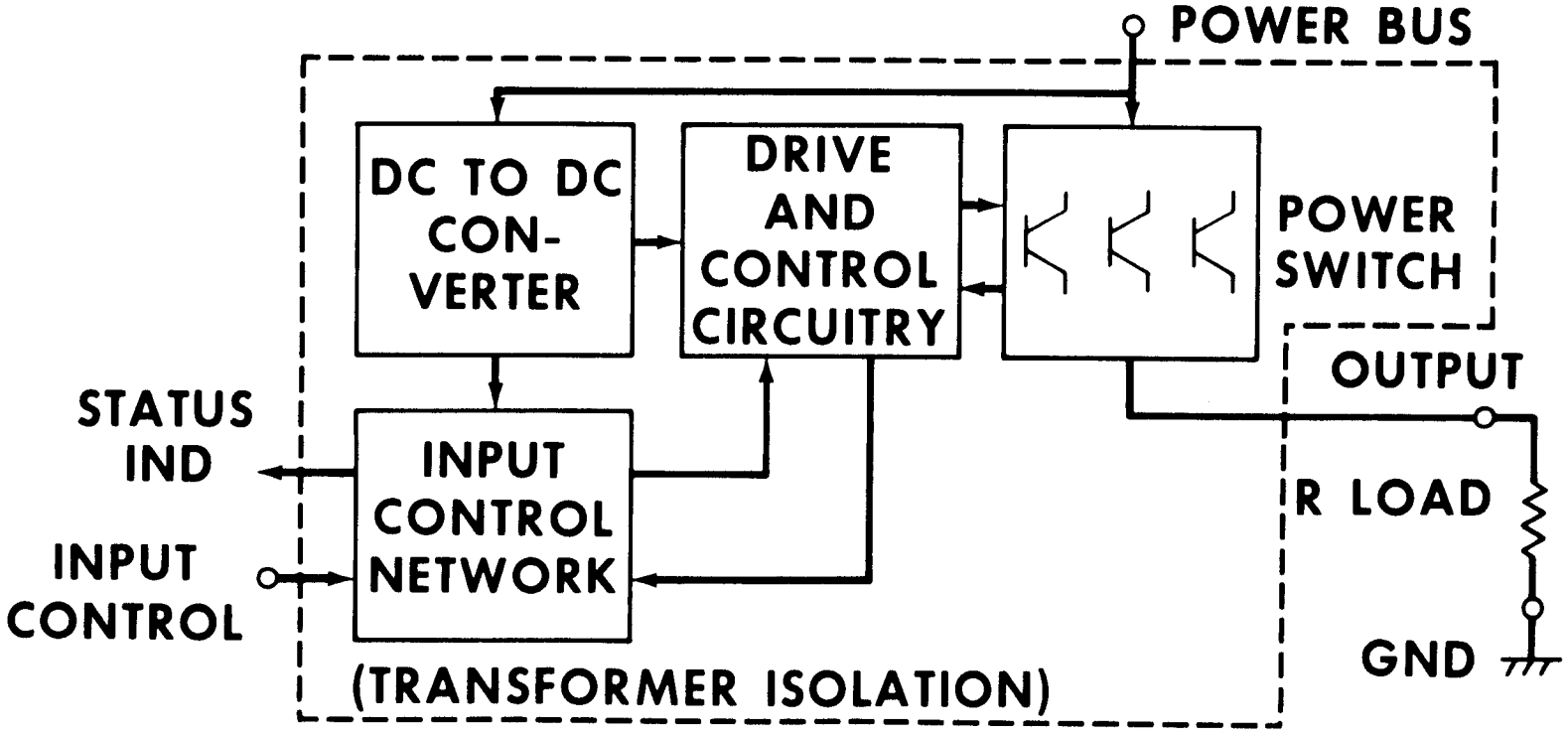
Figure 2 illustrates a design which uses a transistor in deep saturation as the power switch for normal operation. When an overload exists, the base drive to the power output transistor is decreased so that the transistor now operates in its active region to achieve current limiting. For SSPC ratings up to 5 amps, a single power transistor is employed; for higher ratings, two or more power transistors may be paralleled in order to maintain the power dissipation in each transistor within acceptable limits during all modes of operation. This particular design uses transformer coupling to achieve isolation between the control input and power circuitry.

This design has two distinct advantages. During normal operation, the single transistor in deep saturation provides a low voltage drop and consequently low power dissipation in the SSPC. This design also provides a current limiting mode of operation which is a very desirable feature because of its effect in minimizing transients on the power bus.

One disadvantage of this design is the fact that its internal power supply for the control electronics continues to draw power in the "OFF" state which, when added to the leakage of the power transistor, decreases the efficiency of the PDC subsystem. A possible additional disadvantage is that if parallel power transistors are used for higher current ratings, some complexity may need to be added to the drive circuitry to insure that the power transistors turn on and off at the same time. Also, matching impedances may need to be added in series with each power transistor, thus increasing the voltage drop across the SSPC.

SATURATED OUTPUT

ACTIVE CURRENT LIMITING



ADVANTAGES

(1) LOW OUTPUT VOLTAGE DROP
(2) CURRENT LIMITS

DISADVANTAGES

(1) LOW EFFICIENCY IN 'OFF' STATE

FIGURE 2

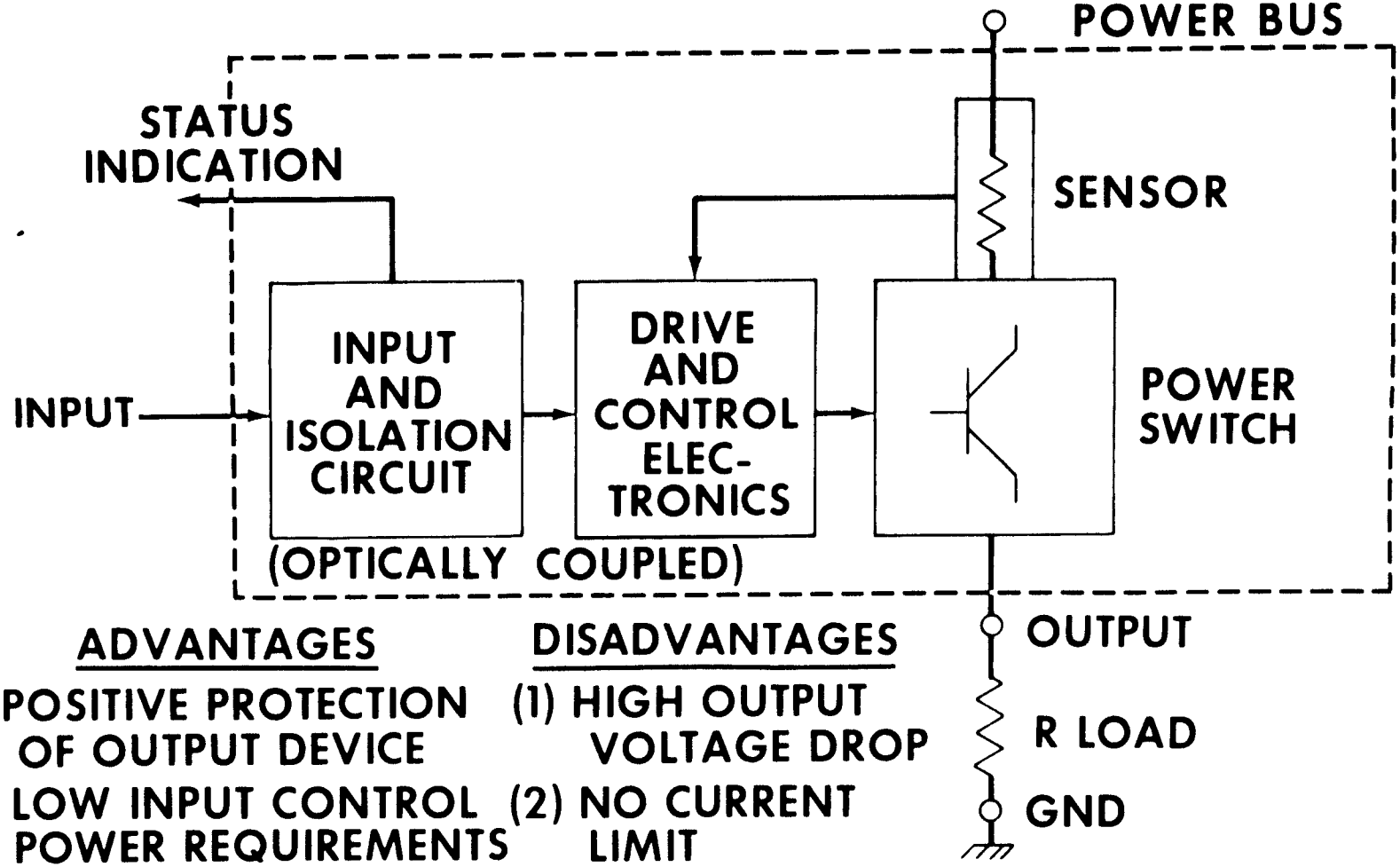
Figure 3 shows another design which employs a deeply saturated transistor as the power switch for normal operation. It differs from the previous example, however, in that overload sensing is accomplished by sensing the actual temperature of the power semiconductor chip. When an overload causes the temperature of the chip to rise to a predetermined critical value, typically 170°C, base drive to the power semiconductor is cut off, thus interrupting the overload current. With such a thermal sensing scheme, the SSPC can be made to be the equivalent of a mechanical "trip-free" circuit breaker. Another difference in this design is that it uses optically coupled semiconductor devices to achieve isolation between the control input and power circuitry.

The thermal sensing scheme offers some advantages and some disadvantages. It offers positive protection for the power semiconductor since the overload sensing method utilizes the parameter most critical to the semiconductor, i.e., the junction temperature. On the other hand, thermal sensing makes the overload trip point and time dependent upon the temperature of the surrounding environment and the heat sink to which the SSPC is mounted.

Some disadvantages to this particular approach are the fact that it does not provide a current limiting mode and it is possible that the combined voltage drop of the power semiconductor and the thermal sensing device may be excessive.

SATURATED OUTPUT THERMAL SENSING

NO CURRENT LIMIT



ADVANTAGES

(1) POSITIVE PROTECTION OF OUTPUT DEVICE

(2) LOW INPUT CONTROL POWER REQUIREMENTS

DISADVANTAGES

(1) HIGH OUTPUT VOLTAGE DROP

(2) NO CURRENT LIMIT

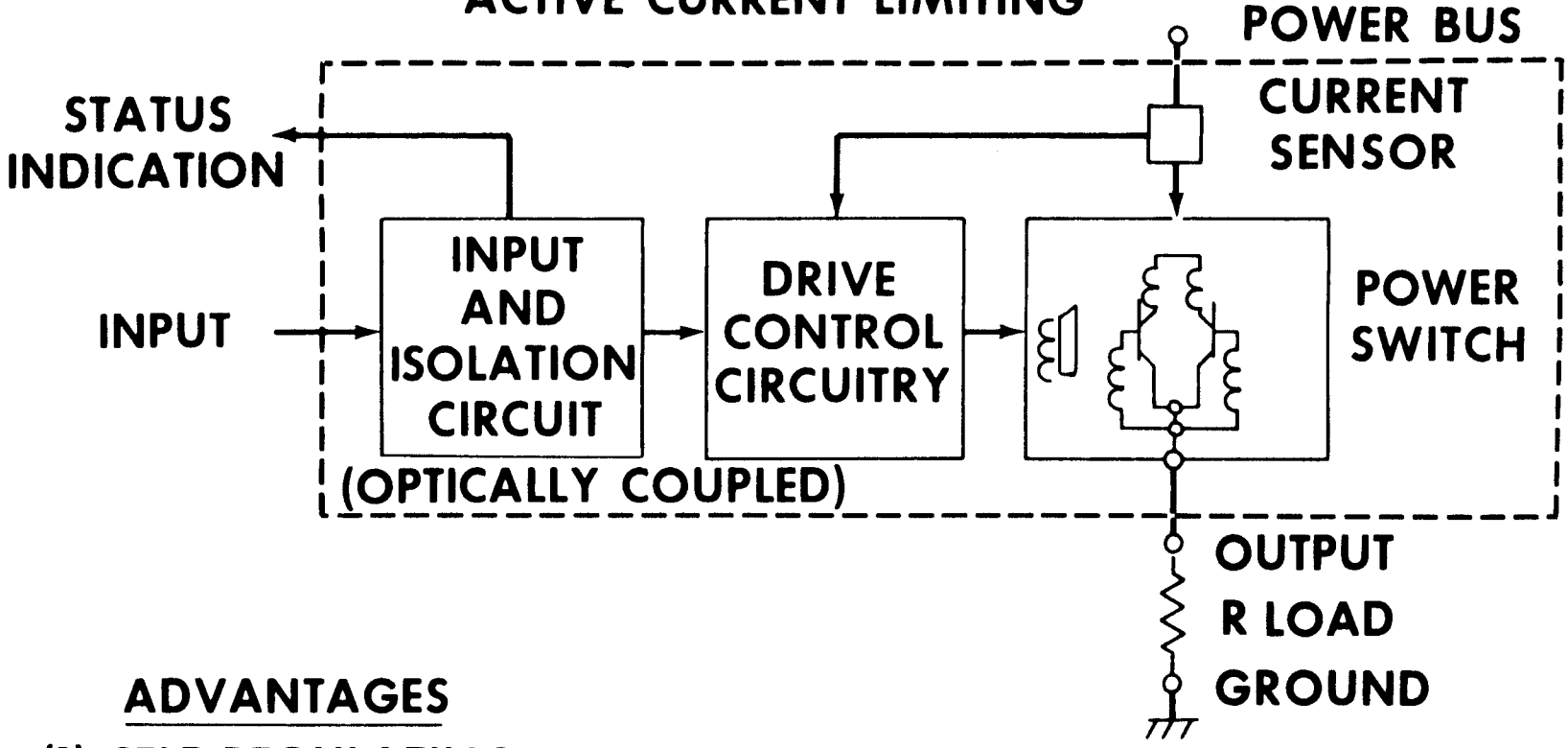
FIGURE 3

The design outlined in figure 4 is radically different from the first two presented and employs basically a saturated switching transformer driving the power output transistor and is similar in approach to a switching oscillator. By using this switching technique, the designer can accomplish time sharing of the load current between the two output transistors. Time sharing at a frequency below the thermal time constant of the output transistor can reduce the thermal stress of the transistor by allowing a finite cooling time between power pulses during normal and overcurrent conditions. This switching concept could be limited due to output noise generation and/or EMI-RFI generated by the current transformers. This problem could be severe enough that large and complex filtering networks might counter the advantages of the switching device.

This design uses optically coupled semiconductor devices to achieve control input isolation similar to figure 3.

CURRENT SWITCHING OUTPUT

ACTIVE CURRENT LIMITING



ADVANTAGES

(1) SELF-REGULATING
(2) LOW INPUT POWER
(3) HIGH EFFICIENCY IN 'ON' STATE

DISADVANTAGES

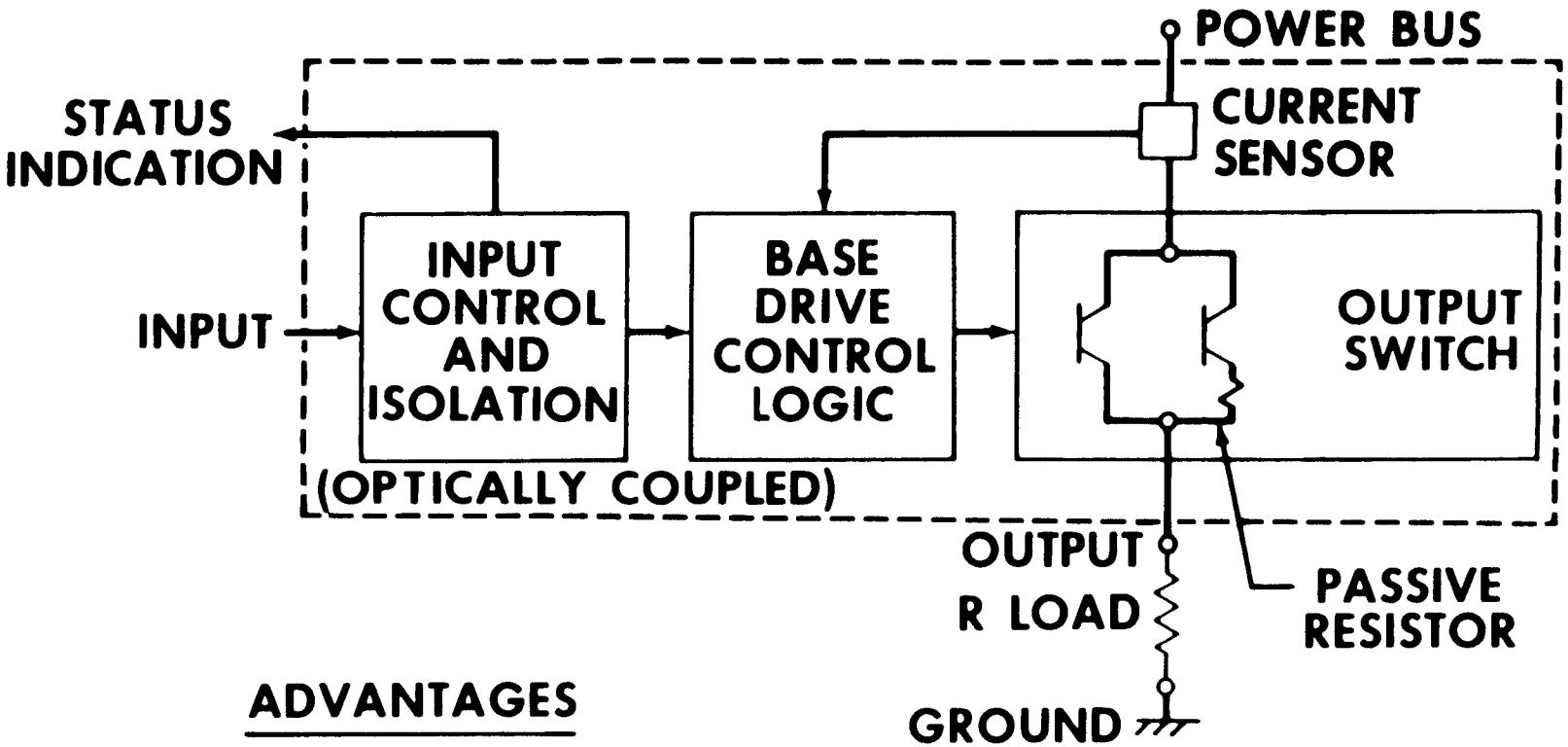
(1) POSSIBLE NOISE ON OUTPUT LINE
(2) RFI-EMI GENERATION

FIGURE 4

Figure 5 illustrates another concept different in basic philosophy from those previously presented. This approach proposes current limiting by a means other than high power dissipation in the output transistor. Using a dual output power stage, the first path is active during normal load conditions and a separate path is used for overload conditions. The first stage uses a single power transistor which is operated in a deep saturation state, thus allowing the low voltage drop characteristic. Under overload conditions, the first stage is turned off and the second stage is turned on. This stage consists of an output transistor (also operated in a saturated mode) in series with a power resistor which provides current limiting and a relief element for the main power switch during overload conditions in which high power dissipation is required. The major problem with this design is the complexity of the circuitry involved in switching from one stage to the other.

The examples presented here show only a few of the many possible circuit designs which could fulfill the Shuttle switching requirements if development is carried to completion. The technologies involved in these designs appear to be fully capable of meeting Shuttle requirements, leaving the designer with the prime task of hardening a concept and producing a candidate flight packaged unit for test and evaluation.

PASSIVE CURRENT LIMITING



ADVANTAGES

(1) CURRENT LIMIT
(2) LOW INPUT POWER
(3) LOW OUTPUT VOLTAGE DROP
(4) LOW POWER DISSIPATION IN OUTPUT TRANSISTORS

DISADVANTAGES

(1) INCREASED COMPLEXITY
(2) RFI-EMI GENERATION

FIGURE 5

ADVANCED SPACECRAFT TRENDS AFFECTING THE POWER DISTRIBUTION AND CONTROL SUBSYSTEM

The overall Shuttle Program requirements emphasize the shortcomings of a conventional PDC subsystem and point out the three basic trends in spacecraft design which make PDC subsystem improvements mandatory: (1) automation, (2) reuseability, and (3) system size.

Automation

The advances in electronic technology in recent years have made digital computer capability a realistic flight item which has been utilized by individual avionics subsystems to improve upon their capabilities. This has resulted in increased sophistication and capability of these systems. This has allowed the use of automated functions for not only increasing the accuracy and speed of the functions, but also reducing man's workload. The effectiveness of this automation is presently reduced somewhat due to the unavoidable interfaces with the conventional PDC subsystem. Presently applied solutions to this problem involve complex and heavy hardware such as the Apollo sequencer system to allow even a minimal number of automated functions. The interfacing subsystems implementing the advanced electronic capability available to them are also more susceptible to the transients generated by the conventional PDC systems interfaces. Their circuits must usually suffer reliability, weight, and simplicity penalties to counter this transient susceptibility.

Reuseability

Typical Shuttle planning calls for mission cycles in the hundreds and program life of up to ten years. Present PDC subsystem components are not regarded as suitable for spacecraft application under these conditions due to the normal degradation processes of mechanical wear and tear. Solid-state devices substituted for these components offer a potential for approaching an unlimited life component.

System Size

Perhaps the driving function in the requirement for an improved PDC subsystem is the trend towards a larger system. The vehicle being designed is on the order of 200 feet in length, with electrical power requirements higher than ever before on a space vehicle. A conventional PDC subsystem to service this type of system involves extremely heavy, complex and inflexible wire harnesses, as well as large quantities of power handling electromechanical devices which are subject to wear and limited cycle life.

ADVANCED SPACECRAFT TRENDS AFFECTING THE PDC SUBSYSTEM

- AUTOMATION
  - REMOTE CONTROL
  - COMPUTER COMPATIBILITY
- REUSEABILITY
  - 10 YEAR, MULTI-MISSION SYSTEMS
- SYSTEM SIZE
  - PHYSICAL DIMENSIONS
  - POWER REQUIREMENTS
  - DISTRIBUTED BUSES

DISTRIBUTED POWER BUS SYSTEM

In order to optimize the PDC subsystem in a Shuttle with the aforementioned characteristics, the basic change from conventional systems to a distributed power bus system with remote control is mandatory. A typical Shuttle distributed bus arrangement is shown in figure 6. The main power control stations are located as nearly as possible to the prime power sources and have remote control capability. Remote PDU's (power distribution units) are located in various other strategic areas according to the location of the individual loads themselves. The PDU's feed power directly to the users through SSPC's which are controlled from the data bus system. The greatest advantage of this concept is the weight savings in wiring no longer required to be routed through the manual control elements in the crew area. Wire weight savings are also gained in removing the many individual wires required to carry power from central buses to each user in a remote area and replacing these with the one larger power feeder to a PDU. Individual wires must still distribute power from the PDU to each user, but over a relatively short distance. The major portion of the numerous individual wires is replaced by a single feeder larger than any one of the original wires, but much lighter than the sum of the wires replaced.

ELECTRICAL EQUIPMENT LOCATION

EXAMPLE

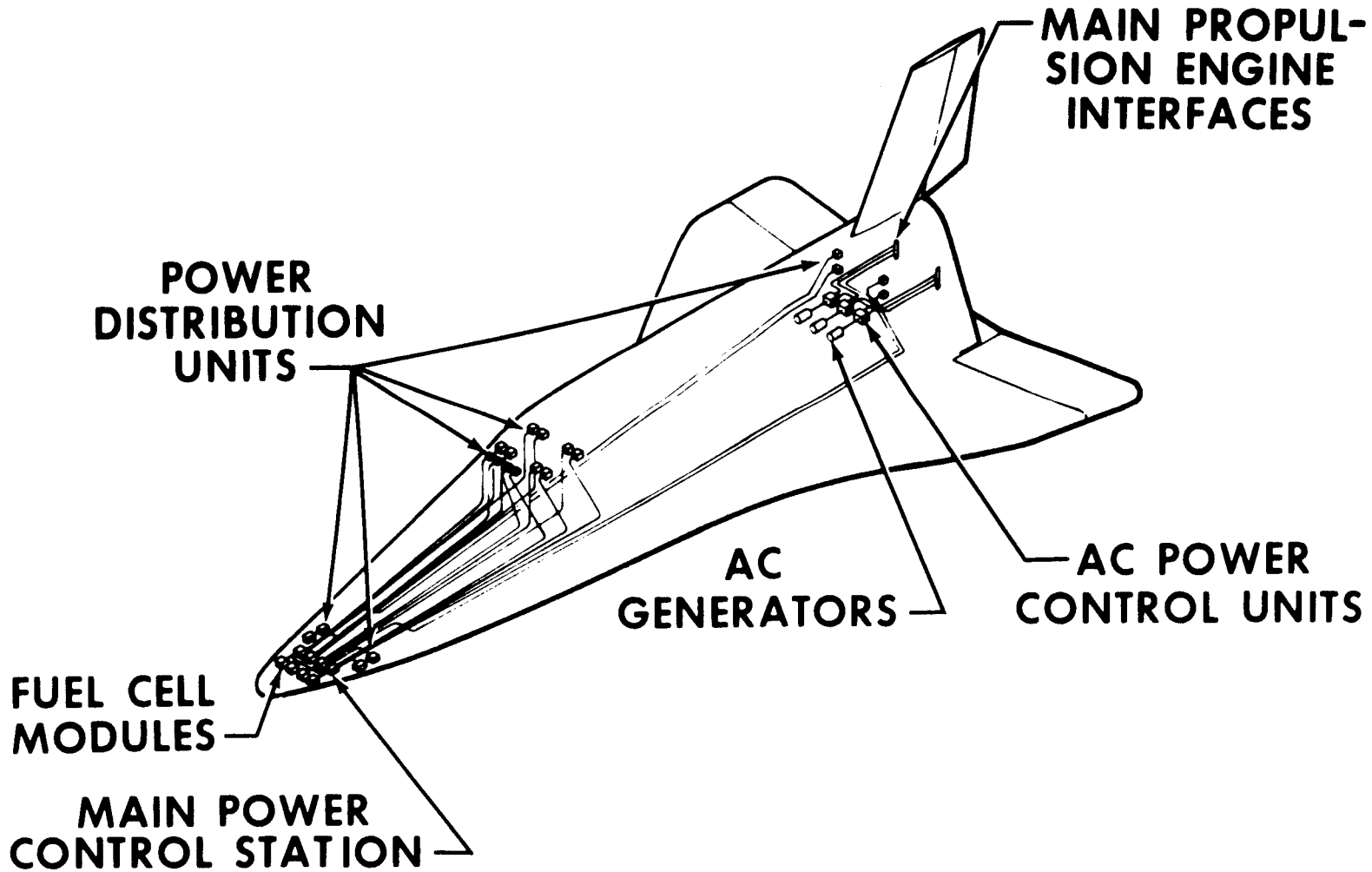


FIGURE 6

WEIGHT TRADE-OFF STUDIES

The potential weight savings previously discussed may be very significant for payload critical aircraft and spacecraft such as the Shuttle. The magnitude of this potential savings, however, is dependent on the system to which the concept is applied. Two systems which have received detailed trade studies in this area are the A-7 Aircraft and the Phase B Space Shuttle. As shown in table I, the potential savings are of significant magnitude to warrant further investigation into application of the SSPC concept. There are other areas of potential weight savings in the PDC subsystem which are receiving special study in conjunction with the SSPC concepts; for example, preliminary results indicate possible weight savings on the order of 15 percent with the application of flat conductor cable in the Shuttle.

WEIGHT TRADE-OFF STUDIES

APPLICATION	SYSTEM WEIGHT		REDUCTION, PERCENT
	CONVENTIONAL	SOLID-STATE	
A-7 AIRCRAFT	576 LB	315 LB	45
PHASE B SHUTTLE	2516 LB *	1998 LB *	21

* WITH FLAT CONDUCTOR CABLE THESE FIGURES WOULD BE 15 PERCENT LOWER

TABLE I

ADVANTAGES OF SOLID-STATE POWER CONTROLLERS

All of the improvements to the PDC subsystem previously discussed have depended on the application of a remote control power switch. Some of the inherent problems of mechanical contacts were mentioned earlier, and are well known to power system designers. Recent semiconductor technology advancements have provided us with a design concept which lessens, if not completely eliminates, the bulk of these problems while offering other system improvements at the same time.

One of the most important advantages the SSPC has over the electromechanical device is the inherent compatibility with a data bus control system. Low level control and monitoring of these solid-state devices establish the control system/power device interface with common hardware, whereas conventional power devices must undergo significant modification in order to accomplish this interface. Potential higher reliability, longer life, reduced EMI levels, and greatly improved overload protection accuracy are other examples where inherent mechanical limitations are alleviated by the SSPC. Another possible advantage of the SSPC is the capability of the solid-state device to current limit for fault protection. This capability offers many potential system improvements such as reduced transients, decreased generator fault capacity requirements, and perhaps even additional weight savings.

ADVANTAGES OF SOLID-STATE POWER CONTROLLERS

- COMPATIBILITY WITH DATA BUS CONTROL SYSTEMS
  - REMOTE CONTROL (ON-OFF-RESET)
  - TRIP INDICATION
- POTENTIALLY HIGHER RELIABILITY WITH LONGER LIFE
  - PC CAN REPLACE CONVENTIONAL BREAKER AND ASSOCIATED SWITCH
- CURRENT LIMITING (DC UNITS)
- REDUCED EMI
- PROTECTION ACCURACY GREATLY INCREASED

DEVELOPMENT STATUS

The basic concept of a PDC subsystem design employing computer control and solid-state switching devices was developed about ten years ago by LTV aircraft designers. This effort has progressed to a design and test simulator associated with the Navy and Air Force programs involving the A-7 Aircraft. This program has developed a basic systems application concept, a candidate control and monitoring system, and a flight configuration component designed with most of the basic electrical characteristics required of an SSPC. An extensive test program is planned for evaluation of this simulator, both as a system and on a component level.

A very substantial program has been carried on by Westinghouse Electric Corporation in both systems and components design. This program has resulted in control and interface hardware production as well as various breadboard power controller fabrications. Testing and demonstration programs are presently being performed with this hardware. Many programs are being performed by industry in systems analysis, such as Grumman Aerospace Corporation studies on the F-14 Fighter Aircraft, and all of these efforts should aid in the development of the technology involved.

The Manned Spacecraft Center has undertaken an evaluation program as a result of a feasibility study accomplished by LTV Aerospace Corporation indicating great potential improvements in spacecraft PDC subsystems applying SSPC's. Present efforts at this Center involve systems integration and interface requirements investigations being accomplished with the integrated avionics breadboard program. A limited amount of component evaluation has been accomplished to date on hardware purchased for the integration program, and although it must be kept in mind that these SSPC's are themselves breadboard units, initial test results indicate electrical characteristics equalling or surpassing expected values.

Future Manned Spacecraft Center plans include more component evaluation and systems integration, but the immediate efforts will be concentrated on flight packaging development in order to meet the demanding Shuttle time frame. Marshall Space Flight Center is also supporting and will continue to support component evaluation and development, especially in the area of high voltage semiconductor switches. Lewis Research Center will also support the National Aeronautics and Space Administration efforts in this field, presently concentrating on development of high voltage designs and components.

DEVELOPMENT STATUS

- PREVIOUS APPLICABLE WORK (LTV, W, GAC, ...)
- MSC INVESTIGATIONS (SYSTEM INTERFACE REQUIREMENTS, COMPONENT EVALUATION)
- FUTURE
  - MSC (PACKAGING AND COMPONENT EVALUATION)
  - MSFC (COMPONENT EVALUATION AND HIGH VOLTAGE DEVELOPMENT)
  - LRC (HIGH VOLTAGE COMPONENT DEVELOPMENT)

CONCLUDING REMARKS

The studies discussed here, as well as numerous unmentioned efforts in both system and component development, have precipitated great interest in the application of solid-state power controllers in the Shuttle PDC subsystem. The subsystem weight criticality and complex interfacing problems of the proposed Shuttle concepts present a difficult design task to the PDC subsystem designer, while the SSPC presents him with a very promising method of meeting both of these areas of concern.

Due to the potential advantages of a PDC subsystem applying SSPC's, development will surely continue both through Government and industry funding. There are numerous areas of SSPC development required for universal application, but the Space Shuttle application requires a qualified component within the next few years. In order to meet this requirement, system designers may limit themselves to a maximum rating SSPC, or compromise some electrical characteristics presently envisioned. However, even if design development is slowed temporarily in order to flight package and qualify today's candidate SSPC's, the potential improvements to the Shuttle PDC subsystem could provide the first major step in utilizing this technology to its fullest.

CONCLUDING REMARKS

- SOLID-STATE POWER CONTROLLERS ARE A PROMISING APPROACH TO SATISFYING THE SHUTTLE POWER CONTROL REQUIREMENTS
- PRESENT TECHNOLOGY OFFERS VARIOUS APPROACHES TO ELECTRONIC DESIGN
- SOME DEVELOPMENT WORK STILL NEEDED