

July 1971

Brief 71-10253

NASA TECH BRIEF

Marshall Space Flight Center



NASA Tech Briefs announce new technology derived from the U.S. space program. They are issued to encourage commercial application. Tech Briefs are available on a subscription basis from the National Technical Information Service, Springfield, Virginia 22151. Requests for individual copies or questions relating to the Tech Brief program may be directed to the Technology Utilization Office, NASA, Code KT, Washington, D.C. 20546.

Low-Temperature Bonding of Temperature-Resistant Electronic Connections

Flat metal surfaces can be bonded by using a low-temperature-melting intermediate material and applying pulse heating and pressure. The resultant bond is strong, electrically conductive, and resistant to melting at temperatures well above the melting point of the intermediate material. The technique can be applied to provide a joint that will resist temperatures in excess of 573 K compared to solder at 454 K.

The new technique is now used for joining gold-plated Kovar ribbon leads to copper printed circuit pads plated with indium or tin. The leads require no special preparation, and the method is relatively insensitive to process variables.

The copper pads on the printed board are plated with from 19.3 to 50.8 nm of either indium or tin. Tests are now being conducted to determine the relative merits of these two low-temperature-melting materials. Heat is applied with a parallel-gap pulse bonder. The tip temperature is controlled between 673 and 773 K, and the pulse time is from 4 to 5 sec.

It has been proven conclusively that the bonds do not remelt at temperatures that are well above the melting point of the intermediate. Analysis

by electron secondary emission shows that little or no low-temperature-melting material remains at the interface, and that the gold is largely either consumed by alloying or squeezed from the interface. Neither copper nor Kovar is melted.

Application of this technique to bonding beam-lead devices to thin-film and thick-film substrates should be investigated. Such processes should interest those involved in semiconductor design and electronic assembly manufacturing.

Note:

Requests for further information may be directed to:

Technology Utilization Officer
Code A&TS-TU
Marshall Space Flight Center
Huntsville, Alabama 35812
Reference: TSP71-10253

Patent status:

No patent action is contemplated by NASA.

Source: R. F. Peluso of
Martin Marietta Corp.
under contract to
Marshall Space Flight Center
(MFS-20909)

Category 08