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Brief 70-10524

NASA TECH BRIEF

Latching Overcurrent Circuit Breaker

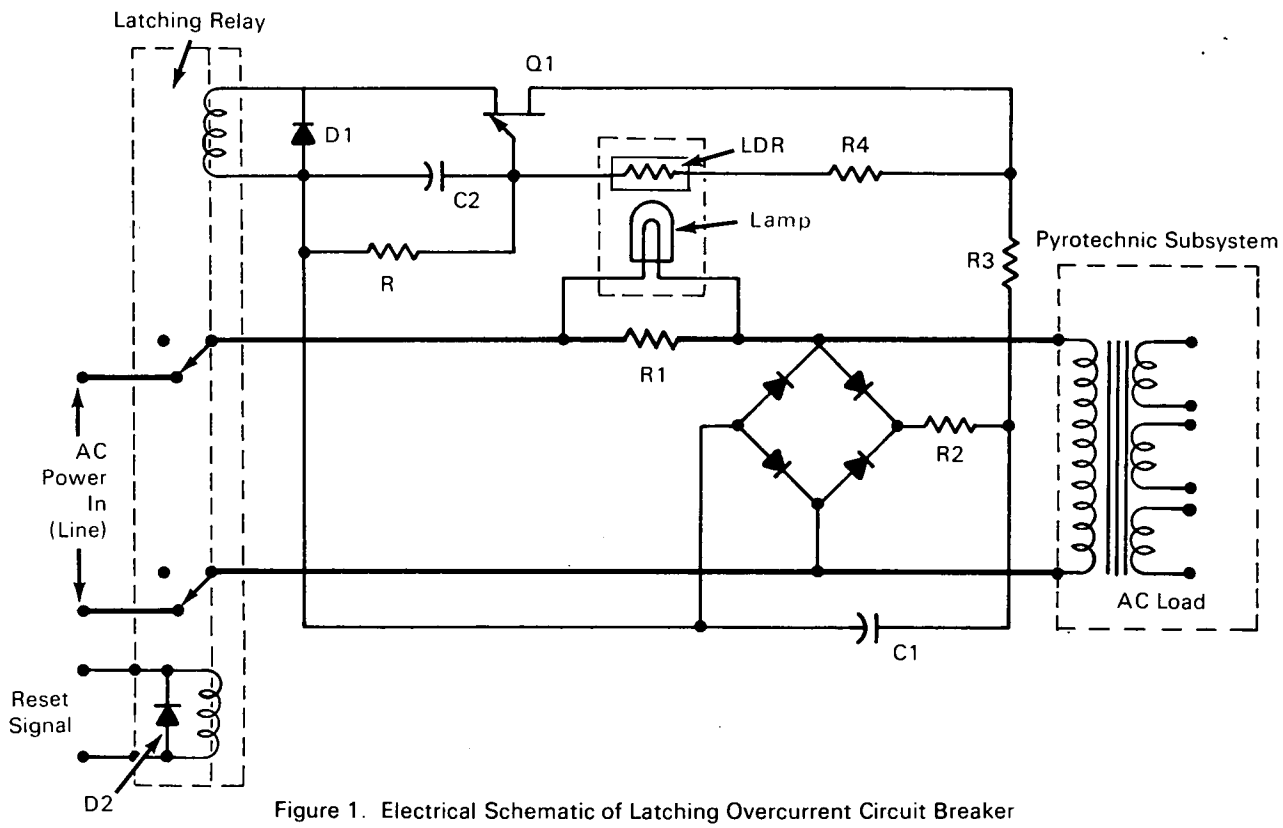

Figure 1. Electrical Schematic of Latching Overcurrent Circuit Breaker

Manufacturers of electrical test equipment and small appliances and personnel concerned with repeated nondestructive preflight testing should be interested in a latching overcurrent circuit breaker. It consists of a preset current amplitude sensor, and a lamp-photo-resistor combination in a feedback arrangement which energizes a power switching relay. The ac input power is removed from the load at predetermined current amplitudes.

Figure 1 illustrates the action of the circuit breaker. A double pole latching relay interrupts both sides of the ac line from the control circuit and ac load to be controlled. A 3.9 ohm resistor (R1), placed in series with one side of the line, produces a small voltage drop proportional to the amount of current drawn by the ac load. A dc voltage to the unijunction transistor (Q1) is supplied by a bridge rectifier. The 15 ohm resistor (R2) provides current limiting and the 47 μf

(continued overleaf)

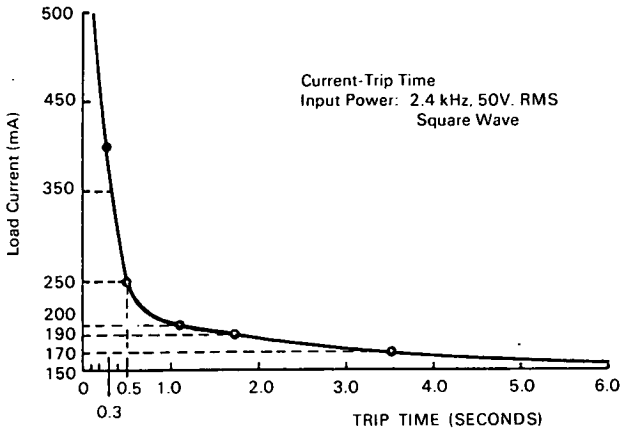

Figure 2. A Plot of Load Current Versus Trip Time

capacitor (C1) provides filtering. A 390 ohm resistor (R3) supplies temperature compensation for the unijunction transistor. The sensor for the circuit is a combination light dependent resistor (LDR) and lamp assembly.

As the load current increases, the illumination from the lamp increases and lowers the resistance of the light dependent resistor. The 2.0 μf capacitor (C2) charges to the peak point voltage of the unijunction transistor causing it to fire; this action energizes the latching relay which causes the ac power line to be disconnected from the load and control circuit. Diode (D1) absorbs the back EMF from the activated relay coil. The time constant formed by the 20,000 ohm resistance (R4) and 2.0 μf capacitor determines the required trip time. The value of R1 determines the trip current amplitude.

Capacitor C1 stores sufficient energy to ensure operation of the trip circuit when an overcurrent surge or transient causes a drop in line voltage. The circuit is designed to function reliably for fault currents less than 0.5 amp. Once the relay latches, which removes ac power from the load and control circuit, a pulsed reset signal supplied to the reset will place the ac load and control circuit back in operation. Diode (D2) absorbs the back EMF from the activated reset coil. The reliability and performance of a laboratory test model, upon repeated interruption of fault currents less than 0.5 amp, are satisfactory. Figure 2 depicts a plot of load currents versus trip times for the circuit adjusted to pass a steady state current of 150 mA without tripping.

Notes:

1. Resistor R in Figure 1 may or may not be required, depending on the dark resistance of the LDR and the leakage of capacitor C2.
2. No additional documentation is available. Specific questions, however, may be directed to:

   Technology Utilization Officer
   NASA Pasadena Office
   4800 Oak Grove Drive
   Pasadena, California 91103
   Reference: B70-10524

Patent status:

Inquiries about obtaining rights for the commercial use of this invention may be made to NASA, Code GP, Washington, D.C. 20546.

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