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Brief 70-10496

NASA TECH BRIEF

Rapid Method for Interconversion of Binary and Decimal Numbers

The problem:

To increase the speed of interconversion of binary and decimal numbers by avoiding the use of time-consuming software subroutines or of slow iterative sequential logic circuits.

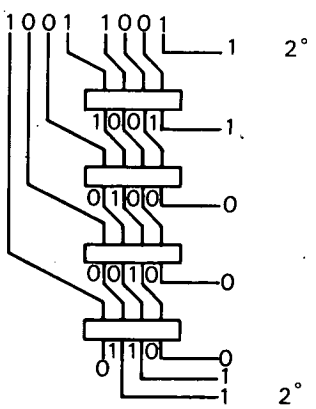

Figure 1

The solution:

The conversion is accomplished by a decoding tree consisting of a few 40-bit semiconductor read-only memories. The speed of conversion is proportional to the propagational delay in the operation of the read-only memory.

How it's done:

The decimal-to-binary conversion algorithm is based on the divided-by-2 iterative equation

$$\frac{Q_{j-1}}{2} = Q_j + b_i \qquad \begin{matrix} j = 1,2,\text{---},n \\ i = j-1 \end{matrix}$$

where Q_0 = the decimal number N, Q_j = quotient of jth iteration, and b_i = remainder of jth iteration, which is also the converted binary digit. The decimal number digits are represented in the 8-4-2-1 BCD form. The dividing-by-2 process is performed on a decimal number by shifting, and the shifting is accomplished by decoding. The truth table of the decoder is emulated by a 40-bit read-only memory module, and a converter is formed by connecting many identical modules in the form of a tree. The tree consists of j levels and k columns, where j is the number of binary digits minus three and k is the number of decimal digits. The conversion speed and the number of modules required for a converter are dependent only on j.

Decoder Input				Decoder Output			
C_1	X_8	X_4	X_2	Y_8	Y_4	Y_2	Y_1
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0
0	0	1	1	0	0	1	1
0	1	0	0	0	1	0	0
1	0	0	0	0	1	0	1
1	0	0	1	0	1	1	0
1	0	1	0	0	1	1	1
1	0	1	1	1	0	0	0
1	1	0	0	1	0	0	1

Table 1

Figure 1 is a decoding tree for converting the decimal number $(99)_{10}$ to the binary number $(1100011)_2$. The decoding tree implements the divided-by-2 conversion algorithm; the tree consists of four decoders having four inputs $C_1X_8X_4X_2$ and four outputs $Y_8Y_4Y_2Y_1$, with the decoding function indi-

(continued overleaf)

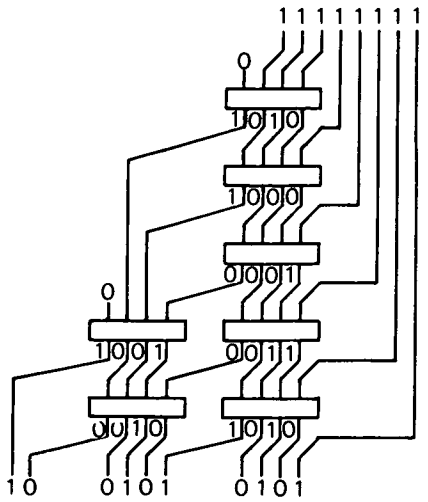

Figure 2

cated in Table 1. The decoder is emulated by a 40-bit read-only memory, but the structure of the decoding tree grows in complexity such that for any given decimal number having p digits, the number of decoders, M_{db}, required for the converter is

$$M_{db} = 2p(p-1) - (1/2)(4p-n-1)(4p-n)$$

where n is the number of digits in the resulting binary number.

The binary-to-decimal conversion algorithm is based on the multiplied-by-2 iterative equation

$$S_{n\ 1} = 2S_{n\ j+1} + b_{n\ j} \quad j = 1,2,\text{---},n$$

where $S_{n\ j}$ = sum of jth iteration, $S_{n\ j} = b_{n-1}$, b_{n-j} = binary digit at position n−j, and S_0 is the resultant number in decimal form. Implementation of the above equation is accomplished as described previously.

Figure 2 is a decoding tree for converting the binary number $(11111111)_2$ to the decimal number $(255)_{10}$. The decoding tree implements the multiplied-by-2 conversion algorithm. The decoding tree consists of seven decoders having four inputs $X_8X_4X_2X_1$ and four outputs $C_0Y_8Y_4Y_2$. The decoding function is shown in Table 2. The number of decoders, M_{bd}, required for a given converter is

Input				Output			
X_8	X_4	X_2	X_1	C_0	Y_8	Y_4	Y_2
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0
0	0	1	1	0	0	1	1
0	1	0	0	0	1	0	0
0	1	0	1	1	0	0	0
0	1	1	0	1	0	0	1
0	1	1	1	1	0	1	0
1	0	0	0	1	0	1	1
1	0	0	1	1	1	0	0

Table 2

$$M_{bd} = n(p-1) - (3/2)p(p-1) - \left(\frac{n-4}{10}\right)_1$$

where the term (K)/I as $(K)_1$ is defined as the integral part of K.

Notes:

1. With typical commercially available read-only memories, the speed of a 15-bit binary-to-decimal converter is 540 ns and a 4-digit decimal-to-binary converter is about 495 ns. Conversion speeds are at least 50 to 100 times faster than methods in current use.
2. Since the converter is a combinational net, random transient disturbances are without effect and timing and clocking are not required.
3. Additional information is available from:
   Technology Utilization Officer
   Ames Research Center
   Moffett Field, California 94035.
   Reference: TSP70-10496

Patent status:

No patent action is contemplated by NASA.

Source: Raymond S. Lim
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