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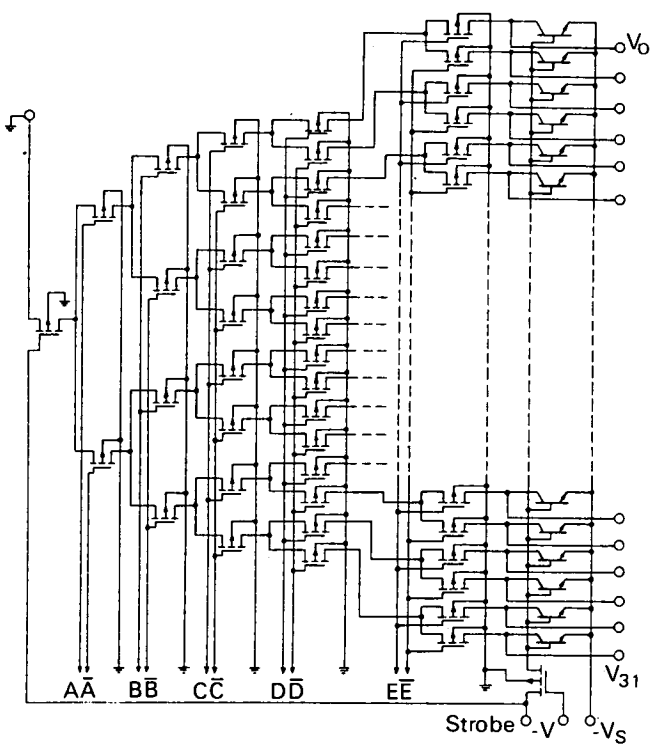
Brief 70-10372

NASA TECH BRIEF

Integrated Circuit Random-Access Memory Decoder

The problem:

Develop a decoder, for use in a medium-speed random-access memory, which consumes negligible power and exhibits low output impedance, and to maintain compatibility with present integrated circuit (IC) technology.



Schematic of Basic 32-Output BIMOS Decoder

The solution:

Using a complementary-symmetry circuit configuration composed of MOS and n-p-n bipolar devices minimizes power consumption. An emitter-follower output stage provides low output impedance. The MOS transistors are p-channel enhancement-mode devices.

How it's done:

The circuit shown in the figure has a five-bit binary input with corresponding address complements. When a given address signal is applied to lines A-$\bar{A}$, B-$\bar{B}$, C-$\bar{C}$, D-$\bar{D}$ and E-$\bar{E}$, only one path, comprised of five p-channel transistors, conducts. Because the strobe signal is at ground potential during the quiescent state, the n-p-n bipolar devices are biased in the ON state, and all output devices are forced to the negative supply voltage, $-V_S$. Upon command ($-V_S$ on strobe terminal), the common p-channel strobe-controlled transistor activates the selected address line and switches the output of that address line to ground. The other 31 unselected outputs remain at the negative supply voltage. When the strobe signal returns to ground potential, the selected output voltage reverts to $-V_S$. The maximum width of the strobe pulse is limited by the time required for unselected lines to discharge to ground. Because of the complementary structure, quiescent power dissipation is negligible and circuit operation is essentially independent of device parameters. The common source-drain connections inherent in MOS ICs enable the bipolar devices to function as output units with a minimal use of silicon areas; additional space is conserved by incorporating a MOS device, in place of a diffused resistor, to drive the base of the bipolar transistor.

Notes:

1. The decoder circuit with an emitter-follower drive scheme results in low power dissipation and high speed operation. This circuit should find wide use in integrated low power memory systems and in applications where a decoder must drive a high capacity line in short time periods.

(continued overleaf)

2. The following documentation may be obtained from:

Clearinghouse for Federal Scientific
and Technical Information
Springfield, Virginia 22151
Single document price $3.00
(or microfiche $0.65)

Reference:
NASA-CR-86115 (N69-14036), Research to Develop Data Storage

Patent status:

Inquiries about obtaining rights for the commercial use of this invention may be made to NASA, Code GP, Washington, D.C. 20546.

Source: S. Katz of
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